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Power Converters

Baden, Switzerland
7–14 May 2014

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Abstract

These proceedings collate lectures given at the twenty-eighth specialized course organised by the CERN Accelerator School (CAS). The course was held at the Hotel du Parc, Baden, Switzerland from 7 - 14 May 2014, in collaboration with the Paul Scherrer Institute. Following introductory lectures on accelerators and the requirements on power converters, the course covered components and topologies of the different types of power converters needed for particle accelerators. Issues of design, control and exploitation in a sometimes-hostile environment were addressed. Site visits to ABB and PSI provided an insight into state-of-the-art power converter production and operation, while topical seminars completed the programme.


Power Converters

Preface

The aim of the CERN Accelerator School (CAS) is to collect, preserve and disseminate the knowledge accumulated in the world's accelerator laboratories over the years. This applies not only to general accelerator physics, but also to related sub-systems and associated technologies, and to how these are adapted to particular requirements. This wider aim is achieved by means of specialized courses currently held yearly. The topic of the 2014 specialized course was Power Converters and was held at the Hotel du Parc, Baden, Switzerland from 7 to 14 May 2014.

The course was made possible through the fruitful collaboration with the Paul Scherrer Institute in Villigen, Switzerland, in particular through the efforts of Lenny Rivkin, René Künzi, Marlen Bugmann and Daniela Lerch.

The backing of the CERN management and the guidance of the CAS Advisory and Programme Committees enabled the course to take place, while the attention to detail of the Local Organising Committee and the management and staff of the Hotel du Parc ensured that the school was held under optimum conditions.

Financial support offered by OCEM, Italy and CAENels, Slovenia allowed scholarships to be offered to deserving students who would not otherwise have been able to attend, while both PSI in Villigen and ABB in Turgi hosted extremely interesting half-day visits. There was also a small industrial exhibition featuring OCEM, CAELels, Hivolt and Ampegon.

Special thanks must go to the lecturers for the preparation and presentation of the lectures, even more so to those who have written a manuscript for these proceedings.

The enthusiasm of the 84 participants of 21 nationalities, from institutes in 14 countries, provides convincing proof of the usefulness and success of the course.

For the production of the proceedings we are indebted to the efforts of Barbara Strasser and to the CERN E-Publishing Service, especially Valeria Brancolini for her very positive and efficient collaboration.

These proceedings have been published in paper (black and white) and electronic form. The electronic version, with full colour figures, can be found at https://cds.cern.ch/collection/CERN%20Yellow%20Reports.

Roger Bailey
CERN Accelerator School

PROGRAMME FOR POWER CONVERTERS, BADEN, SWITZERLAND
7 – 14 May, 2014

Time	Wednesday 7 May	Thursday 8 May	Friday 9 May	Saturday 10 May	Sunday 11 May	Monday 12 May	Tuesday 13 May	Wednesday 14 May
08:30		Introduction and Accelerator Basics	Power Converters and Power Quality I	RF Solid State Amplifiers		Thermal Design		Simulations
09:30		R. Bailey	K. Kahle	J. Jacob		R. Kuenzi		N. Ngada
09:30		Requirements on Power Converters	EMC	Long Pulse Converters		Design Methods and Tools		Power Converters for Accelerators
10:30	**A R R I V A L**	J.-P. Burnet	A. Charoy	J. Eckoldt	**E X C U R S I O N**	T. Meynard		R. Visintini
		COFFEE	**COFFEE**	**COFFEE**		**COFFEE**		**COFFEE**
11:00		Definition of Power Converters I	Power Converters and Power Quality II	Solid State Power Modulators		Regulation Theory	**Half Day at ABB + Half Day at PSI**	Putting It Into Practice
12:00		D. Aguglia	D. Siemaszko	J. Biela		F. Bouvet		J.-P. Burnet
12:00		Definition of Power Converters II	Switched Mode 1 Q Converters	Power Converter Controls: Radiation Risks & Mitigations		High Precision Current Measurement for Power Converters		Closing Remarks
13:00		D. Aguglia	R. Petrocelli	B. Todd		M. Cerqueira		R. Bailey
		LUNCH	**LUNCH**	**LUNCH**		**LUNCH**		**LUNCH**
14:30	**D A Y**	Active Devices	Switched Mode 4 Q Converters	Power Filter Design		A Review of ADCs & DACs and their Application		**D E P A R T U R E**
15:30		M. Rahimo	Y. Thurel	R. Kuenzi		J. Pickering		
15:30		Passive Devices Magnetic	Converters for Low Frequency Machines	Protection and Interlocks		Controls and Interfaces		
16:30		P. Viarouge	J.-F. Bouteille	B. Todd		Q. King		
		TEA	**TEA**	**TEA**		**TEA**		
17:00		Passive Devices Capacitive	**Seminar** Proton Therapy	**Seminar** Swiss FEL, the X-Ray Free Electron Laser at PSI		**Seminar** Overview on Latest Development of ABB's Power Semiconductors Technology and Research Topics		
18:00	**Registration**	R. Gallay	G. Goitein	H. Braun		I. Nistor		
19:00	**Buffet Dinner**				**Special Dinner**			
19:30		**Dinner**	**Dinner**	**Dinner**		**Dinner**	**Dinner**	

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Requirements for Power Converters

J.-P. Burnet
CERN, Geneva, Switzerland

Abstract
This paper introduces the requirements for power converters needed for particle accelerators. It describes the role of power converters and the challenges and constraints when powering magnets. The different circuit layouts are presented as well as the operating cycles. The power converter control and high precision definition are also introduced. This paper lists the key circuit parameters to be taken into consideration to properly specify a power converter that can be compiled in a functional specification.

Keywords
Magnet Power supply; power electronics; power converter control.

1 Introduction

Particle accelerators are very special machines that consume a lot of electricity. The main devices consuming this energy are the magnets and the radio-frequency (RF) systems. It represents from 70% to 90% of the total energy needed for a machine. The way to power these two main loads is always special and needs a lot of care to obtain the right performance from the machine, see Fig. 1. The performance of the power converters directly impacts upon the beam quality, and the requirements for power converters are outside the range of classical industrial products. This paper will introduce the power converters needed for particle accelerators, and their main parameters.

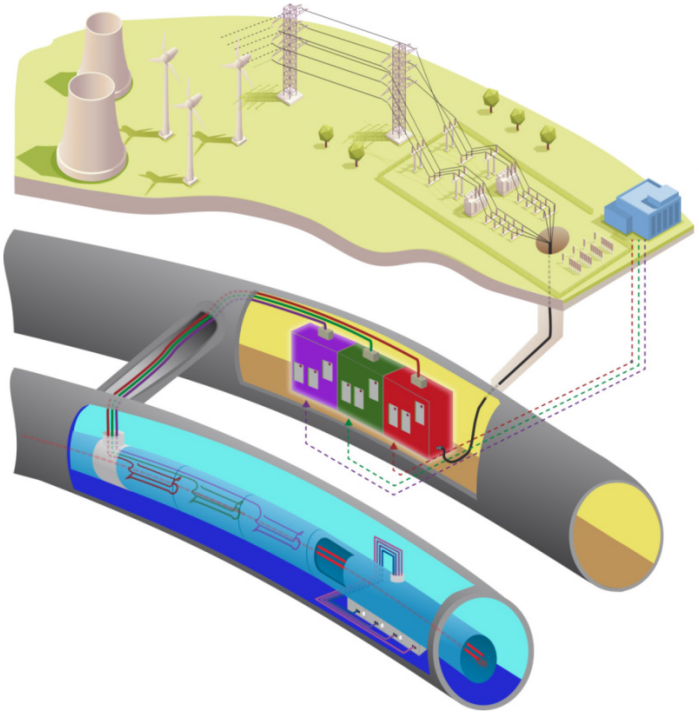


Fig. 1: Particle accelerator powering chain

http://dx.doi.org/10.5170/CERN-2015-003.1

2 Type of loads

The most popular particle accelerator today is the synchrotron machine. In such machines, a large number of magnets is used to control the beam and, depending of the type of particle, there may be many radio-frequency cavities for acceleration, see Fig. 2. This paper will mainly concentrate upon magnet powering, as radio-frequency powering is covered by another paper.

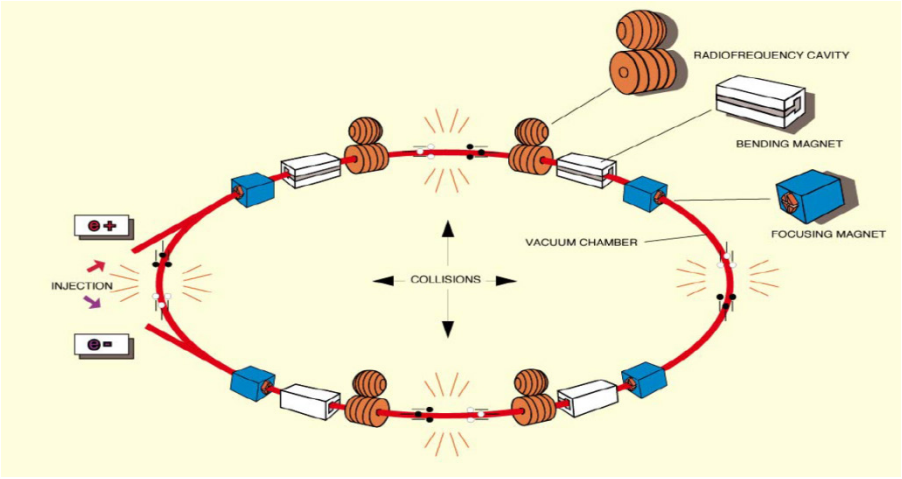


Fig. 2: Basic concept of a synchrotron machine

The power converters or power supplies are the devices that take energy from the electrical grid and transform it to control the flow of energy supplied to the magnets or radio-frequency power amplifiers. The magnet power converters are always of an AC/DC type.

3 Powering magnets

Different types of magnets are needed for particle accelerators, see Fig. 3. The two main families are the dipole magnets that bend the beam and the quadrupole magnets that focus the beam. Sextupole magnets are used to correct the chromaticity, and octupole magnets control the Landau damping. Particle accelerators also need a lot of small correctors to compensate for local distortion due to magnet imperfections, alignment, etc.

A synchrotron is composed of a periodic repetition of focus-defocus (FODO) cells. Each cell contains dipole, quadrupole and sextupole magnets, see Figs. 4 and 5 [1].

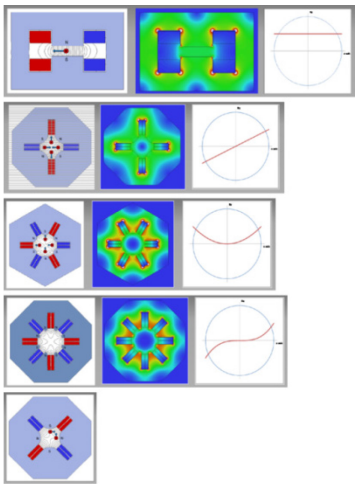


Fig. 3: Different magnet types: (a) dipole magnet; (b) quadrupole magnet; (c) sextupole magnet; (d) octupole magnet.

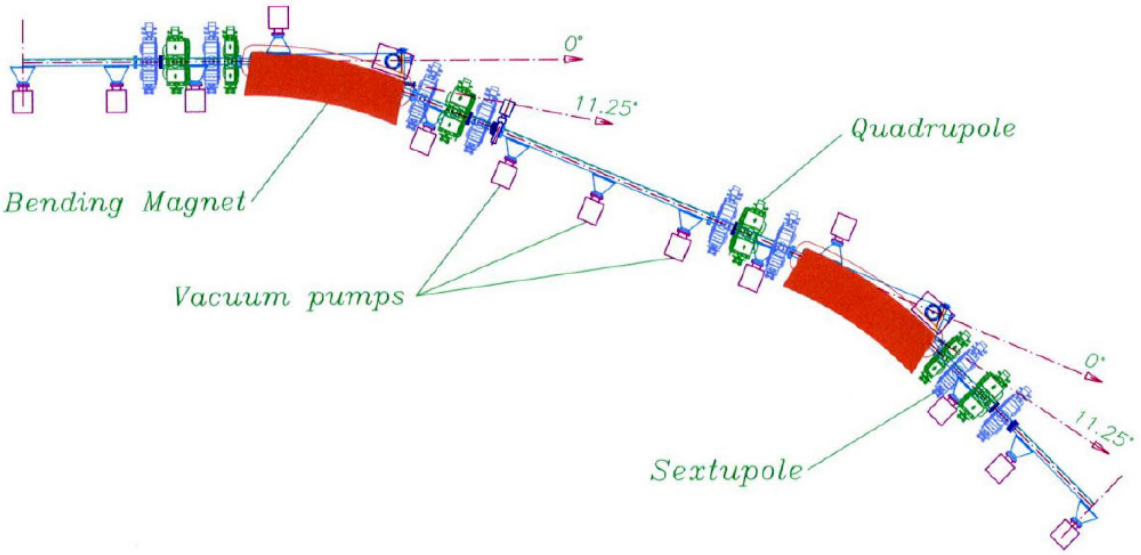


Fig. 4: Arrangement of the magnets within one unit cell of the SESAME storage ring

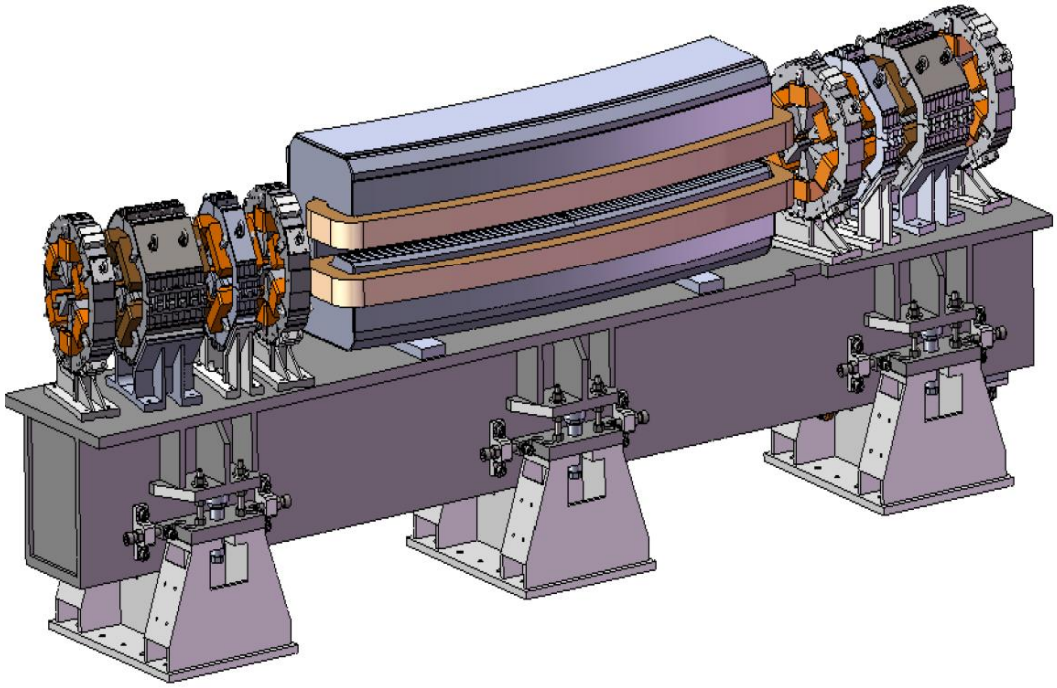


Fig. 5: SESAME FODO cell

The magnets are made with a magnetic core (laminated or not) and winding coils. As seen by the power converters, the magnets are always inductive loads. The equivalent circuit is an inductance in series with a resistor (due to the resistance of the coils and the DC cables between the power converter and the magnet).

In a synchrotron the beam energy is proportional to the magnetic field of the dipole magnets. The magnetic field is generated by the current circulating in the magnet coils, see Fig. 6. To then control the beam, the operators need to control the current through the magnets.

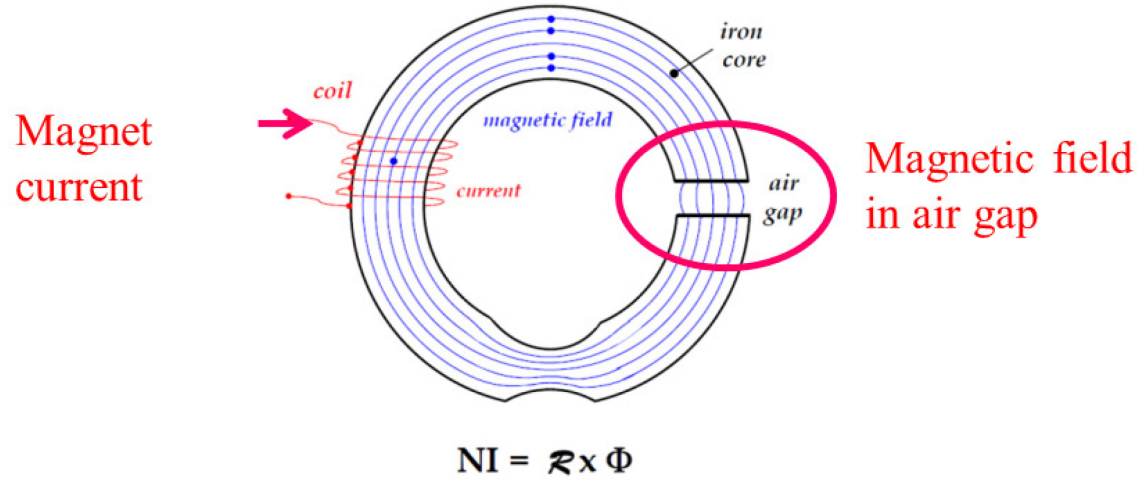


Fig. 6: Magnetic field

The main specification for the magnet power converters is high precision control of the current delivered to the magnets. Typically, the good field region of a magnet is defined within $\pm 10^{-4}$ $\Delta B/B$ and the typical performance of the power converter is to control the current to the order of 10^{-5} of the maximum output current.

The main difficulty is the fact that in a magnet the relation between the current and magnetic field is not linear due to magnetic hysteresis of the core and the eddy currents, see Fig. 7.

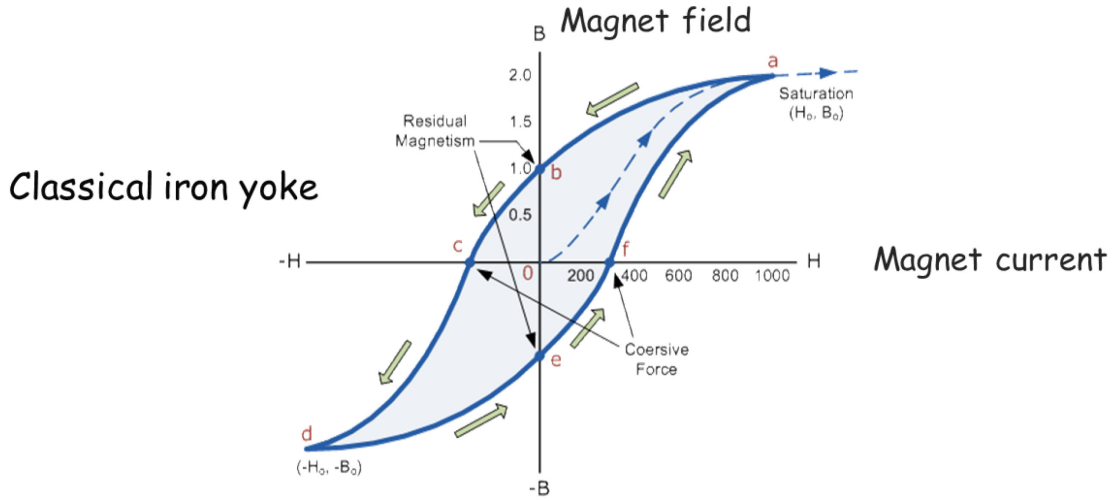
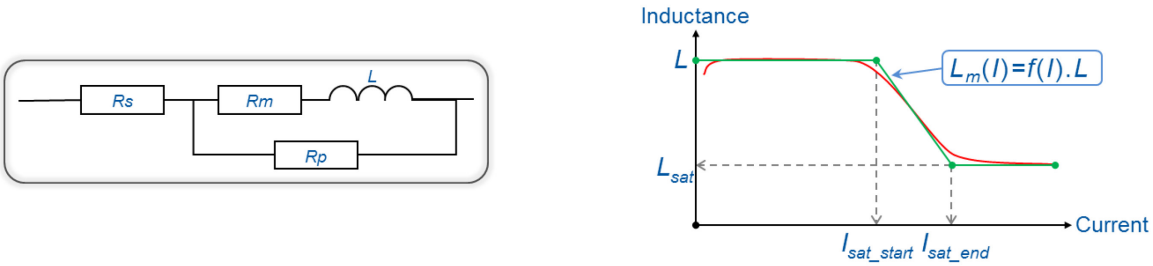


Fig. 7: Magnet hysteresis

This problem is one of the major difficulties when operating a synchrotron that is to work with different beam energies.

3.1 Magnet parameters

A good model of the load is needed to control the current delivered by the power converters. The transfer function gives the main parameters of the circuit which are inductance and resistance. To improve control, it is mandatory to include the saturation curve of the magnet to adapt the current loop parameters depending of the current level, see Fig. 8(b).



(a) (b)

Fig. 8: Magnet model: (a) equivalent circuit of the load (b) inductance value versus current

3.2 Circuit layout

The magnets can be powered individually or in series. The main advantage to powering them individually is the increase in flexibility of the beam optics. The main drawback is the uncertainty of the magnetic field between the magnets due to the magnet current history (hysteresis effect). The global cost is also higher, with more DC cables and more power converters. In some cases it can become mandatory to split a circuit because of the size of the load becoming too large. For example, this is the case for the LHC superconducting dipoles and quadrupoles, where the total energy of the circuit is very huge (8 GJ). The machine was therefore divided into eight sectors, see Fig. 9. Even with this split, the inductance of one octant is 15 H with a stored energy of more than 1 GJ. This configuration needs high-precision control of the magnet current as well as excellent tracking of the magnet current between the eight sectors [2].

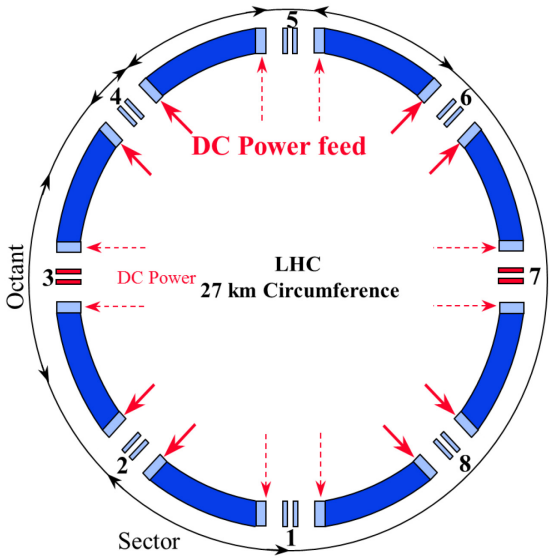


Fig. 9: Split of the LHC dipole and quadrupole circuits

The classical solution for dipole, quadrupole, and sextupole magnets is to connect all of them in series. The main advantage is that this suppresses the uncertainty of the magnetic field between magnets and assures easy control of these circuits. In some cases, trim power converters are needed to adapt the magnetic field locally. This solution is globally the cheapest one, but it requires a large power converter to power such circuits. As an example, the SPS machine requires a power system of 150 MW to power all of the dipole in series. A special distribution of power sources was chosen to reduce the common mode voltage applied to the magnets, see Fig. 10.

In some cases, the creation of nested circuits reduces the cost of the powering system. In a series of magnets that are powered by a main power converter, some magnets have additional connections to a trim power converter to adjust their current, see Fig. 11. This creates some difficulties for the power converter control as the different power converters are coupled by their load. This type of scheme isn't recommended due to the induced complexity. However, in some case the savings are such that it is difficult to avoid this solution [3].

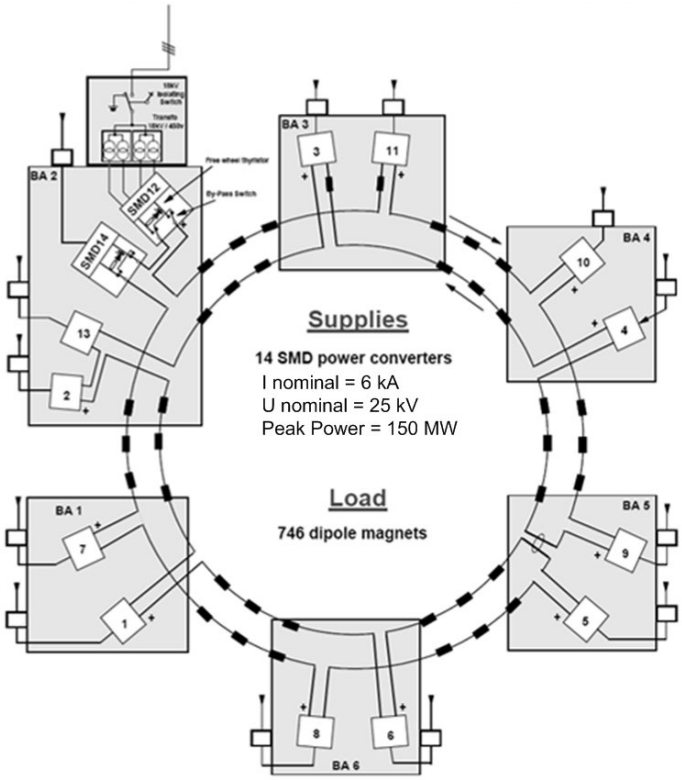


Fig. 10: SPS dipole power system

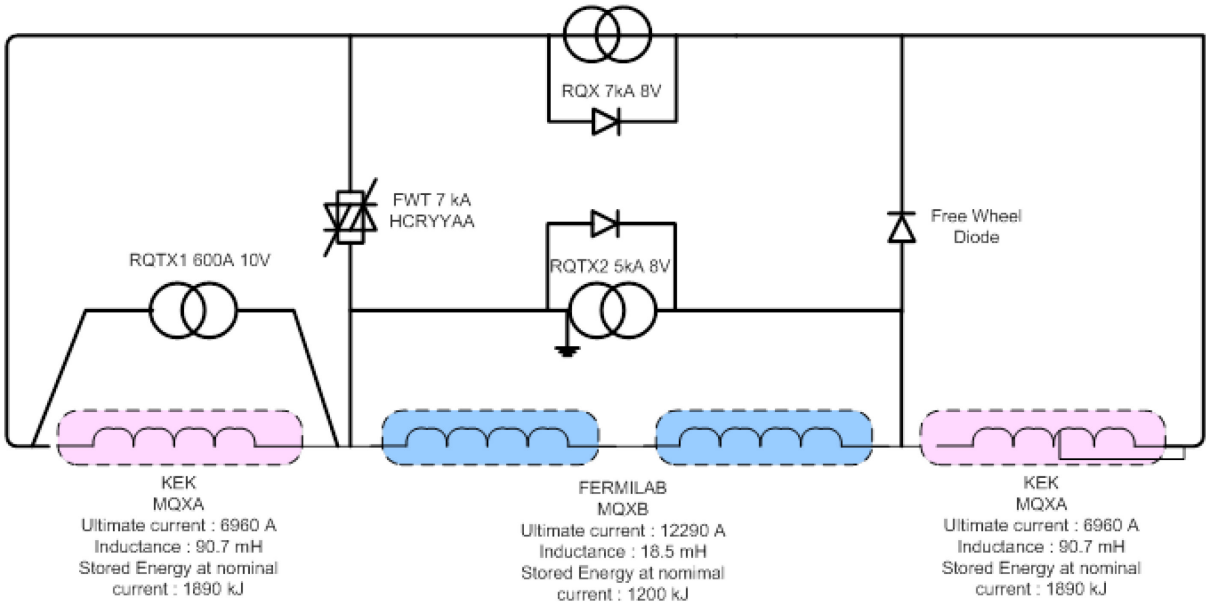


Fig. 11: LHC inner triplet powering scheme

3.3 Powering optimization

Powering optimization plays with the magnet parameters, the power converter parameters, and the circuit layout. For the same integral magnetic field, the magnet can be laid out in different ways. The magnet parameters are the number of turns per coil, the maximum current, the current density in the conductor, and the length of the magnet [4].

The number of turns per coil does not influence the total power losses in the magnet. By increasing the number of turns, the current required decreases linearly. This reduces the losses in the DC cables and power converters. The drawback is the higher voltage applied to the magnets and the increased size of the magnet due to insulation.

The magnet's current density determines the magnet's losses. The choice is made based on economic criteria. High current densities result in a small conductor cross-section, but with water cooling. This reduces the size of the magnet and thus the capital costs, but it requires larger power converters and gives increased running costs due to the magnet's losses. By lowering the current density, the electricity bills can be strongly reduced but at the price of having to invest in larger magnets, as shown in Fig. 12. A global optimization has to be carried out to find the best economical solution for the magnets as well as for the power converters.

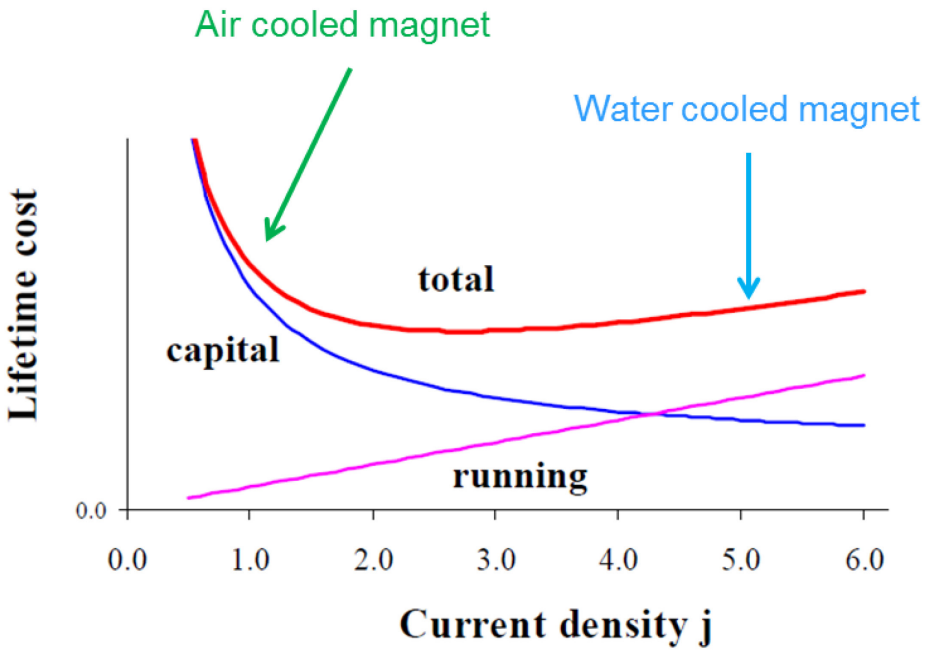


Fig. 12: The variation in magnet capital cost, running cost, and total lifetime cost versus conductor current density.

Another way to reduce power consumption is to reduce the time during which the magnets are powered. This is, for example, the case for linacs and transfer lines where the beam isn't always present, see Fig. 13. The idea is to power the magnets only when the beam is present, and this has a strong impact on electricity consumption. For example, in Linac4, the beam is pulsing at 2 Hz while the beam is present for 2 ms. The duty is then 0.4%. By pulsing the magnets, when compared to DC magnets, the savings are enormous (99%). This technique requires special designs for those power converters where energy storage can be implemented.

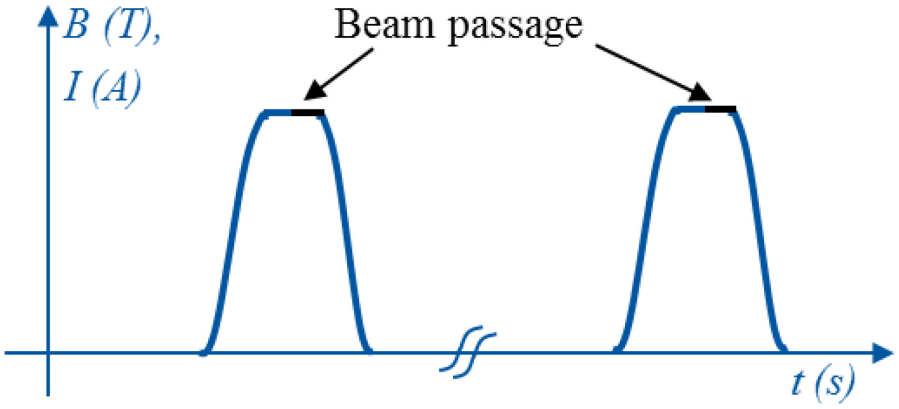


Fig. 13: Beam passage versus time

3.4 Magnet grounding

For safety reasons, magnets are isolated from the electrical grid. The power converter needs an isolation transformer in its topology. Magnets are connected to the ground at one point; they can't be left floating with their parasitic capacitances. One polarity can be connected directly to the ground through a resistor to limit the earth fault current, or via a divider for better voltage sharing, see Fig. 14. The ground current is monitored and stops the power converter in the case of an earth fault in the DC circuit.

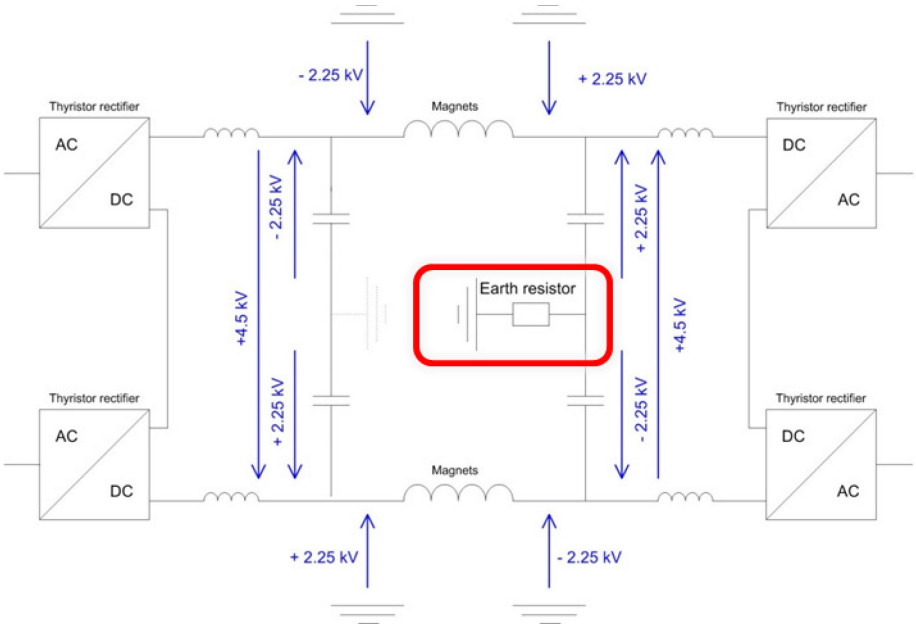


Fig. 14: An example of earthing the system

For a large number of magnets in series, the arrangement of multiple power sources can be made so that the common mode voltage of the magnets (any polarity of the magnet to ground) is reduced, when compared to the total applied voltage in differential mode. As shown in Fig. 14, the total applied voltage is 9 kV while the maximum common voltage of the magnets is limited to 2.25 kV.

3.5 Magnet protection

The magnets will have an interlock system that requests the power converter to stop in the event of any faults. For warm magnets, it is quite simple (water flow, thermostat, red button, etc.) For superconducting magnets, it is quite complex (quench protection, cryogenics, etc.)

In the event of a fault, the magnet current will be stopped but, because the magnets are inductive loads, the circuit can't be opened. The power converters assure a freewheeling path to the current, and the decay time is determined by the time constant of the circuit (L, R). In some cases, an additional dump resistor is needed to accelerate the discharge time, see Fig. 15.

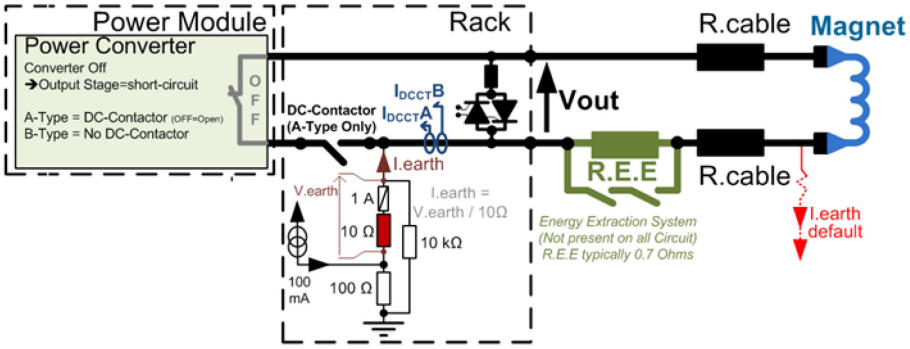


Fig. 15: Output circuit for magnet protection

3.6 Operation cycle

Magnet operation has a strong impact on the power converter topology and on power converter ratings. The magnet current cycle has to be defined from the beginning of a project, see Fig. 16.

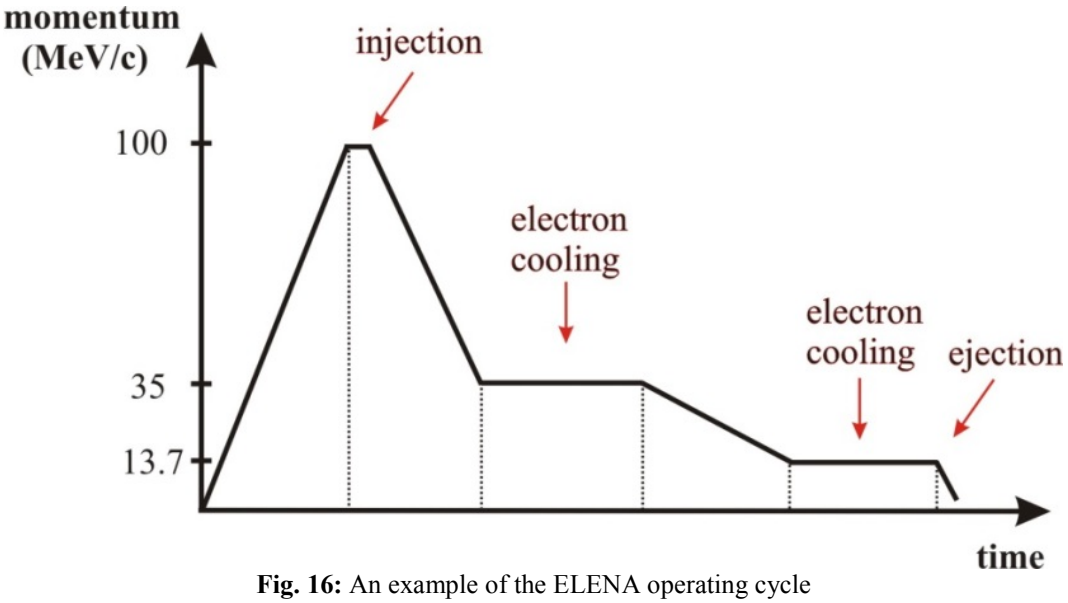


Fig. 16: An example of the ELENA operating cycle

The main parameters to be defined are the minimum and maximum operating current and the ramp rates. This will define the voltage needed and the topology of the converters. If the applied current and voltage are always positive, then a one-quadrant converter can be selected. If the current is always positive but the voltage is bipolar, then the power converter must be of the two-quadrant type. If the voltage and the current are bipolar, then, a four-quadrant power converter will be required, see Fig. 17.

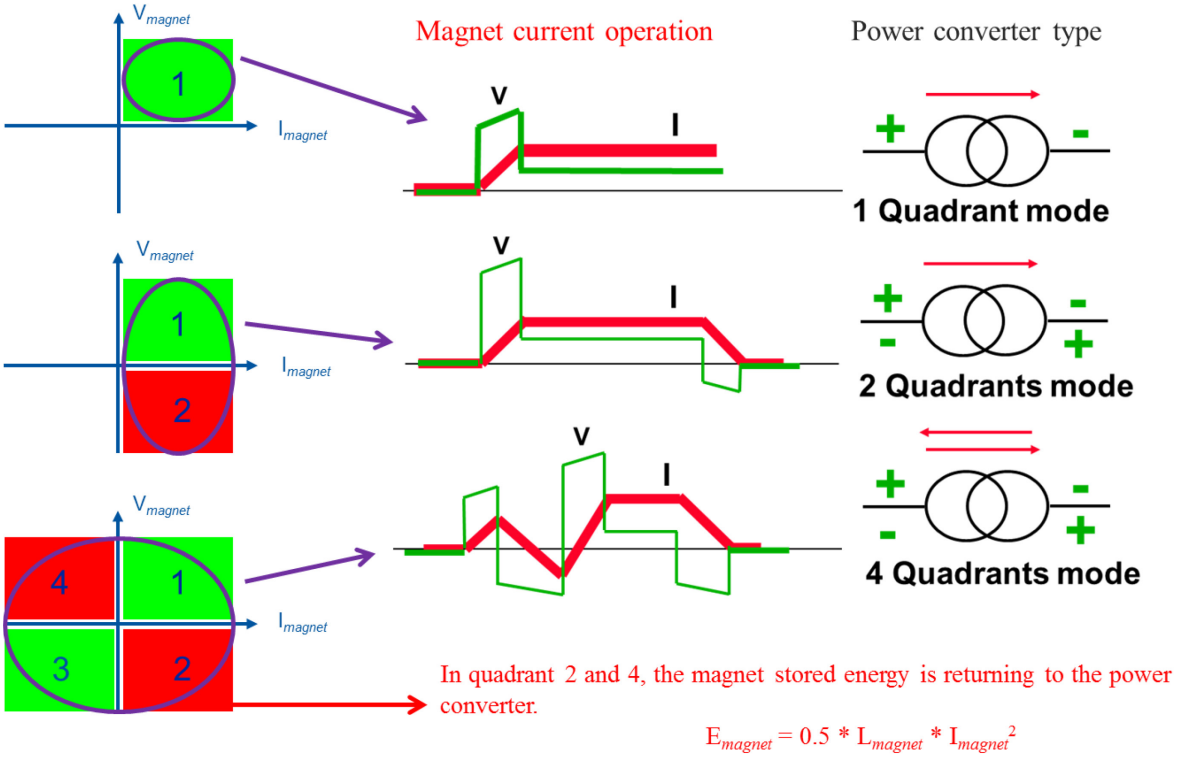


Fig. 17: The power converter type depends upon the operating cycle

4 Power converters

The power converter types will be introduced in the following papers. Control of power converter current is a challenge, and the main principles are described below.

4.1 Power converter control

Power converter performance has to be defined at the beginning of the project, based on the accelerator's requirements. The power converters needed for particle accelerators are always of high-class precision. The term 'precision' is only a generic term covering accuracy, reproducibility, and stability. For each power converter, the requirements depend on the magnet type and function. The most demanding are the dipole and quadrupole magnets, typically in the order of $1–10 \times 10^{-5}$, while the performance for corrector magnets are less demanding, typically in the order of $1–10 \times 10^{-4}$.

Power converters are always of the current control type, and the control principle is shown in Fig. 18. The power converter receives a current reference from the control room that needs to be executed with precise timing. All of the machine's magnets need to be synchronized, and a central timing system is distributed to all power converters and other accelerator devices. The precise execution of the current reference is one of the most challenging aspects of the control system.

The performance of the current control can be monitored through the tracking error, which is the ability of the power converter to follow the reference function. The static part of the tracking error is linked to static performance (accuracy and reproducibility). The dynamic part comes from timing error and regulation lagging error. All of these requirements lead to a definition for the power converter controller.

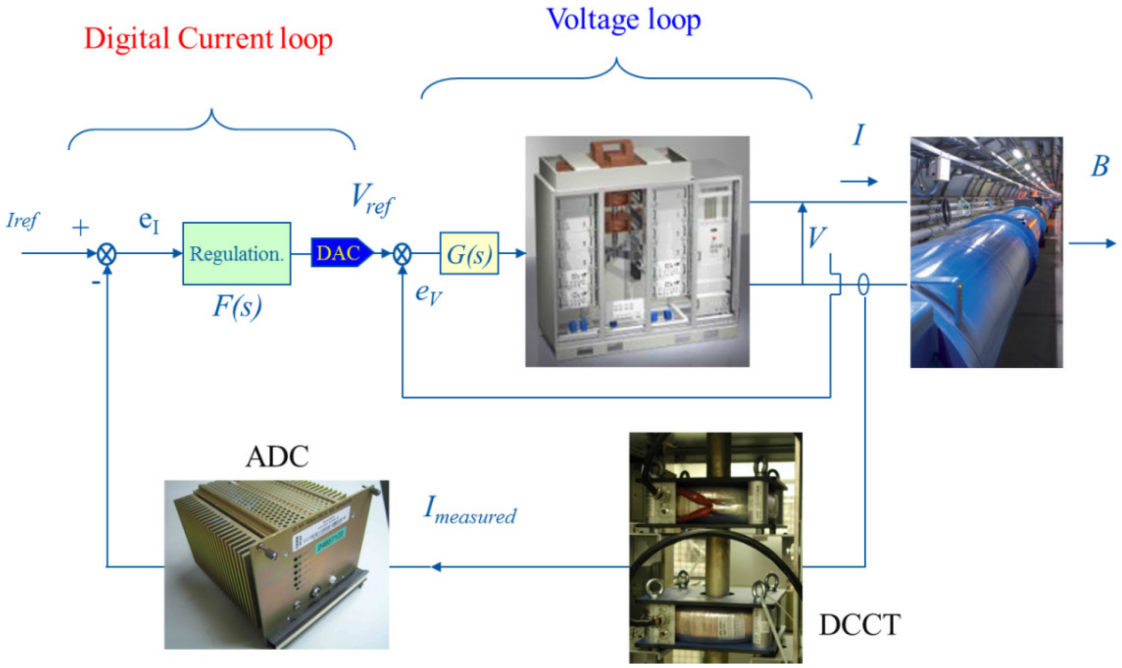


Fig. 18: Principle of power converter control

4.2 High precision

To get a high-precision power converter, a device capable of precisely measuring the output current is needed. The most popular current transducer is the DCCT (Direct-Current Current Transducer) for its high performance in many different fields, see Fig. 19. It is also classical to install two devices to be able to monitor any deviations of the currents between them [5].

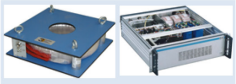
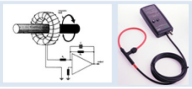
	DCCTs	Hall effect	CTs	Rogowsky	Shunts
					
Principle	Zero flux detection	Hall effect	Faraday's law	Faraday's law	Ohm's law
Output	Voltage or current	Voltage or current	Voltage	Voltage	Voltage
Accuracy	Best devices can reach a few ppm stability and repeatability	Best devices can reach 0.1%	Typically not better than 1%	Typically %, better possible with digital integrators	Can reach a few ppm for low currents, <% for high currents
Ranges	50A to 20kA	hundreds mA to tens of kA	50A to 20kA	high currents possible, up to 100kA	From <mA up to to several kA
Bandwidth	DC ..kHz for the higher currents, DC..100kHz for lower currents	DC up to couple hundred kHz	Typically 50Hz up to a few hudreds of kHz	Few Hz possible, up to the MHz	Up to some hundreds of kHz with coaxial assemblies
Isolation	Yes	Yes	Yes	Yes	No
Error sources	**Magnetic** (remanence, external fields, centering) **Burden resistor** (thermal settling, stability, linearity, tempco) **Output amplifier** (stability, noise, CMR, tempco)	**Magnetic** **Burden resistor** **Output amplifier** **Hall sensor stability** (tempco, piezoelectric effect)	**Magnetic** (remanence, external fields, centering, magnetizing current) **Burden resistor**	**Magnetic** **Integrator** (offset stability, linearity, tempco)	Power coefficient, tempco, ageing, thermal voltages

Fig. 19: Different types of current transducers

The performance of the power converter also strongly depends upon the current regulation control algorithm. The most powerful algorithm is the RST controller, which allows management of the tracking error as well as regulation, see Fig. 20 [6].

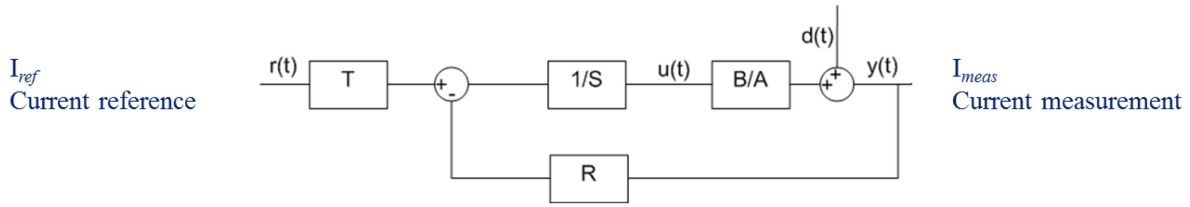


Fig. 20: RST controller

4.3 Power converter ripple

In principle, the voltage delivered by a power converter has a ripple that is due to semiconductor switching. The voltage ripple is generated by the power converter, and it is converted into a magnetic field ripple through the impedance of the magnet. The maximum magnetic field ripple has to be determined by the beam quality requirements, and then from the impedance of the magnet the maximum voltage ripple can be specified, see Fig. 21. The impedance of the vacuum chamber, between the current ripple and the magnetic field ripple, can also be taken into account. Typically, the vacuum chamber has a filtering effect above 100 Hz. The voltage ripple has to be specified for all frequencies, see Fig. 22.

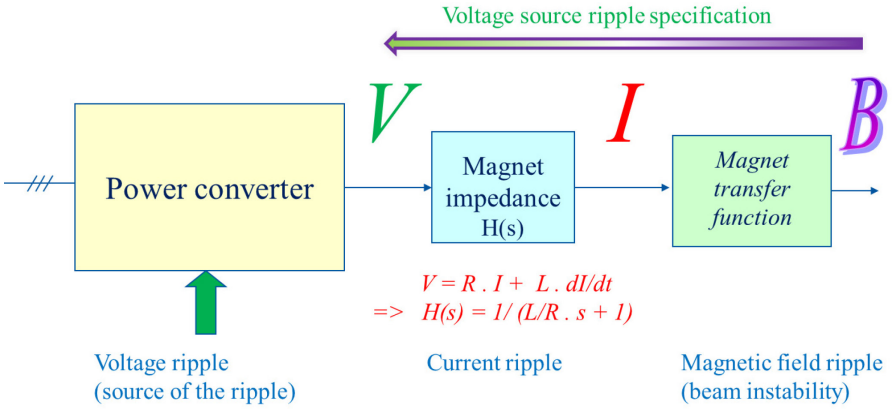


Fig. 21: Ripple chain

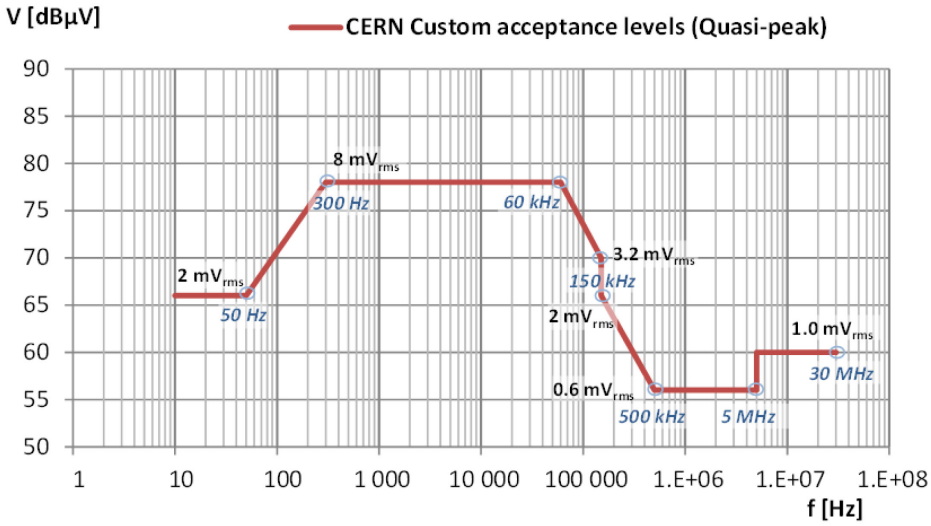


Fig. 22: Example of voltage ripple specification

4.4 Functional specification

Before starting the design of a new power converter, a functional specification needs to be approved between the accelerator physicists and the magnet designers. This functional specification includes:

- a short description of the machine;
- a description of the loads: magnet layout, magnet parameters, optimization with integral cost, and energy saving;
- a description of the operation duty cycle: machine cycles, minimum and maximum beam energy, ramp rates, hysteresis management, etc.;
- power converter requirements: power converter rating, current precision, current tracking, control system, energy management, lock-out and safety procedure, infrastructure (layout, electricity, cooling, handling, etc.);
- purchasing and development strategy;
- planning;
- budget;
- resources.

5 Introduction to the main challenges

The design of power converters covers a large range of disciplines. It needs more than one specialist to build it, it is a team work. The main challenges are listed below:

- power:
  - power converter topologies;
  - semiconductors, switching frequency, thermal design, fatigue while cycling…
  - filtering and electromagnetic compatibility (EMC);
  - connection to AC grid and robustness to grid perturbations;
  - energy management and energy saving;
  - protection and safety of the system;
- control:
  - accuracy class;
  - digitalization;
  - control loops;
  - timing and synchronization;
  - control interfaces;
  - interlocks with external systems.

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Definition of Power Converters

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Abstract
The paper is intended to introduce power conversion principles and to define common terms in the domain. The concepts of sources and switches are defined and classified. From the basic laws of source interconnections, a generic method of power converter synthesis is presented. Some examples illustrate this systematic method. Finally, the commutation cell and soft commutation are introduced and discussed.

Keywords
Power converter; power electronics; semiconductor switches; electrical sources; design rules; topologies.

1 Introduction

The task of a power converter is to process and control the flow of electrical energy by supplying voltages and currents in a form that is optimally suited for user loads.

Energy conversions were initially achieved using electromechanical converters (which were mainly rotating machines). Today, with the development and the massive production of power semiconductors, static power converters are used in numerous application domains and especially in particle accelerators. Their weight and volume are smaller and their static and dynamic performance are better.

A static converter is composed of a set of electrical components building a meshed network that acts as a linking, adapting, or transforming stage between two sources, generally between a generator and a load (Fig. 1).

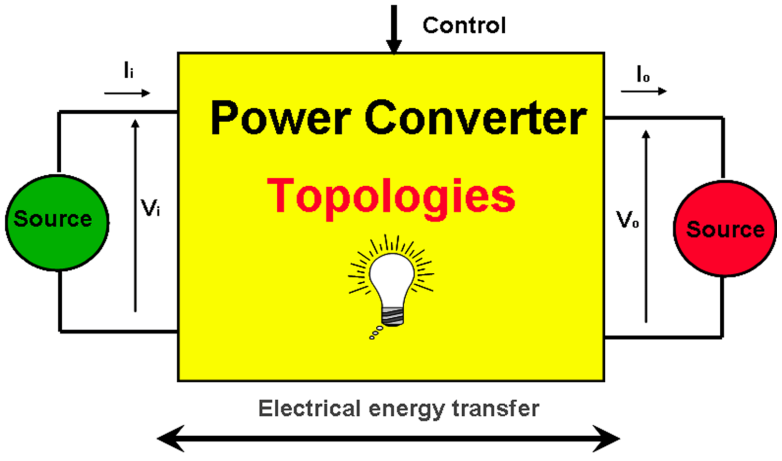

Fig. 1: Definition of a power converter

An ideal static converter allows control of the power flow between the two sources with 100% efficiency. A large part of power converter design is the optimization of its efficiency. But as a first approach and to define basic topologies, it is interesting to take the hypothesis that no losses occur

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through a power converter's conversion process. With this hypothesis, the basic elements are of two types:

- non-linear elements that are, most of the time, electronic switches: semiconductors used in commutation mode [1];
- linear reactive elements: capacitors, inductances (and mutual inductances or transformers). These reactive components are used for intermediate energy storage but also perform voltage and current filtering. They generally represent an important part of the size, weight and cost of the equipment [2, 3].

The objective of this introductory paper is to recall and give a precise definition of basic concepts essential for the design or understanding of power converter topologies [4]. First, a very simple example is presented to illustrate the basic principle of modern power electronics converters (switching power converter). Then the sources and the switches are defined, followed by the fundamental connection rules between these basic elements. From there, converter topologies are deduced. Some examples of topology synthesis are then given. Finally, the concept of hard and soft commutation is introduced.

2 The very basic principles of modern power electronics conversion

As a first basic example to illustrate the evolution toward modern power electronics, let us consider a DC to DC converter that aims to deliver 100 V to a resistive load of 10 Ω. The input voltage source delivers a constant 325 V. Until the 1960s, and still in use in some special applications, a typical utilization of transistors consisted of operating them in their linear, or active, region. The basic 'old' topology for this case is illustrated in Fig. 2. This consists of operating the transistor such that a 225 V voltage drop across it is ensured. Simplifying, one can say that in this case the transistor is used as a controllable resistance.

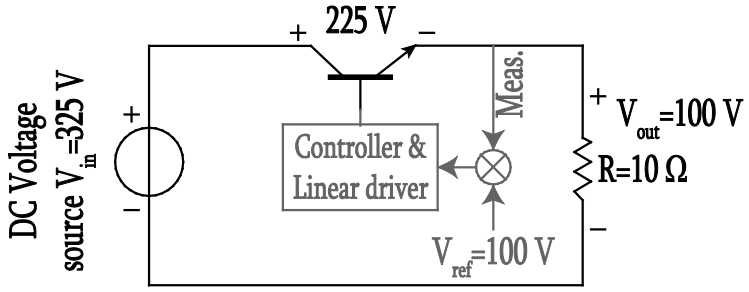


Fig. 2: DC to DC converter using the transistor's linear, or active, region

Analysing this circuit at this operating point, one can derive the input and the delivered output powers P_{in} and P_{out}, the losses in the transistor P_{T}, and the converter efficiency η, as presented in Eq. (1),

$$P_{\text{in}} = 325\ \text{V} \times 10\ \text{A} = 3.25\ \text{kW}\,, \tag{1}$$

$$P_{\text{out}} = 100\ \text{V} \times 10\ \text{A} = 1\ \text{kW}\,, \tag{2}$$

$$P_{\text{T}} = P_{\text{in}} - P_{\text{out}} = 2.25\ \text{kW}\,, \tag{3}$$

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = 0.3 \equiv 30\%\,. \tag{4}$$

Notice that for this particular operating point the efficiency is extremely low. In the general case, the efficiency can be expressed as in Eq. (5), where the efficiency drastically decreases as V_{out} decreases,

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{V_{\text{out}}^2/R}{(V_{\text{in}} \cdot V_{\text{out}})/R} = \frac{V_{\text{out}}}{V_{\text{in}}}\,. \tag{5}$$

This conversion system produces high losses and needs an over-dimensioned transistor able to dissipate the losses. Furthermore, the overall dimensions of this power converter shall be large enough

for being able of evacuating the high losses for a given maximum temperature. This conversion method is still used in some special applications where high precision or high dynamics is required [5].

The basic principle of modern power electronics lies in the utilization of switches in their ON and OFF states only, virtually producing no, or very low, losses (losses in switches are described in Section 4.2, Dynamic characteristics). The basic principle is illustrated in Fig. 3. Between the voltage source V_{in} and the load R, the converter is now composed of a 'special' two-position switch and a low-pass filter. When the switch is in position 1, the input voltage V_{in} appears at the low-pass filter input V_s. When the switch is in position 2, zero volts are applied to V_s. Given a pattern in time of the switch positions, one derives the pattern of the voltage V_s (chopped or switched voltage). In most applications, the voltage V_s, with a fluctuation of 100% (from 0 V to V_{in}), cannot be directly applied to the load, therefore a filtering action must be undertaken in order to apply the voltage V_s average values to the load, which is derived in Eq. (6),

$$V_{\text{out}} = \frac{1}{T_s}\int_0^{T_s} v_{in}(t)\mathrm{d}t = DV_{\text{in}}\,, \tag{6}$$

where T_s is the switching period (which defines the switching frequency f_s), and D is the duty cycle, or duty ratio, which defines the relative time when the switch is in position 1 with respect to the switching period T_s (illustrative definitions are given in Fig. 3). In this case, the regulation of the output voltage is performed by acting on the duty cycle D.

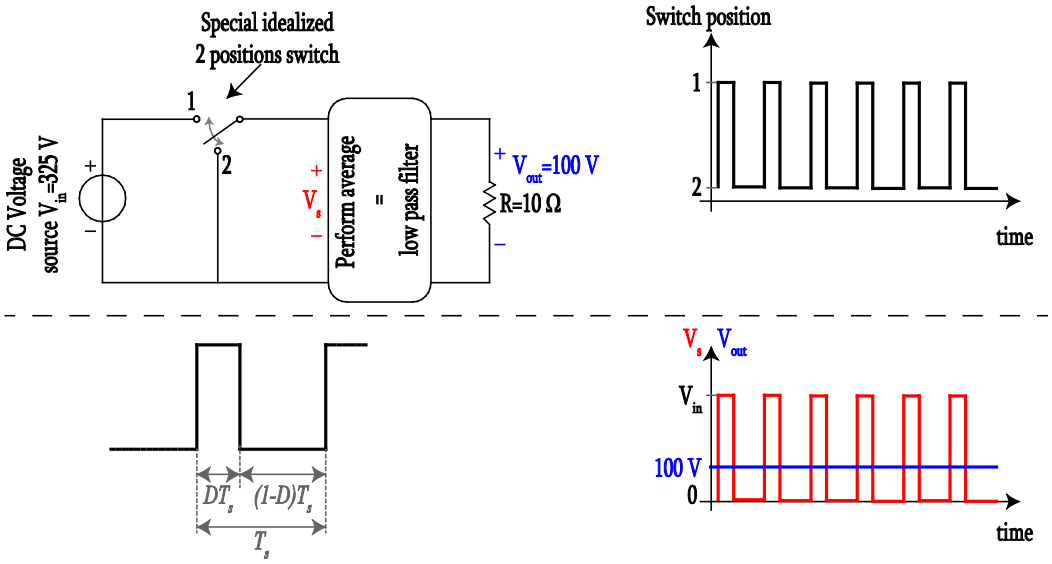


Fig. 3: Idealized switch-mode DC-to-DC converter principle

Thanks to the low losses, modern switch-mode power converters are more efficient and compact. However several new aspects have to be considered during the design phase. A filtering process is required, leading to the introduction of the so-called output voltage and current ripples on the load and voltage, or current, bandwidths. A non-ideal filter is always letting some harmonics pass through the load. Furthermore, the dynamic characteristics of the power converter (rate of change of current and/or voltage) is limited by the filter. This trade-off between ripple and bandwidth is a key aspect in the design and specification process of modern switch-mode power converters.

3 Sources

As mentioned in the introduction, a power converter processes the flow of energy between two sources. To synthesise a power converter topology, the first step is to characterize these sources. We will see later that the converter structure can be directly deduced as soon as the sources are defined: voltage or current sources and their reversibilities.

In the energy conversion process, a source is usually a generator (often called an input source) or a load (often called an output source). However, in the case of a change of direction of the energy flow, i.e. a change in the sign of the power, the sources (generators and loads) can exchange their functions (i.e. restoration of energy from a magnet back to the grid).

3.1 Nature of sources

3.1.1 Definitions

Two types of sources could be defined: voltage and current sources. As mentioned, any of these sources could be a generator or a receiver (load).

A source is called a *voltage* source if it is able to impose a voltage independently of the current flowing through it. This implies that the series impedance of the source is zero (or negligible in comparison with the load impedance)

A source is called a *current* source if it is able to impose a current independently of the voltage at its terminals. This implies that the series impedance of the source is infinite (or very large in comparison with the load impedance).

These definitions correspond to permanent properties. The principle of operation of a converter is based on the switch-mode action of its switches. Commutation of the switches generates very fast current and/or voltage transients so that the transient behaviour of the sources is of fundamental importance for the converter design. The transient behaviour of a source is characterized by its ability or inability to withstand steps in the voltage across its terminal or in the current flowing through it, these steps being generated by the external circuit. Then new definitions could be stated as below.

- A source is a *voltage source* if the voltage across its terminals cannot undergo a discontinuity due to the external circuit variation. The most representative example is a capacitor, since an instantaneous change of voltage would correspond to an instantaneous change of its charge that would require an infinite current (Fig. 4(b)).
- A source is a *current source* if the current flowing through it cannot undergo a discontinuity due to the external circuit variation. The most representative example is an inductor, since an instantaneous change in current would correspond to an instantaneous change in its flux that would require an infinite voltage (Fig. 4(a)).

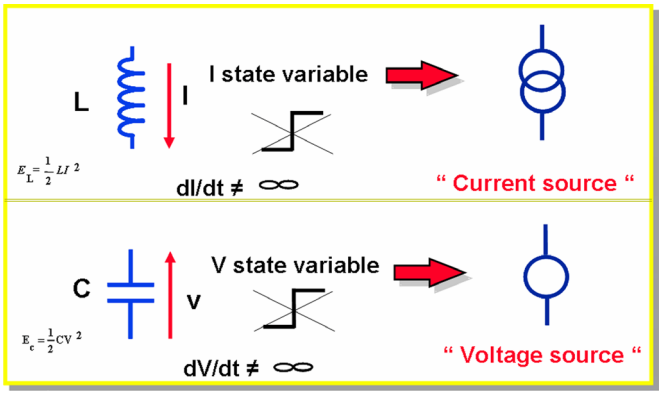


Fig. 4: Inductance and capacitor vs. current and voltage source

It should be noted that a square wave voltage generator is indeed a voltage source as defined above since the voltage steps are not caused by the external circuit. A square wave current generator is indeed a current source as defined above since the current steps are not caused by the external circuit.

With these definitions, it is interesting to define the notion of instantaneous impedance of a source as the limit of the source impedance when the Laplace operator tends towards infinity. Theoretically this instantaneous impedance can be zero, finite, or infinite.

A source is referred to as a voltage source when its instantaneous impedance is zero, while a source is called a current source if its instantaneous impedance is infinite.

For example:

Capacitor: $Z(s) = 1/(C.s)$, $\lim_{s \to \infty}$ $Z(s) = 0$, this leads to a voltage source;

Inductance: $Z(s) = L.s$, $\lim_{s \to 0}$ $Z(s) = \infty$, this leads to a current source.

3.1.2 Source reversibility

The determination of the source reversibilities is fundamental. We will see that the reversibility analysis allows the deduction of the static characteristics of the switches.

The voltage (or the current) that characterizes a source is termed DC if it is unidirectional. As a first approximation, it can be taken as being constant. The voltage (or the current) is termed AC if it is periodic and has an average value equal to zero. As a first approximation, it can be taken as sinusoidal.

A source is voltage-reversible if the voltage across its terminals can change sign. In the same way, a source is current-reversible if the current flowing through it can reverse.

In summary, the input/output of a converter can be characterized as voltage or current sources (generator or loads), either DC or AC, current-reversible and/or voltage-reversible. In total, there are only eight possibilities, shown in Fig. 5.

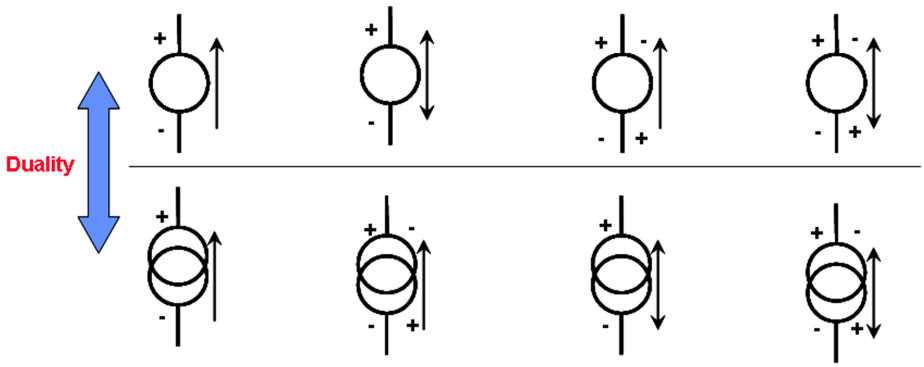


Fig. 5: Voltage and current sources with their reversibilities

3.1.3 Source nature modification

Connection of a series inductance with an appropriate value to a voltage source (i.e. a dipole with zero instantaneous impedance) turns the voltage source into a current source. In the same way, connecting a parallel capacitor of appropriate value to a current source (a dipole with infinite instantaneous impedance) turns the current source into a voltage source (Fig. 6).

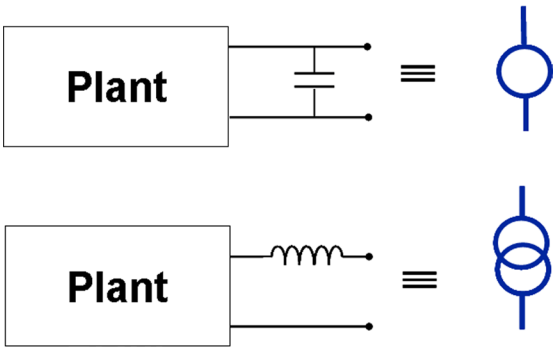


Fig. 6: Source nature confirmation or modification

These inductive or capacitive elements connected in parallel or in series with the source are elements that can temporarily store energy. Consequently, if an inductance connected to a voltage source turns it into a current source it is important to determine the current reversibility of this current source.

In practice the identification of a real generator or of a real load as a voltage or current source is not obvious. That is the reason why the nature of the source is often reinforced by the addition of a parallel capacitor in the case of voltage sources and by the addition of a series inductor in the case of current sources.

Obviously, the current source obtained by connecting an inductance in series with a voltage source keeps the same current reversibility as this voltage source. The inductance acts as a buffer absorbing the voltage differences. Consequently the current source obtained by connecting a series inductance to a voltage source is reversible in voltage. When the voltage source itself is reversible in voltage there is no particular problem. But, if the voltage source is not reversible in voltage, the current source obtained by connecting a series inductance to the voltage source is only instantaneously reversible with respect to voltage.

The former result can easily be transposed to the voltage source obtained by the parallel connection of a capacitor to a current source. The voltage source obtained keeps the same voltage reversibility as the current source and is reversible in current. However, this reversibility is only instantaneous if the current source is not reversible in current.

3.1.4 Example

A set of ideal batteries behaves as a load during charging and as a generator during discharging; such a source is called a DC voltage source, being current reversible but not voltage reversible. Nevertheless, because of the inductance of the connecting cables, this battery can sometimes be taken as a current source that is instantaneously voltage reversible and permanently current reversible. If a capacitor bank is added at the terminals of the cables, it again becomes a voltage source (Fig. 7).

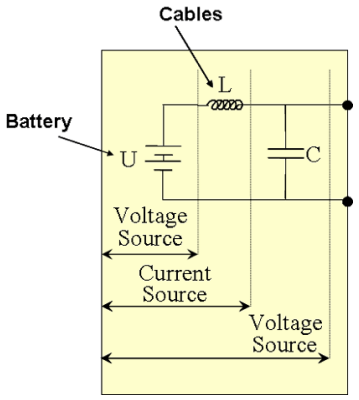


Fig. 7: Modification to voltage or current source

4 Switch characteristics

Static converters are electrical networks mainly composed of semiconductor devices operating in switch mode (as switches). Through proper sequential operation of these components, they allow an energy transfer between two sources with different electrical properties.

The losses in the switches should be minimized in order to maximize the efficiency of the converter. Switches must have a voltage drop (or an ON resistance) as low as possible in the ON state, and a negligible leakage current (or an OFF resistance) in the OFF state. These two states are defined as static states.

The change from one state to the other state (switch commutation) implies transient behaviour of the switch. These behaviours are complex because they depend on the control of the switch (through a gate control) and on the conditions imposed by the external circuit.

4.1 Static characteristics

In the static domain a switch has the same behaviour as a non-linear resistance: very low in the ON state and very high in the OFF state.

Taken as a dipole with the load sign convention (Fig. 8) the static characteristic $I_k(V_k)$, which represents the operating points of a switch, is made up of two branches totally located in quadrants 1 and 3 such that $(V_k \times I_k) > 0$. One of these branches is very close to the I_k axis (ON state) and the other is very close to the V_k axis (OFF state). Each of these branches can be located in one or two quadrants. In the case of an ideal switch, the static characteristics are the half-axis to which they are close.

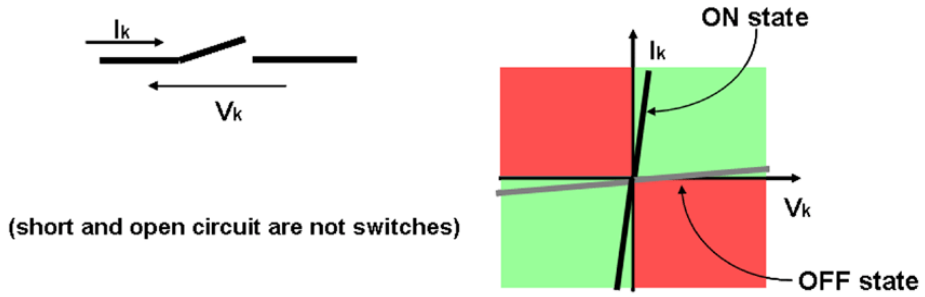


Fig. 8: Static characteristics of a switch

In this representation, except for the obvious cases of a short circuit and of an open circuit that correspond respectively to a switch always ON and to a switch always OFF, any switch that really behaves as a switch (commutation: ON <=> OFF) has a static characteristic consisting of at least two orthogonal half-axes (or segments).

The static characteristic, an intrinsic feature of a switch, reduces to a certain number of segments in the $I_k(V_k)$ plane.

– Two-segment characteristics: the switch is unidirectional in current and in voltage. Two two-segment characteristics can be distinguished: in the first case, current I_k and voltage V_k have the same signs; in the second case, current I_k and voltage V_k have opposite signs. The switches having such characteristics are respectively called T and D switches (Fig. 9).

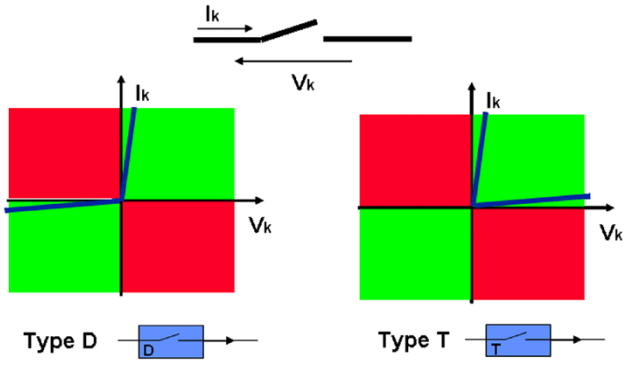


Fig. 9: Static characteristics of a two-segment switch

– Three-segment characteristics: the switch is bidirectional either in current or in voltage while the other is unidirectional. Therefore, there are two types of three-segment static characteristics (Fig. 10). It should be noted that these two types of switches could be synthesized with the association in parallel or in series of two-segment switches (T and D).

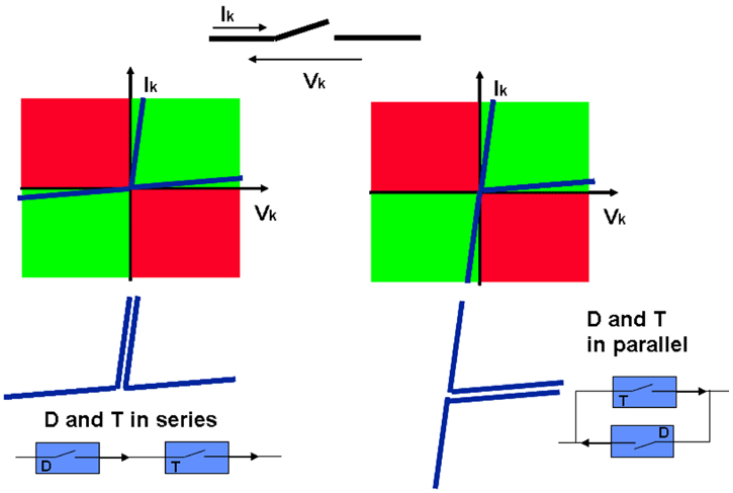


Fig. 10: Static characteristics of a three-segment switch

– Four-segment characteristics: the switch is bidirectional in voltage and in current. There is only one such type of static characteristic (Fig. 11). A four-segment characteristic could be obtained by series or parallel connection of switches with three-segment characteristics.

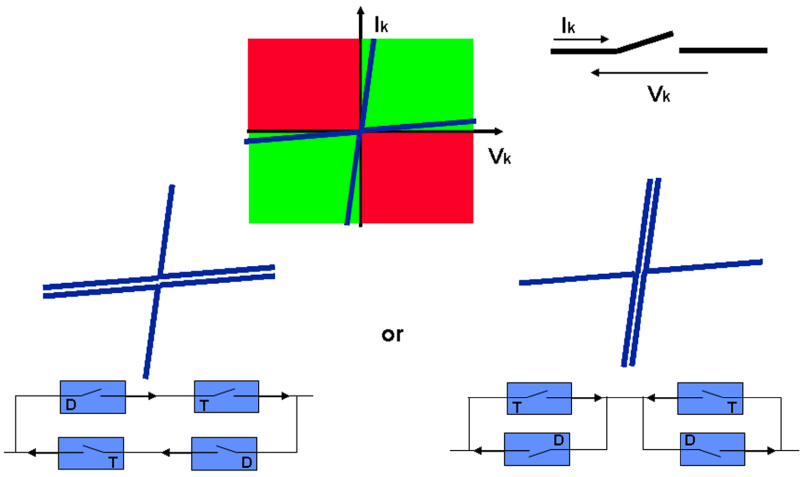


Fig. 11: Static characteristics of a four-segment switch

4.2 Dynamic characteristics

The dynamic characteristic is the trajectory described by the point of operation of the switch during its commutation, to go from one half-axis to the perpendicular half-axis. A switch being either ON or OFF, there are two commutation dynamic characteristics corresponding to the turn-ON and the turn-OFF, which will be grouped under the global term dynamic characteristics.

Unlike the static characteristic, the dynamic characteristic is not an intrinsic property of the switch but also depends on the constraints imposed by the external circuit. Neglecting second-order phenomena, and taking into account the dissipative nature of the switch, the dynamic characteristic can only be located in those quadrants where $V_k \times I_k > 0$ (generator quadrants). For the two commutations (turn-ON and turn-OFF), two modes are possible: controlled commutation and spontaneous commutation.

4.2.1 Controlled commutation

The switch has, in addition to its two main terminals, a control terminal on which it is possible to act in order to provoke a quasi-instantaneous change of state (in the case of a T switch). The internal resistance

of this switch can change from a very low value to a very high value at turn-OFF (and inversely at turn-ON). These changes are independent of the evolution of the electrical quantities imposed on the switch by the external circuit.

It should be noted that, in a controlled commutation, the switch imposes its state on the external circuit. Under such circumstances, the element can undergo severe stresses that depend on its dynamic characteristic. If the switching time is long and the operating frequency is high, the commutation losses can be important.

4.2.2 Spontaneous commutation

The spontaneous commutations correspond to turn-OFF when the current flowing through the switch arrives at zero and to turn-ON when the voltage applied across its terminals reaches zero. Spontaneous commutation is the commutation of a simple PN junction (D switch). It is only dependent on the evolution of the electrical variables in the external circuit. Spontaneous commutations could be achieved with any controlled semiconductor if the gate control is synchronized with the electrical quantities of the external circuit. Spontaneous commutation is achieved with minimal losses since the operating point moves along the axes.

It is important to point out that controlled commutation can only happen in the first or third quadrants while spontaneous commutation can only happen with a change of quadrant (Fig. 12).

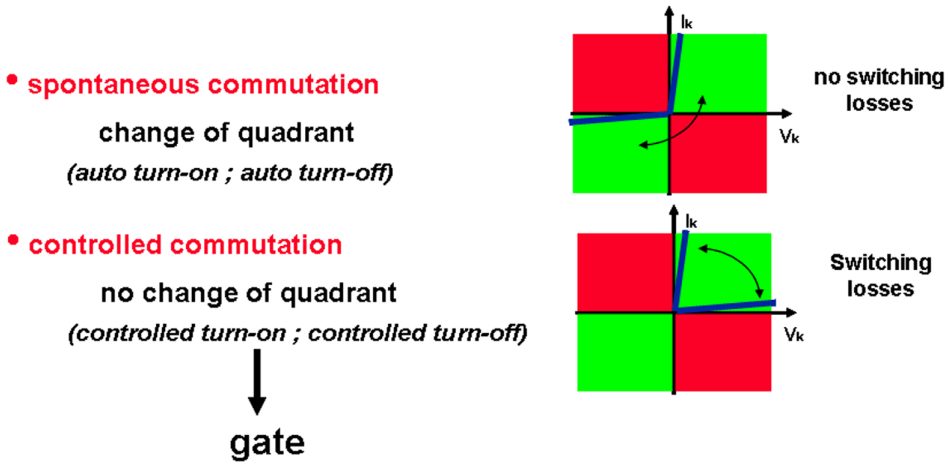


Fig. 12: Spontaneous and controlled commutations

4.3 Classification of switches

Finally, switches used in power converter can be classified by their static characteristics (two, three or four segments) and by the type of commutation (controlled or spontaneous) at turn-ON and at turn-OFF.

4.3.1 Two-segment switches

Except the open circuit and the short circuit, two switches with two-segment characteristics can be distinguished (Fig. 13).

- The first of these switches has the static characteristics of switch D, and its turn-ON and turn-OFF commutations are spontaneous. This switch is typically a diode.
- The second of these switches has the static characteristics of switch T and its turn-ON and turn-OFF commutations are controlled. Examples are the power semiconductors: metal-oxide semiconductior field-effect transistors (MOSFET), insulated-gate bipolar transistor (IGBT), gate tunr-off thyristor (GTO), integrated-gate commutated thyristor (IGCT), etc.

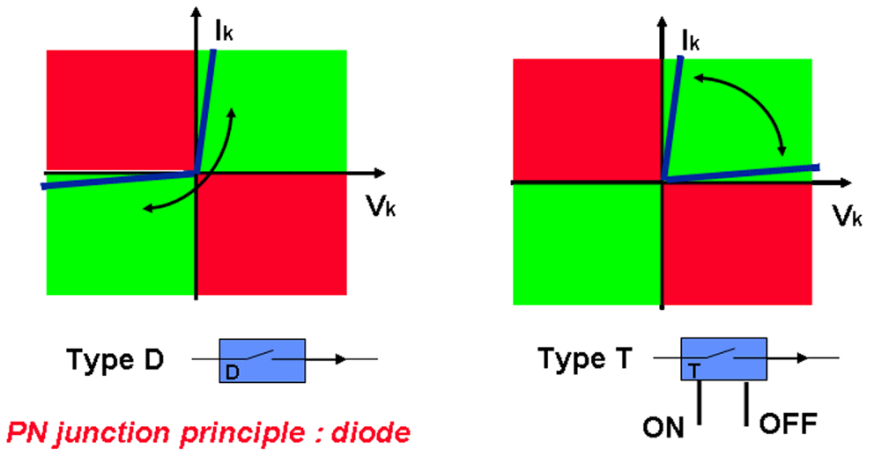


Fig.13: Dynamic characteristics of two-segment switches

This switch will be symbolized by separating the turn-ON and turn-OFF control gate as shown in Fig. 13.

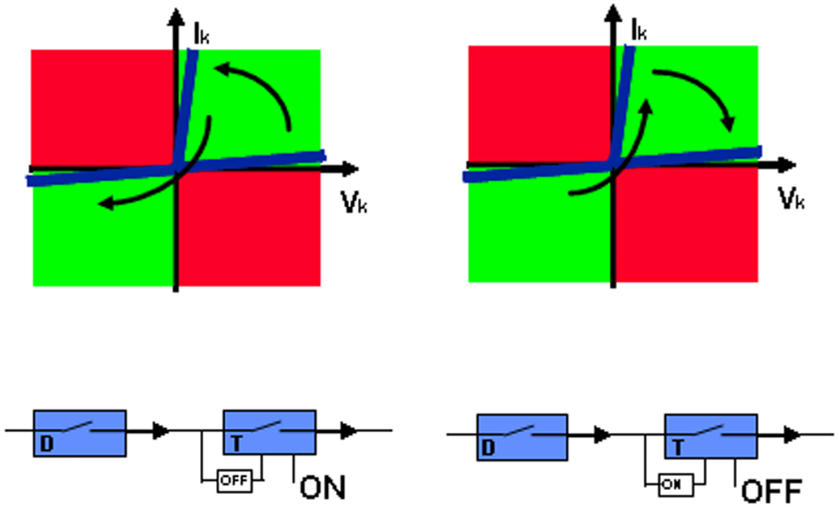
A switch with two-segment characteristics similar to the T type (both segments in the same quadrant), must have controlled turn-ON and turn-OFF commutations. If it would have only one controlled commutation, it would be necessary to put in series or in parallel a switch D (a diode) to get the spontaneous commutation. In this case, it is no longer a two-segment switch, but a three-segment one. Therefore, only two two-segment switches can be used directly.

4.3.2 Three-segment switches

These switches can be divided into two groups depending whether they are:

– unidirectional in current and bidirectional in voltage (Fig. 14);

– bidirectional in current and unidirectional in voltage (Fig. 15).



Fig, 14: Dynamic characteristics of three-segment switches: bidirectional in voltage

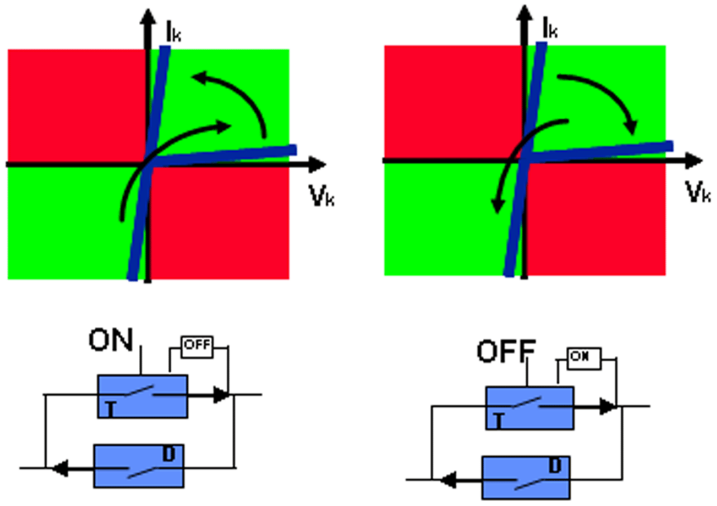


Fig. 15: Dynamic characteristics of three-segment switches: bidirectional in current

Except for the thyristor, all these switches are synthesized switches, realized by connecting a diode in parallel or in series with a two-segment switch. A special driver is needed to obtain spontaneous commutation. The 'dual-thyristor' (unidirectional in voltage, bidirectional in current, controlled turn-OFF and spontaneous turn-ON) is a good example of a useful three-segment switch [6, 7].

In each of these two groups, all switches have the same static characteristics but differ with their commutation mechanisms. It is important to remark that if a three-segment switch has both commutations controlled (turn-ON and turn-OFF) or both spontaneous, it would never use the three segments of its static characteristic. Therefore, a three-segment switch must necessarily have one controlled commutation and one spontaneous commutation.

The cycle of operation, which represents the locus described by the point of operation of these switches, is then fully determined. They can only be used in converter topologies that impose a single cycle on the switches during operation.

4.3.3 Four-segment switches

All four-segment switches have the same static characteristic. They differ only by their commutation modes that can, a priori, differ in quadrants 1 and 3. So, six four-segment switches can be distinguished.

These switches are used mainly in direct frequency changers and in matrix converters; in practice they are made up of two three-segment switches connected in series or parallel.

5 Interconnection of sources: Commutation rules

To control the power flow between two sources, the operation principle of a static power converter is based on the control of switches (turn-ON and turn-OFF) with determined cycles creating periodic modifications of the interconnection between these two sources.

The source interconnection laws can be expressed in a very simple way:

- a voltage source should never be short-circuited but it can be open-circuited;
- a current source should never be open-circuited but it can be short-circuited.

From these two general laws, it can be deduced that switches cannot establish a direct connection between two voltage sources or between two current sources.

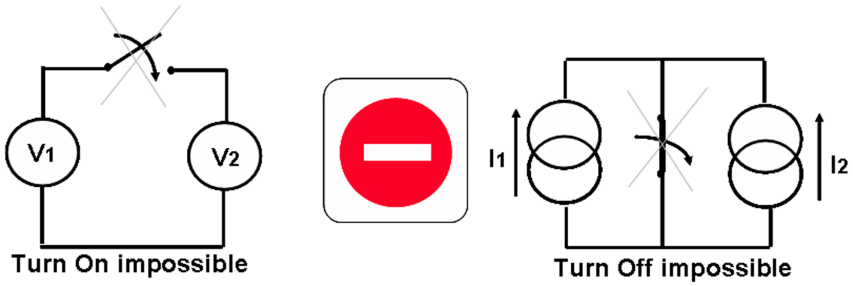


Fig. 16: Basic interdictions of source interconnection

In the case of two voltage sources, the switch turn-ON can only happen when the two sources have the same values, that is to say at the zero crossing of the voltage across the switch. The turn-ON must then be spontaneous (since it depends on the external circuit) and turn-OFF can be controlled at any time. In the case of two current sources, the switch turn-OFF can only happen when the two current sources reach the same value, that is to say when the current in the switch reaches zero. In this case, the turn-OFF is spontaneous and turn-ON can be controlled at any time.

As it is done in day-to-day practise and following the previous arguments, it is obvious that it is possible to put capacitors in parallel and inductances in series but these elements should be connected with zero voltage or zero current, respectively.

From the laws state above, it is easy to deduce that the commutation of switches must not interconnect two sources of the same nature.

6 Structure of power converters

A power converter can be designed with different topologies and with one or several intermediate conversion stages. When this conversion is achieved without any intermediate stage temporarily storing some energy, the conversion is called direct conversion and it is achieved by a direct converter. On the other hand, when this conversion makes use of one or more stages able to store energy temporarily, the conversion is termed indirect and it is achieved by an indirect converter.

The interdiction to connect two sources of the same nature leads to the consideration of two classes of basic conversion topologies:

- direct link topology: when the two sources have different natures;
- indirect link topology: when the two sources have the same nature.

6.1 Direct link topology converters

A direct converter is an electrical network composed only of switches and is unable to store energy. In such a converter, the energy is directly transferred from the input to the output (with the hypothesis that the losses can be neglected); the input power is at any time equal to the output power.

Taking into account the interconnection rules recalled above, the different possible connections between a voltage source and a current source are shown in Fig. 17. To get all these connections, the simplest structure is the four-switches bridge (Fig. 18):

- with K1 and K3 closed, the connection shown in Fig. 17(a) is obtained;
- with K2 and K4 closed, the connection shown in Fig. 17(b) is obtained;
- with K1 and K2 closed (or with K3 and K4 closed), the connection shown in Fig. 17(c) is obtained.

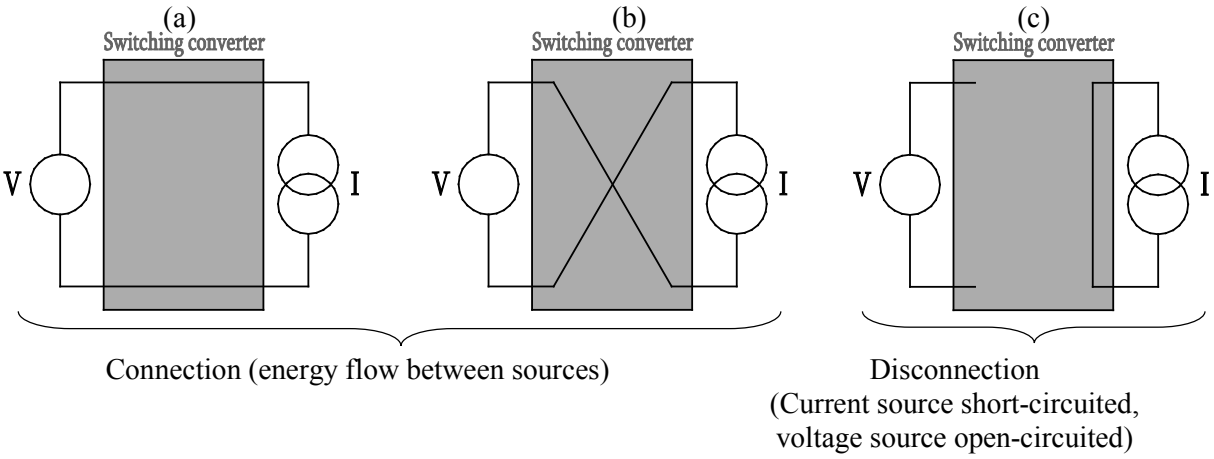


Fig. 17: Interconnection possibilities between a voltage and a current source. (a) – direct connection; (b) – inverse connection; (c) - disconnection with current source in short-circuit.

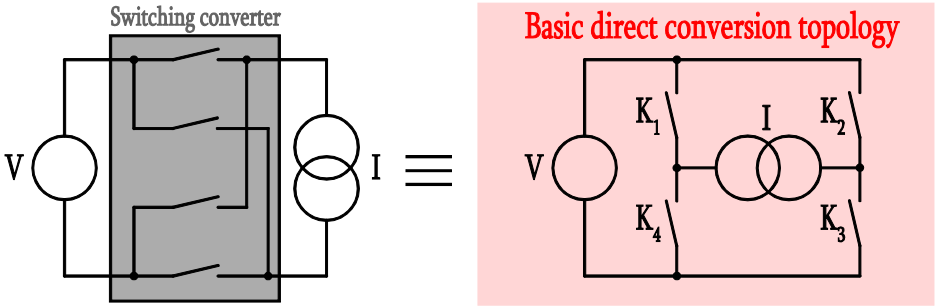


Fig. 18: Basic configuration of voltage–current direct converter

When some of these connections are not necessary, it is possible to simplify the bridge structure into structures using fewer switches (i.e. a buck converter).

Energy conversion between an input current source and an output voltage source is the same problem. The basic configuration is the same but it is more usual to represent the input source on the left and the output source on the right (Fig. 19).

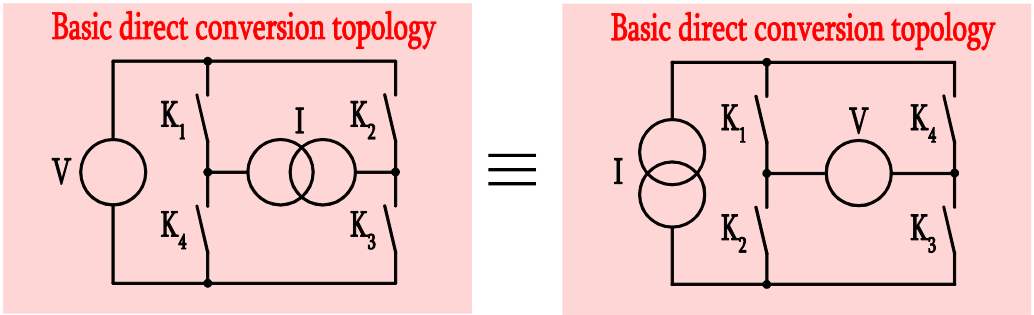


Fig. 19: Basic configuration of current–voltage direct converter

6.2 Indirect converters

If both sources have the same nature, it is not possible to interconnect them directly with switches. It is necessary to add components to generate an intermediate buffer stage of a different type without active energy consumption (capacitor or inductor). This buffer stage is a voltage source (capacitor) if the energy transfer is between two current sources, and it is a current source (inductance) if the energy transfer is between two voltage sources.

6.2.1 Modification of the nature of the input or output source

In the case of voltage–voltage conversion, one solution could be to add an inductance in series with the input voltage source or with the output voltage source. With this change of the source nature, it is possible to use a direct converter: a current–voltage or voltage–current converter according to where the inductance was added (Fig. 20).

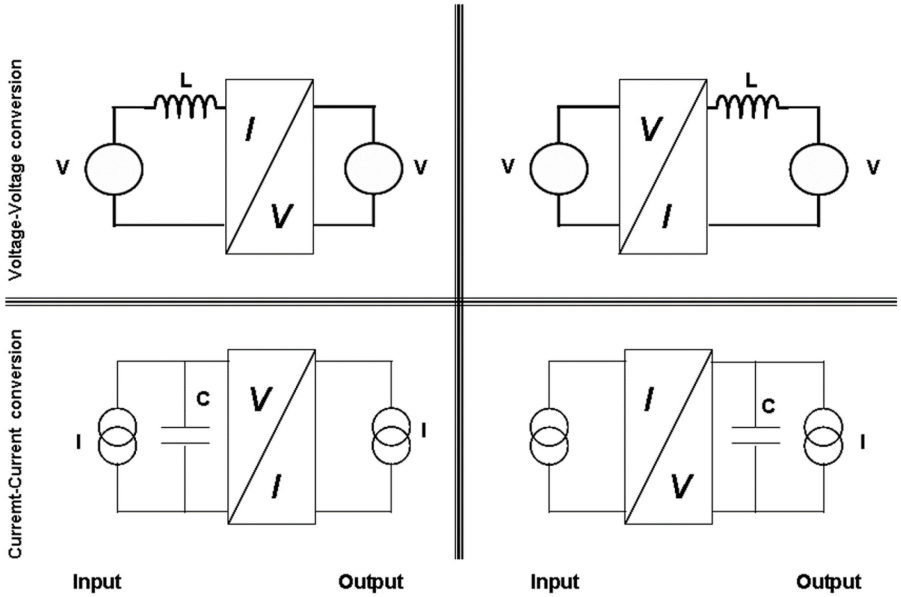


Fig. 20: Indirect converters: modification of the nature of the input or output source. Above one of the voltage sources need to be modified into a current source. Below one of the current sources need to be modified into a voltage source.

The case of current–current conversion is similar to the previous case. Therefore, a capacitor should be added in parallel or in series with the input current source or with the output current source.

6.2.2 Use of two direct converters

If it is not possible or too costly to modify the nature of one source, two direct converters can be connected with an intermediate buffer stage: an inductance for a voltage–voltage conversion and a capacitor for a current–current conversion (Fig. 21).

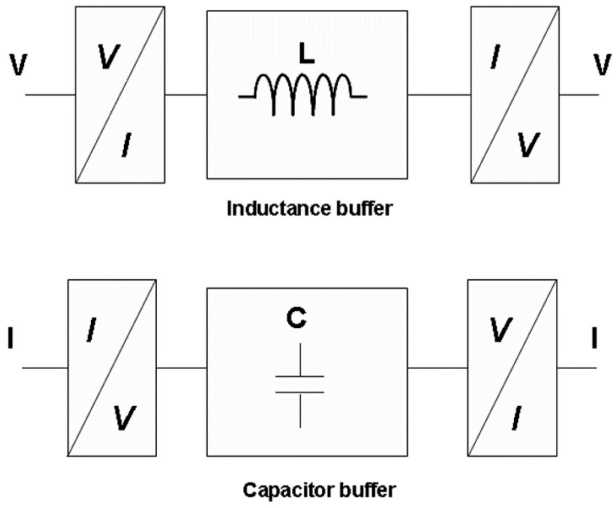


Fig. 21: Indirect converters: intermediate buffer stage, inductive above and capacitive below, between two direct converters.

6.2.3 Voltage–voltage indirect converters

In indirect converters, the two voltage sources are never connected directly (see the basic laws described above). Two sequences are therefore necessary. During the first sequence, the energy is transferred from the input voltage source to the inductance (voltage to current conversion). During the second sequence, the inductance gives back the energy to the output voltage source (current to voltage conversion; two directions are possible) (Fig. 22). An extra switch is necessary to obtain these sequences.

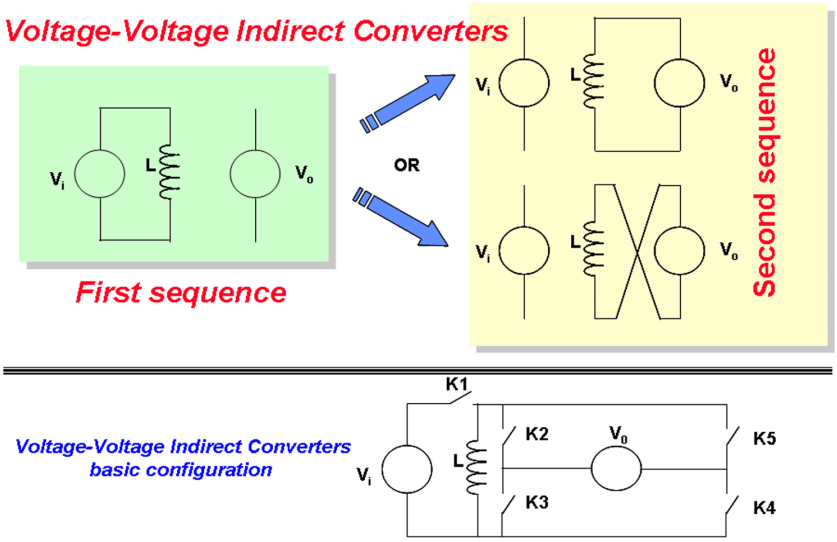


Fig. 22: Voltage–voltage indirect converters. Above the three possible connections between first and second sequences. Below the corresponding topology.

6.2.4 Current–current indirect converters

In the indirect converters, the two current sources are never connected directly. Then, two sequences are necessary. During the first sequence, the energy is transferred from the input current source to the capacitor (current to voltage conversion). During the second sequence, the capacitor gives back the energy to the output current source (voltage to current conversion; two directions are possible) (Fig. 23).

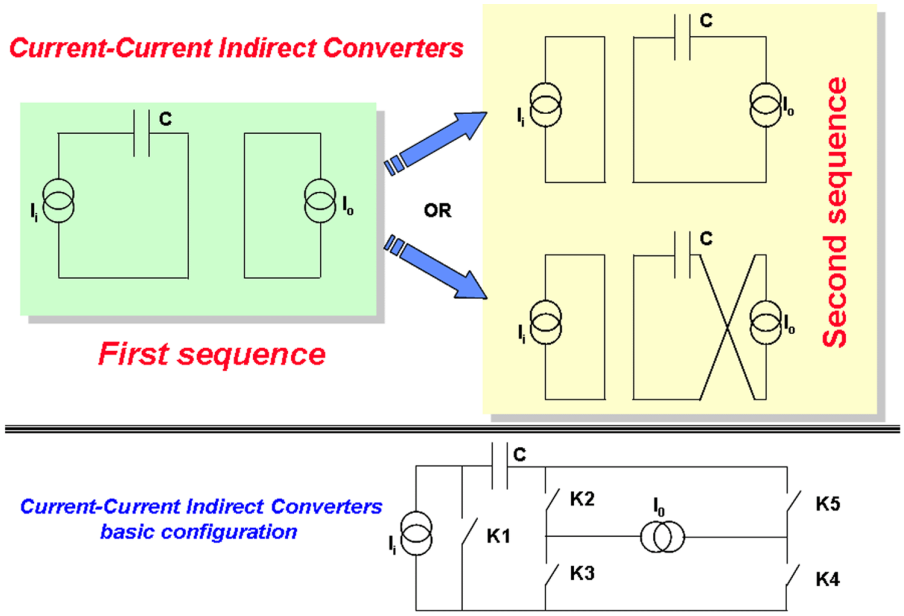


Fig. 23: Current–current indirect converters. Above the three possible connections between first and second sequences. Below the corresponding topology.

6.3 Conclusions

Figure 24 represents the three basic configurations of all single-phase converters.

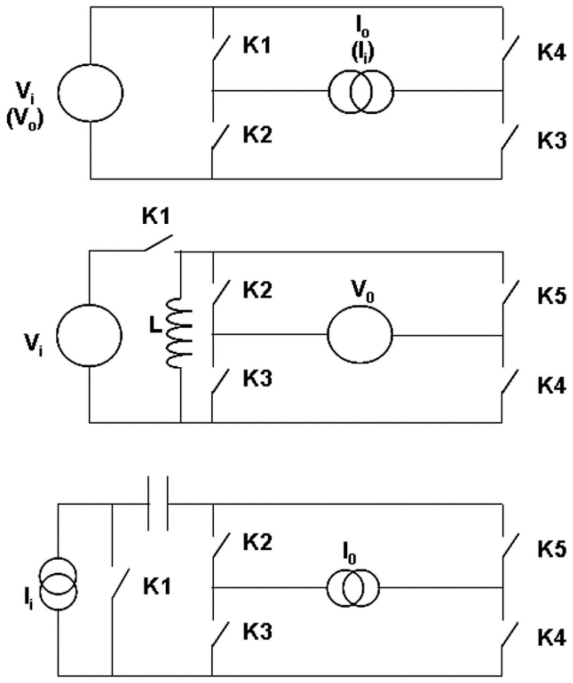


Fig. 24: Three basic structures of single-phase power converters. Voltage to current (and vice-versa) direct conversion (above), voltage to voltage indirect conversion (in the middle), and current to current indirect conversion (below).

From these basic configurations, it is possible, according to the nature of the sources, to associate them or to add other components. For example, in the case where one of the sources is AC, it is possible to insert a transformer for adaptation or galvanic insulation (Fig. 25).

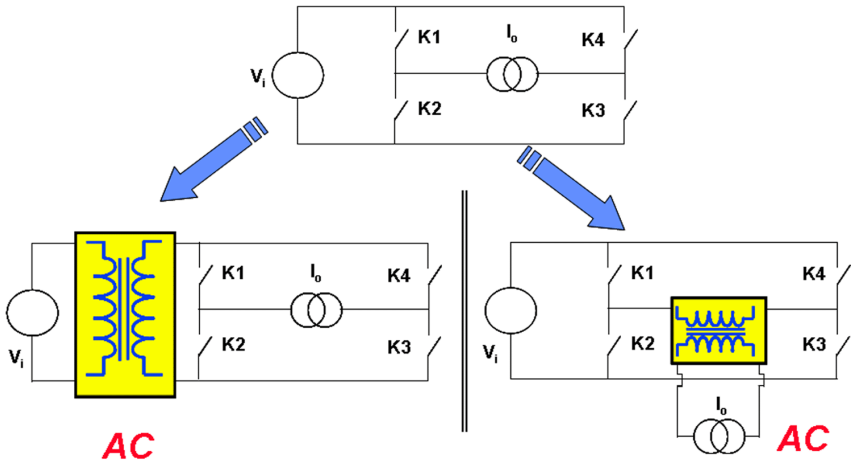


Fig. 25: Insertion of a transformer in a direct topology

It is also possible to associate several basic topologies. One application that is more frequently used is to have an intermediate stage operating at a high frequency to reduce the size of the transformers and magnetic elements and to get higher performance at the output (bandwidth, ripple, etc.) (Fig. 26). Details of magnetic component design are given in Ref. [3].

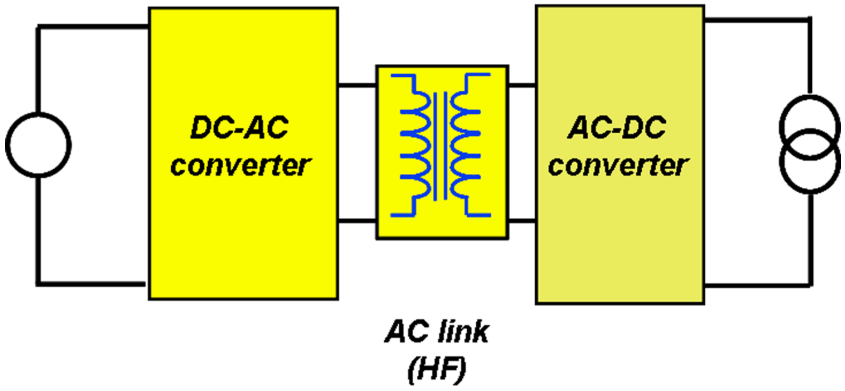


Fig. 26: Association of elementary structures

Figure 27 illustrates the case of resonant converters [8, 9]. It should be noted that the interconnection of the various intermediate sources must respect the interconnection laws. It is especially important for the choice of the output filter.

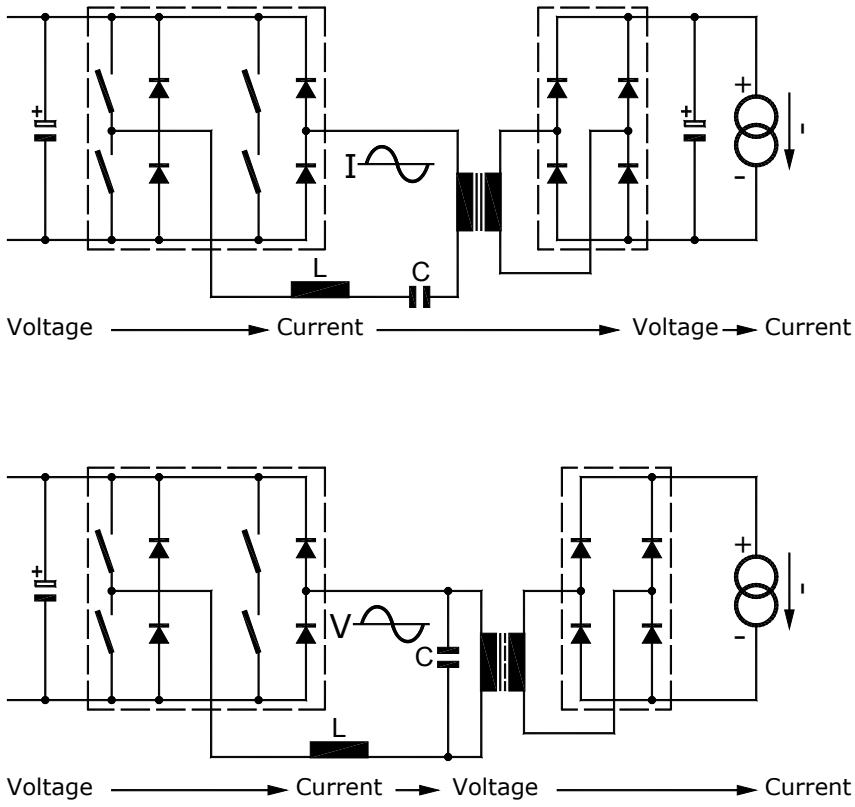


Fig. 27: Series (above) and parallel (below) resonant converters

7 Power converter classification

Figure 28 is a table summarizing the power conversion topologies. The crossed cells correspond to reversibility incompatibilities between the input and output sources. Two symmetric cells, with respect to the diagonal line D, represent two reversible topologies. Two topologies corresponding to two cells symmetric with respect to the point O are dual.

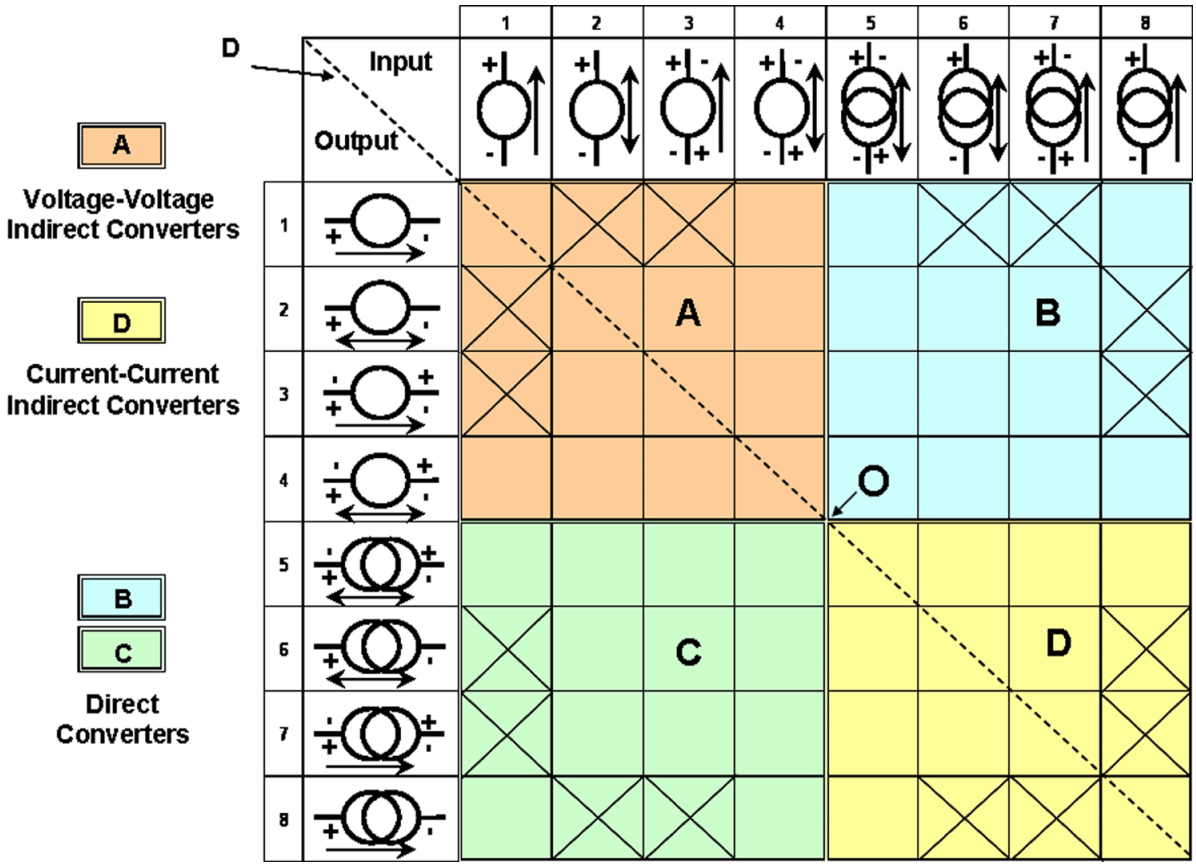


Fig. 28: General power conversion table

Figure 29 gives the different types of power converters and their usual names.

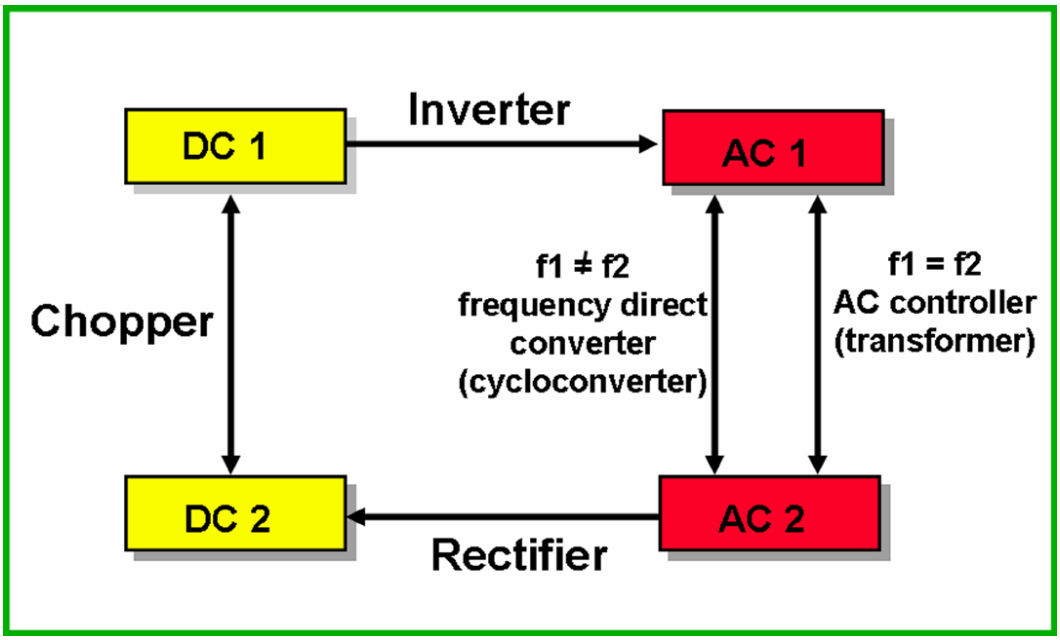


Fig. 29: Power converter classification

8 Synthesis of power converters

8.1 Synthesis method

A general and systematic method to obtain the power converter topologies is given below.

1. Determine the natures of the input and output sources. The basic structure can then be chosen (Fig. 24).
2. From the specification, deduce the voltage and current reversibilities of the input and output sources (one configuration from the general table (Fig. 28)).
3. From the basic structure, identify the different phases of operation according to the reversibilities and the energy transfer control. If necessary, simplify the configuration (short-circuit or open switches).
4. For the various phases, check the sign of the current through the ON switches and the sign of the voltage across the OFF switches: the static characteristics $I_k(V_k)$ of each switches are defined.
5. From the specification (desired output current and/or voltage functions), deduce the sequence of the different phases. For every commutation, represent the working point of each switch before and after the commutation.
6. From the static and dynamic characteristics, choose the type of switches (semiconductor type).

8.2 Examples

8.2.1 Non-reversible current chopper

Hypothesis:

- power conversion between a voltage source and a current source;
- these two sources are unidirectional in voltage and in current.

Following the steps of the synthesis method:

1. a direct converter topology can be used;
2. cell (1,8) of the general table according to the source reversibilities;
3. Sequence 1 (active phase) and 2 (free wheel phase) from Fig. 30;
4. the different plots for the four switches for the two sequences are represented in Fig. 30;
5. from the previous plots, it can be easily deduced that:
   - K1 is a controlled two-segment switch (T switch) (Fig. 13);
   - K2 is an inverse D switch;
   - K3 is a short-circuit;
   - K4 is an open-circuit.

The topology of the converter is thus fully determined.

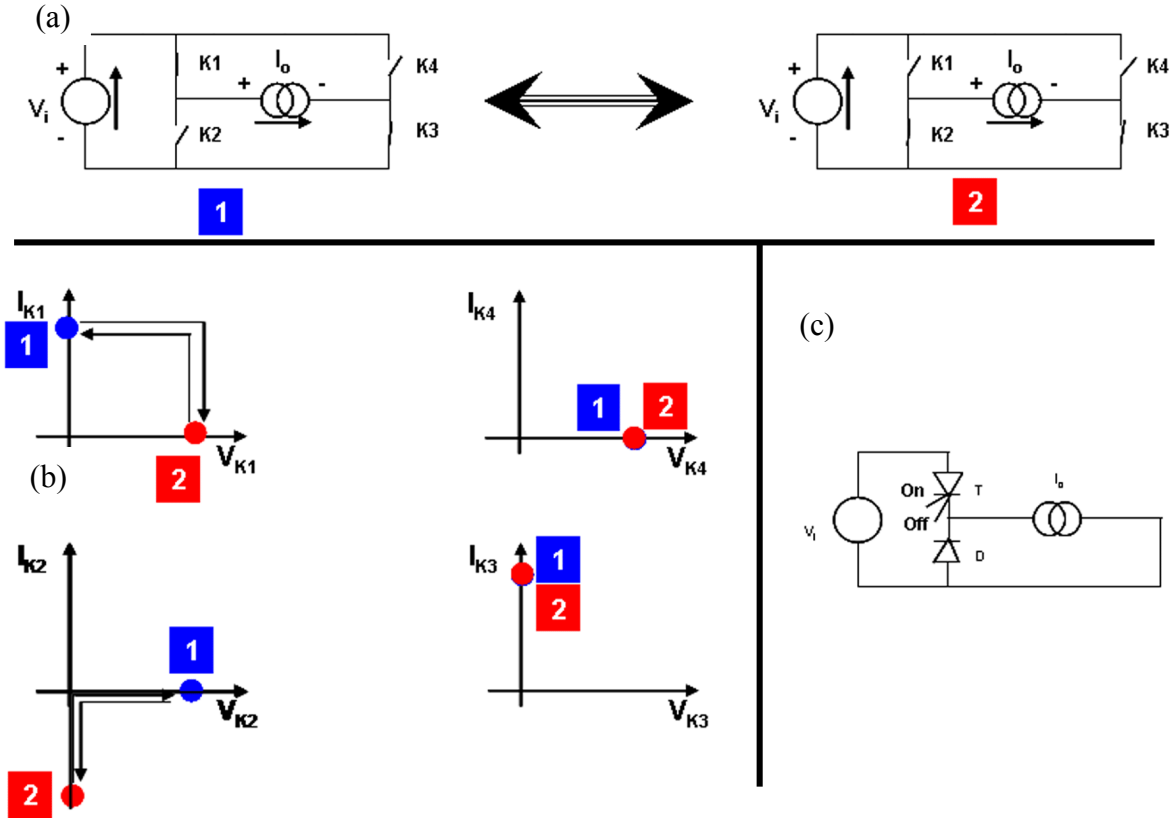


Fig. 30: Study of a non-reversible current chopper. (a) – sequences 1 and 2 (change in K1, K2, and K4); (b) – Current-voltage characteristics of each switch for the two sequences; (c) corresponding topology with transistor and diode.

8.2.2 Reversible current chopper

Hypothesis:

- power conversion between a voltage source and a current source;
- the input voltage source is bidirectional in current;
- the output current source is unidirectional in voltage and bidirectional in current.

Following the steps of the synthesis method:

1. a direct converter topology can be used;
2. cell (2,6) of the general table according to the source reversibilities;
3. sequence 1 (active phase) and 2 (free wheel phase) of Figs. 30 and 31;
4. the different plots for the four switches are represented in Fig. 30 for the two sequences for the transfer of energy from the input source to the output source. Figure 31 represents the analysis of the brake phase: transfer of energy from the output source to the input source.
5. the analysis of the two phases leads to the determination of the structure presented in Fig. 32.

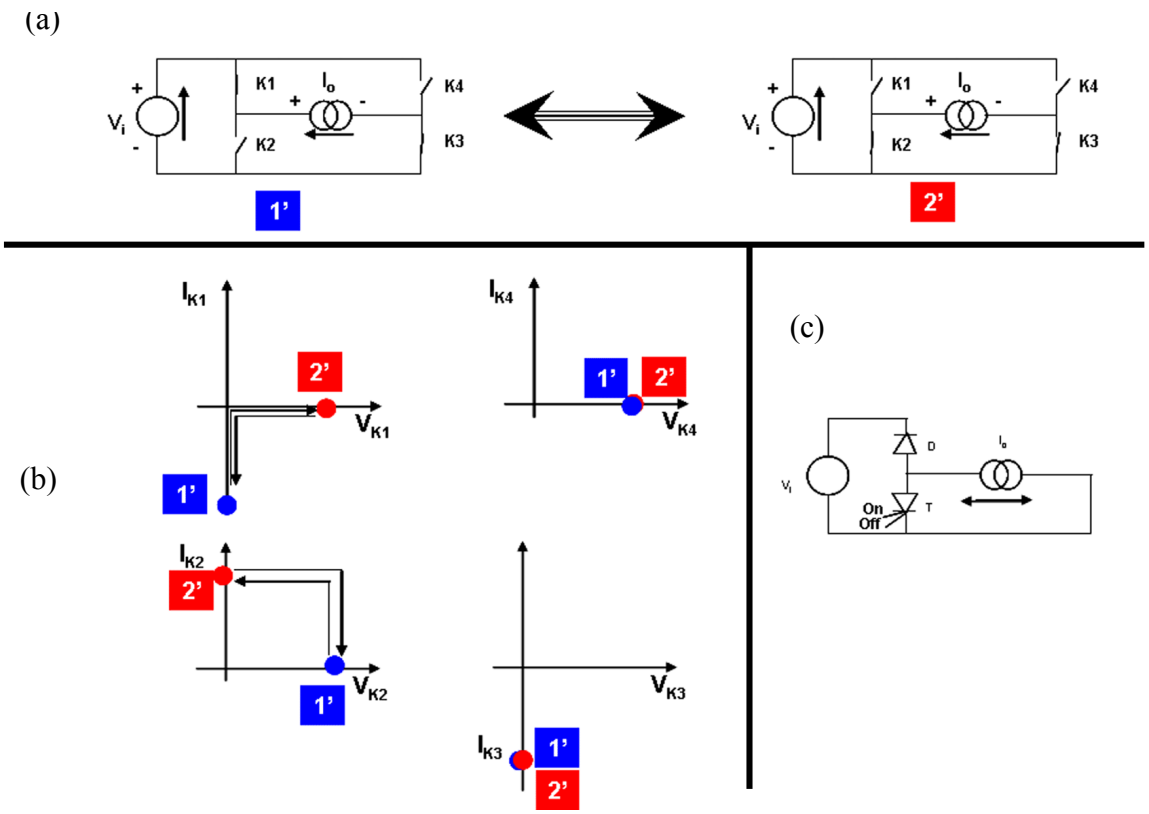


Fig. 31: Study of a reversible current chopper: brake phase. (a) – sequences 1 and 2 (change in K1, K2, and K4); (b) – Current-voltage characteristics of each switch for the two sequences; (c) corresponding topology with transistor and diode.

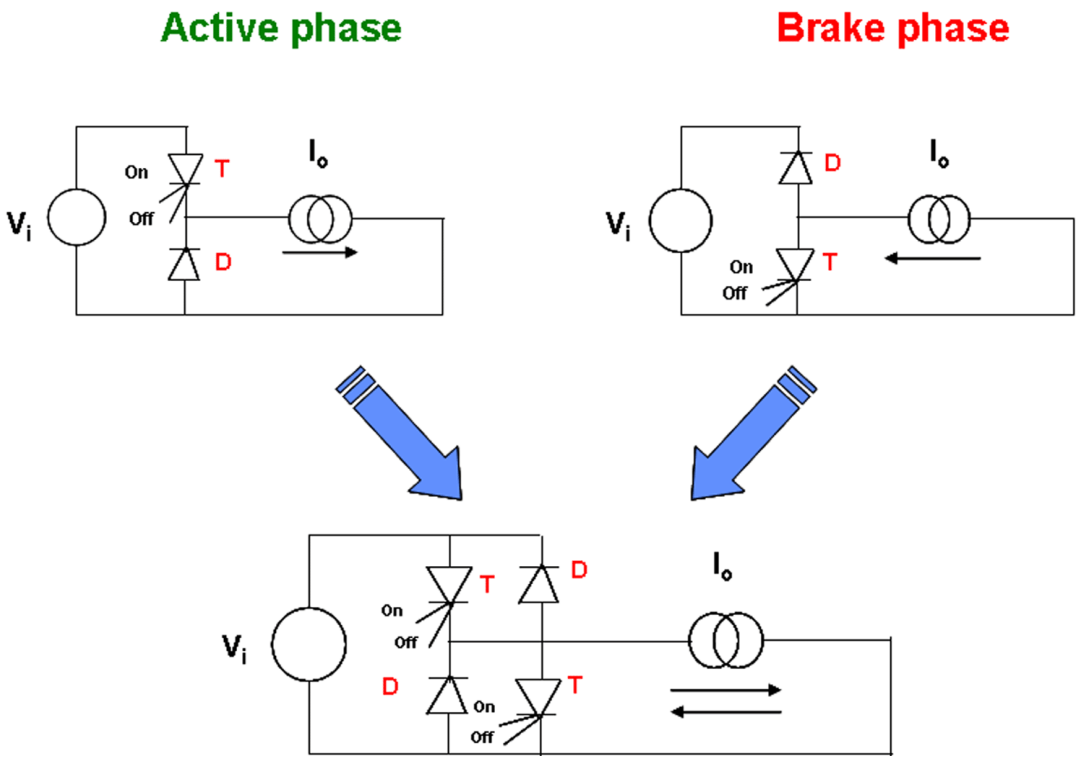


Fig. 32: Structure of reversible current chopper

8.2.3 Voltage inverter

Hypothesis:

- power conversion between a voltage source and a current source;
- the input voltage source is unidirectional in voltage and bidirectional in current; it is a DC source of value *E*.
- the output current source is bidirectional in voltage and bidirectional in current; it is an AC source. The specification is to get a $+E$, $-E$ voltage at the output of the converter.

The steps of the synthesis method are followed.

1. A direct converter topology can be used.
2. Cell (2,5) of the general table according to the source reversibilities.
3. The two sequences are shown in Fig. 33.
4. From the analysis of two sequences, it can be deduced that the switches must be bidirectional in current and unidirectional in voltage. They correspond to three-segment switches (D and T in parallel; Fig. 10).
5. To represent the working point of each switch, it is necessary to detail the specification. Two cases are defined according to whether the output voltage is ahead or not of the output current.

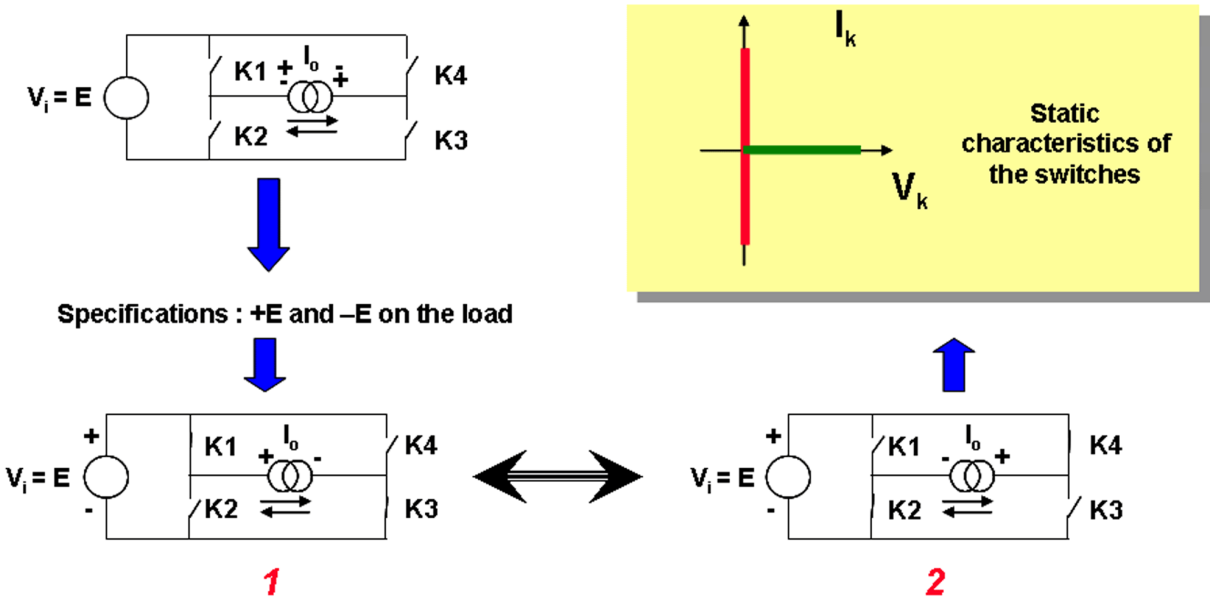


Fig. 33: Sequence of a voltage inverter

8.2.3 .1 Case 1: The output voltage is ahead of the output current

For the hypothesis that the output voltage is ahead of the output current, Fig. 34 shows the dynamic characteristics based on the analysis of the commutation between the two sequences.

It can be easily deduced that the four switches (K1, K2, K3, and K4) should be controlled turn-OFF and spontaneous turn-ON switches (dual thyristor; Fig. 15).

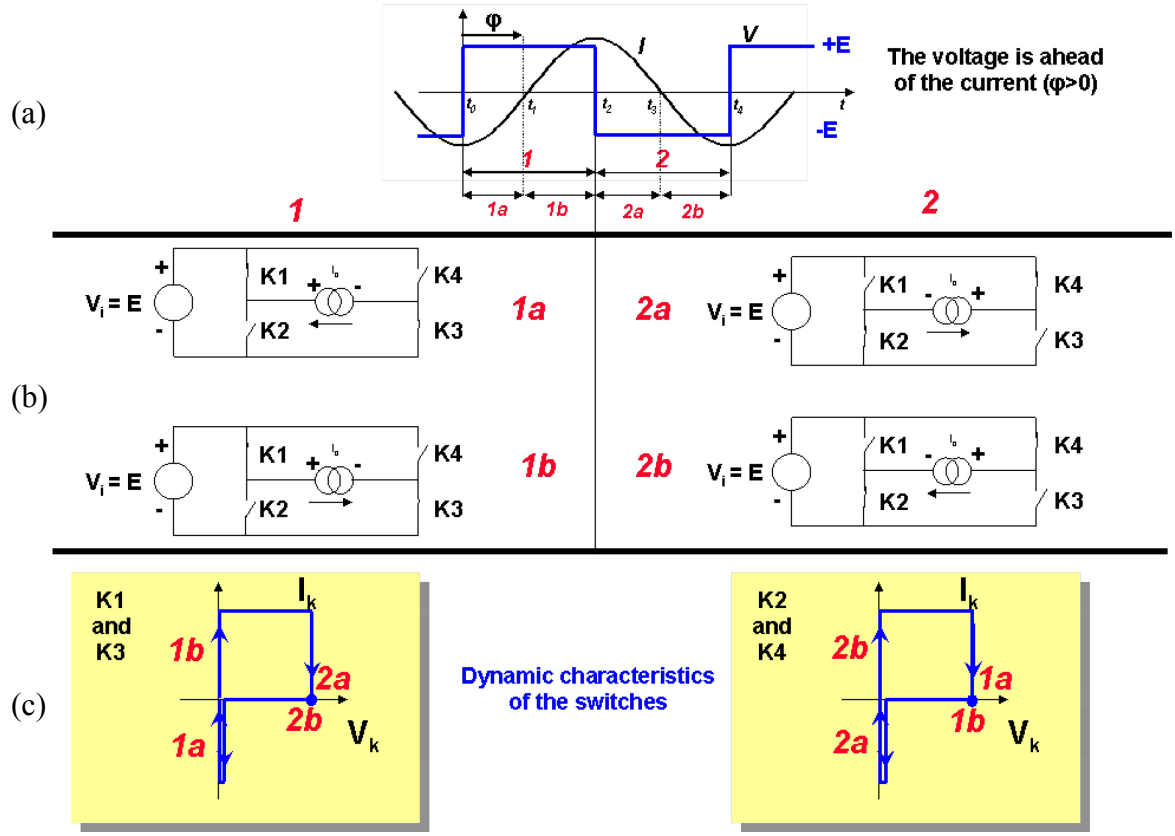


Fig. 34: Voltage inverter (Case 1): (a) – output voltage and current; (b) – Switches states for each time period (1a, 1b, 2a, and 2b); (c) - dynamic characteristics of the switches.

The topology of the converter is fully determined and is shown in Fig. 35. It is a zero-voltage-switching topology (see Section 9).

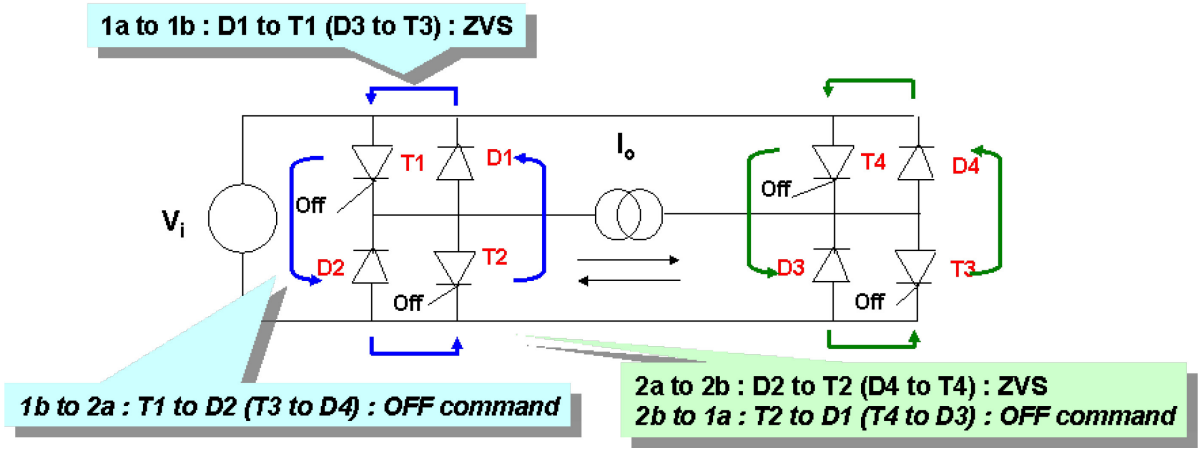


Fig. 35: Voltage inverter (Case 1): converter topology

8.2.3 .2 Case 2: The output current is ahead of the output voltage

Identical study can be made if the output current is ahead of the output voltage. Figures 36 and 37 represent the dynamics characteristics of the switches and the deduced topology. It is a zero-current-switching topology using a thyristor with a reverse diode in parallel (Fig. 15).

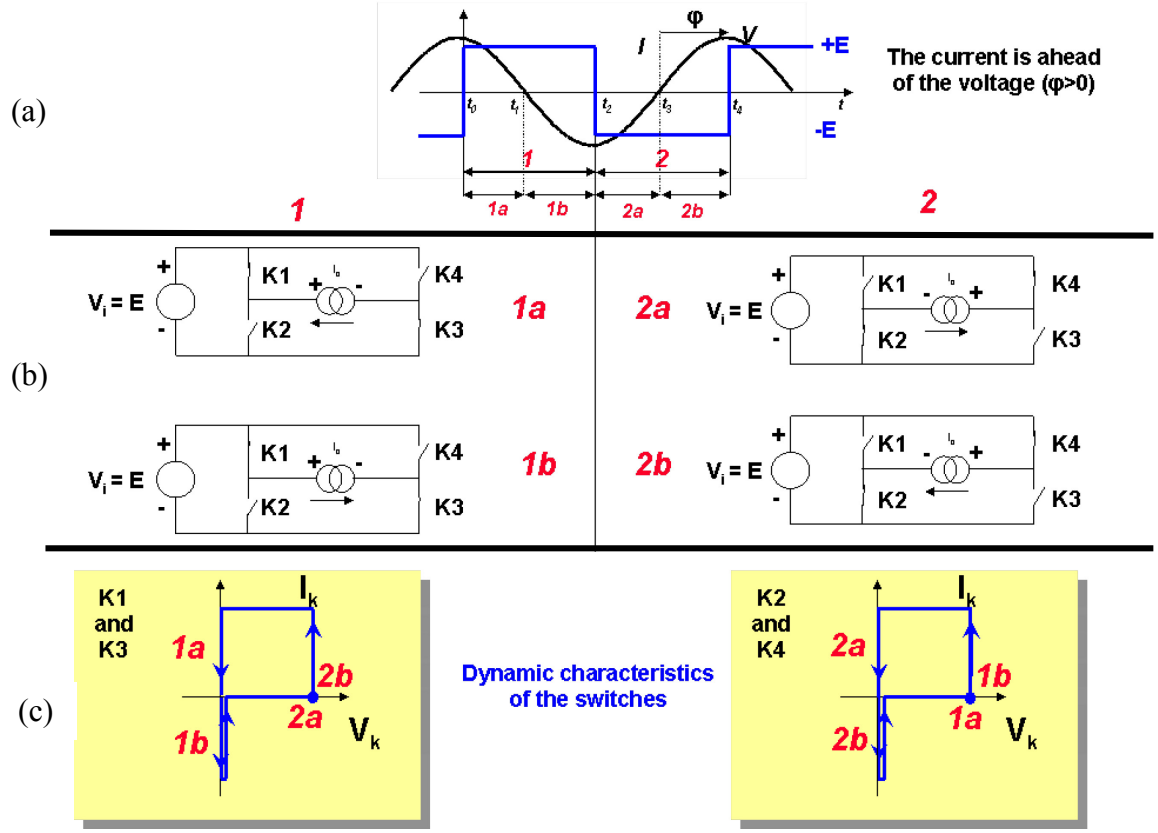


Fig. 36: Voltage inverter (Case 2): (a) – output voltage and current; (b) – Switches states for each time period (1a, 1b, 2a, and 2b); (c) - dynamic characteristics of the switches.

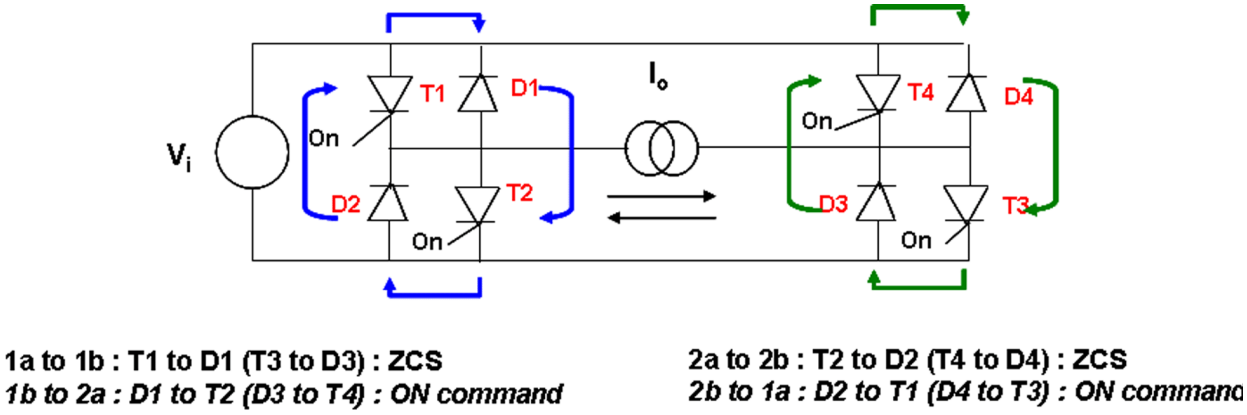


Fig. 37: Voltage inverter (Case 2): converter topology

9 Commutation cell

As presented in the previous chapters, the operation of a static converter can be split into sequences. A distinctive electrical network characterizes each sequence. The interconnection modifications of the sources by switches give the electrical networks. In the general case, the modifications are made by switches, which connect *n* branches to *one*. Figure 38 shows an example of a three-way switch.

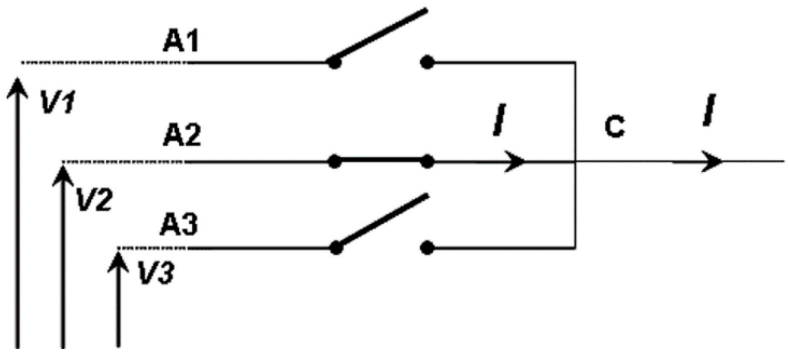


Fig. 38: Three-way switch

The network branches connected to these switches must fulfil the connection laws of the sources. Therefore, it can be deduced that:

- each switch is connected to a voltage source (otherwise opening a switch would result in open-circuiting a current source);
- the node at the centre of the star is connected to a current source since a voltage source can be connected only to a current source through a controlled switch;
- at a given time one and only one switch must be ON to avoid connecting two voltages sources and open-circuiting the current source.

Following these deductions, each commutation mechanism is a sequence of commutation only involving two switches. Thus, an elementary commutation cell, represented in Fig. 39, could be defined. The reversibilities of the voltage and current sources determine the static characteristics of the two switches. The switches need to have static characteristics with the same number of current and voltage segments. The two switches must be complementary, that is to say if one switch is ON the other one is OFF and, furthermore, if the turn-ON (turn-OFF) commutation of a switch is controlled, the turn-OFF (turn-ON) commutation of the other must be spontaneous.

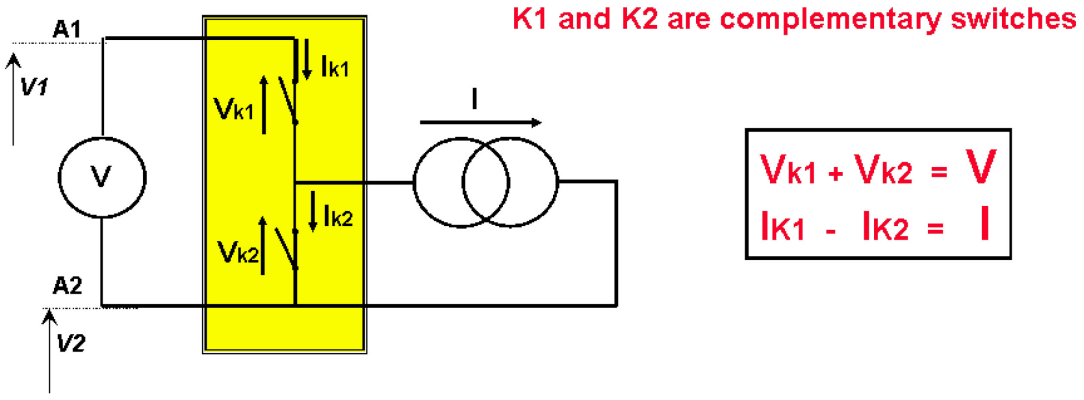


Fig. 39: Elementary commutation cell

To study a power converter topology, it is always fundamental to isolate all the elementary commutation cells and to check the complementarities of the switches. Figure 40 represents several examples of power converter topologies for which the elementary cells were highlighted.

Detailed information on commutation cells and on local and system commutation mechanism can be found in Refs. [9, 10, 13].

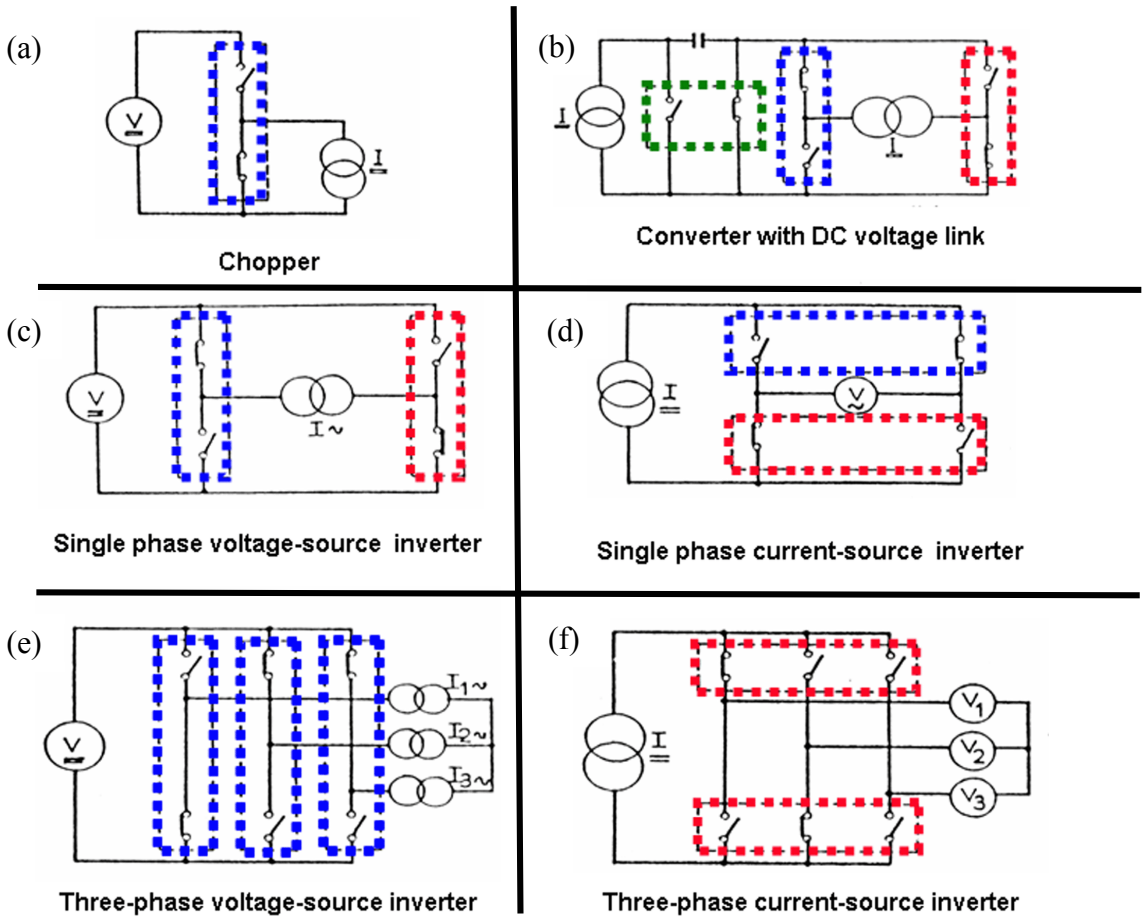


Fig. 40: Elementary cells in power converter examples. (a) – Chopper; (b) – indirect converter with DC voltage link; (c) – single phase voltage source inverter; (d) – single phase current-source inverter; (e) – three-phase voltage-source inverter; (f) – three phase current-source inverter.

10 Hard and soft commutation

In the domain of power conversion, the only available active components were diodes and thyristors. The topologies had to respect the commutation of these components: i.e. spontaneous turn-OFF of thyristors. The commutation mechanism was called 'natural commutation'.

If the spontaneous turn-OFF was not directly fulfilled (especially in the case of DC sources), it was necessary to add auxiliary circuits with reactive components (inductors and capacitors) and auxiliary semiconductors. The goal of these circuits was to create the conditions for thyristor turn-OFF. This commutation mechanism was called 'forced commutation'.

Power specialists were dreaming of having a power semiconductor with a controlled turn-OFF to avoid adding complex and costly auxiliary circuits and being limited to the grid frequency. With the development of the power transistor and the GTO, a new spectrum of topologies was opened. Then, specialists pushed to get faster components with simple and lighter drivers. From 1985, these components are available on the market. Power converters with higher power and frequency were then designed and built. However, the consequence is the management of (very) high dV/dt and dI/dt with stress on semiconductors but also on all of the other components. EMC became a constant concern of power electronics designers. Hard commutation was born! A first approach was to add components (snubber) to slow down the commutation (series inductor for a controlled turn-ON and a parallel capacitor for a controlled turn-OFF) and to avoid as much as possible the commutation losses close to the axes: aided-commutation. To avoid discharging the stored energy of the snubber in the

semiconductor at the next commutation (inductance energy at turn-OFF and capacitor energy at turn-ON), it is necessary to add an auxiliary circuit to discharge the snubber energy and then to generate losses.

The solution to avoid all these problems and be able to use these new fast semiconductors with lossless snubbers is to have only one controlled command per switch. One commutation is spontaneous and the other one is controlled. Two types of commutations are possible: zero-voltage switching (ZVS; Fig. 41) and zero-current switching (ZCS; Fig. 42).

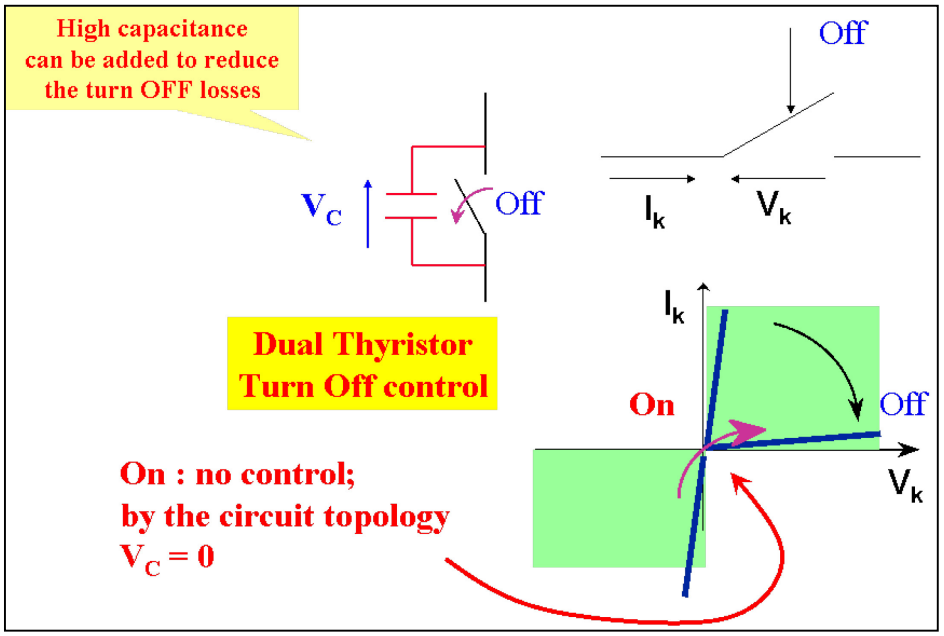


Fig. 41: Zero-voltage switching principle

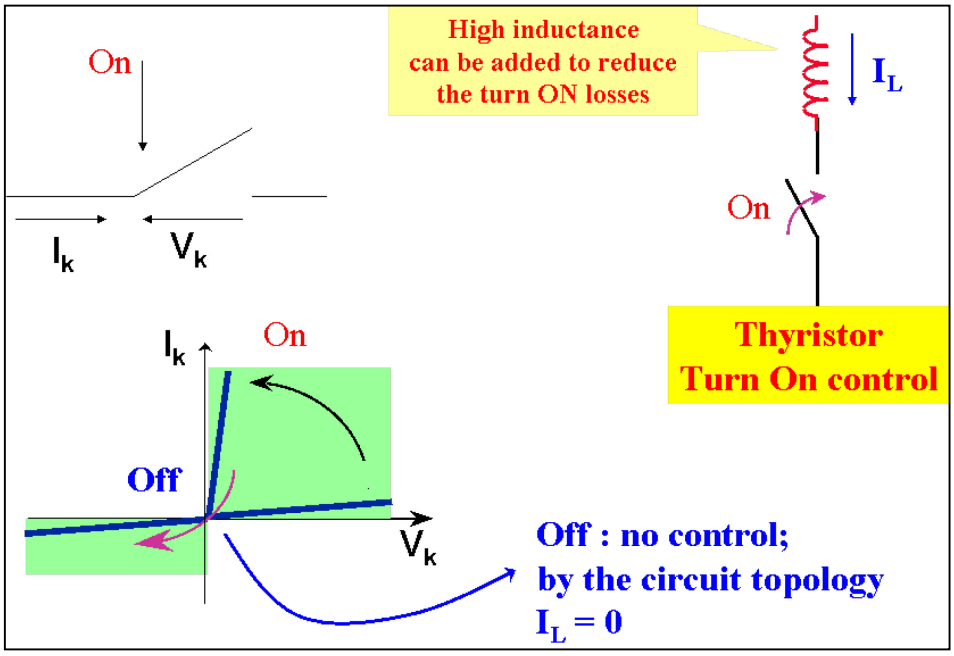


Fig. 42: Zero-current switching principle

The spontaneous commutation is lossless and it is easy to limit the losses for the controlled commutation with a series inductor for ZCS and a parallel capacitor for ZVS. These reactive

components are naturally discharged for the next commutation, which is a spontaneous commutation. This commutation mechanism is called soft commutation.

For a power converter topology to obtain the conditions of soft-commutation, the following conditions must be fulfilled:

- the switches must have three-segment characteristics;
- the characteristics must be entirely described at each period;
- the converter must include reversible source(s) able to provoke the conditions for spontaneous commutation of the switches at the right instant.

The attractive properties of soft-switching [9, 11] are:

- the large reduction of switching losses;
- the improved reliability due to reduced stress;
- a limited frequency spectrum, which means an advantage with respect to EMI and losses in passive components;
- a reduction of weight and volume of the components resulting from the higher switching frequency;
- a higher bandwidth resulting from the high internal switching frequency;
- integration of parasitic elements in the commutation mechanism (e.g. leakage inductance of the transformer in the resonant circuit).

The soft-commutation domain has been a key research domain in power electronics in the last two decades. Numerous papers and conferences can be consulted for more information.

It should be noted that all LHC power converters were designed with soft-commutation topologies [12, 13, 14].

11 Conclusions

This paper has made an introduction and classification of the basic power converter components: sources and switches. From interconnection rules of the sources, the direct and indirect power converter topologies were deduced. A general and systematic method to synthesize was described and illustrated with examples.

With the fast development of turn-off controllable power semiconductors, the commutation mechanism becomes more and more important. To improve the performance of converters, frequencies are increased with the minimization of losses and EMI perturbations. Local treatment of commutation is no longer possible and it is crucial to design a suitable topology for the commutation of high-frequency and high-power semiconductors. To reach these goals, it is necessary to create, through the circuit topology, the turn-ON and turn-OFF conditions for the switches. Soft commutation is certainly the most appropriate and optimal solution.

Acknowledgements

For the work reported here, different references in the domain of power electronics and especially from publications of the Laboratoire d'Electrotechnique et d'Electronique Industrielle, Toulouse, France (LEEI) members were used. The first author would like to express his deep gratitude and admiration to Professor Foch, who initiated the work around the systematic synthesis of power converter topologies. It was an opportunity and honour to work with him for more than 10 years.

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Metallized Film Capacitor Lifetime Evaluation and Failure Mode Analysis

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Abstract
One of the main concerns for power electronic engineers regarding capacitors is to predict their remaining lifetime in order to anticipate costly failures or system unavailability. This may be achieved using a Weibull statistical law combined with acceleration factors for the temperature, the voltage, and the humidity. This paper discusses the different capacitor failure modes and their effects and consequences.

Keywords
Metallized film capacitor; failure mode; lifetime.

1 Capacitor technologies

The following different power capacitor technologies are used in inverters:

- Electrolytic capacitors characterized by very big capacitance per volume unit, but with low rated voltages and very important power losses due to the ionic conductivity. In particular, the bigger the capacitance density, the lower the rated voltage.
- Film foil capacitors made of dielectric films between two plain aluminium foils. These capacitors can sustain very high currents.
- Metallized film capacitors, which are made with dielectric films with a metallic coating on the surface. With this technology the electric-field stress may be much bigger than with film capacitors thanks to the metallization self-healing capability.

Today the dielectric films that are used are mainly polypropylene (PP) or polyethylene terephthalate (PET). Formerly, paper (PA) was used in film foil technology—either pure paper or mixed with polypropylene (DM). In special applications, where high temperatures are required, polyethylene naphthalene (PEN) up to 125°C or polyphenylene sulfide (PPS) up to 150°C are used.

PET presents the following advantages over PP: a dielectric constant 50% bigger ($\varepsilon = 3.3$ versus 2.2), which means 50% more capacitance in the same volume, a better mechanical resistance (which means a higher endurance to self-healing), and the possibility of manipulating thinner films, consequently leading to a smaller capacitance and a higher exploitation temperature (+10°C). The negative point is that the loss factor is ten times larger, which means a ten-fold increase in temperature elevation for the same rated power. The nominal electrical field is about the same.

The capacitive elements must be dried to remove moisture, which would cause accelerated aging and bigger losses if left in the capacitor. In the case of power capacitors, the dried elements are either impregnated with vegetable oil or with gas (SF_6, N_2, etc.).

The dielectric films are either wound or stacked before being inserted in a plastic or metallic container. The best winding machines are required to produce active wound elements of reliable quality in the case of oil-free capacitors. One way of overcoming the difficulty of controlling the space ratio between the gas and the film in the winding curves is to wind the film on a large-diameter wheel and to cut the film layers to obtain a stack.

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The plastic containers are not completely moisture tight—there is always some residual permeability in polymers. In the case of metallized films, this may lead to electrode corrosion when the capacitors are submitted to environmental conditions of high humidity.

The electric-field stess in metallized film capacitors may be much larger than in film foil capacitors. This is obtained thanks to the ability of the electrodes to self-heal. If a breakdown occurs in the polymer, the current will increase through the defect and on the electrode near the defect. Close to the defect the current density will be big enough to evaporate the 100 nm metallic layer. If the capacitor is well designed, the phenomenon will stop when the diameter is large enough to insulate the defect and small enough not to damage the film. The electrode resistance (given in ohm/square) is the key parameter to define to achieve good self-healing behaviour, with Joule losses as small as possible. A thick metallized layer will present a lower resistance, but higher energies will be involved during the self-healing process, leading to greater damage [1-5].

2 Capacitor failure modes

Most of the metallized film capacitors fail because the capacitance drops below the required tolerance. This normally occurs after the expected lifetime given by the manufacturer. The capacitance drop is generally accompanied by an increase of the loss factor.

From a general point of view, the causes of capacitor failures may occur because of bad design, bad processes, or inappropriate application conditions. During the design phase, the following causes may lead to failure: the dielectric film is too thin, insulation distances are too small, the metallization layer is too thick or too thin, or the conductor is the wrong size. During production, causes may include the following: poor mechanical tension control during the winding, bad drying (leaving too high a humidity content in the capacitor), or bad sealing. In application, the causes may be: higher voltages, EMI, lightning, higher temperature, or a high humidity environment.

The failure modes are a little more complicated to describe because different causes may lead to the same modes. Figure 1 gives a non-exhaustive summary of the possible failure modes which can occur in metallized film capacitors.

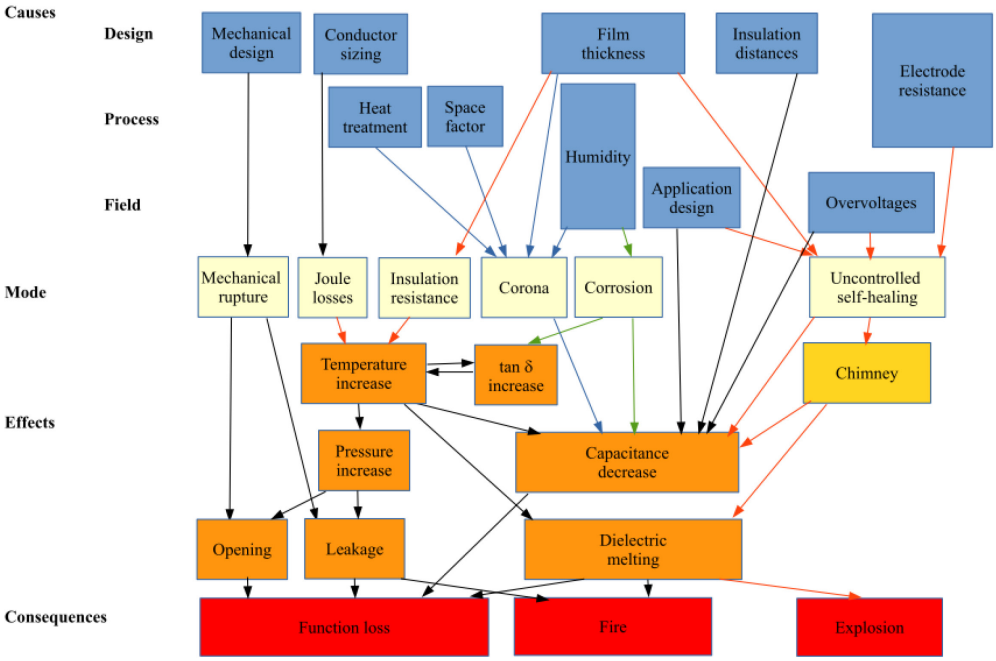

Fig. 1: Metallized film capacitor failure modes with their causes, effects, and consequences

For example, bad space factor control of the dielectric films during the winding operation will be the cause of the electrode corona demetallization, which will lead to a fast capacitance drop and to the loss of functionality of the capacitor.

A bad choice of the metallization resistance value, or poor metallization control during the film manufacturing process, leads to bad self-healing management, which may damage the dielectric film mechanically and produces heat which is transmitted locally to the next film layers. At this location the dielectric strength of the film drops and breakdown may occur. Consequently, chimneys of melted polypropylene may appear through the winding. The formed channel is conductive, inducing a drop in the insulation resistance and a leakage current that can generate enough heat to melt the polypropylene and increase the internal pressure of the capacitor. Along with bad metallization resistance, the final consequence can, in the worst case, lead to fire ignition or even a capacitor explosion.

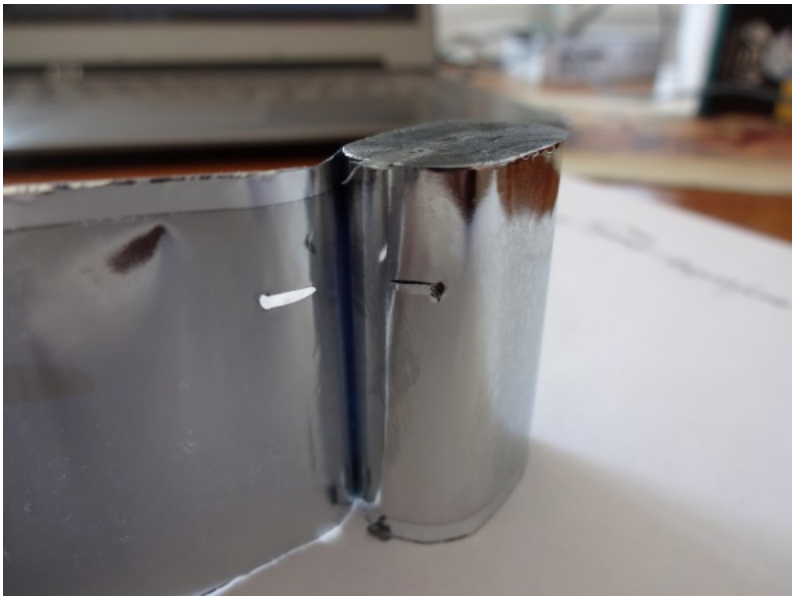

Fig. 2: Chimney through the film layers in the capacitor winding

One of the main failure modes is often due to high currents, which increase the capacitor temperature, leading to a reduction of the breakdown voltage and, in the worse cases, even melting of the capacitor. In this regard, the shape of the capacitor is very important. For high-power applications, it is important to build short elements in order to reduce the current path length and increase the number of parallel layers, and consequently reduce the heating. The current capability of a capacitor is specified through the series resistance R_s and the loss factor tan δ_s at different frequencies. The relation between the two factors, in the high-frequency domain where the effect of the insulation resistance is negligible, is given by the linear relation

$$\tan \delta_s = \frac{Z_R}{Z_i} = R_s \omega C , \tag{1}$$

where C is the capacitance, $\omega = 2\pi f$ is the frequency, Z_R is the impedance real part and Z_i the impedance imaginary part.

The presence of humidity in the capacitor, because of poor drying during the manufacturing process, or because the moisture permeability of the material was too high, or because the humidity level where the capacitors are installed was too high, may lead to three failure modes with different effects and consequences.

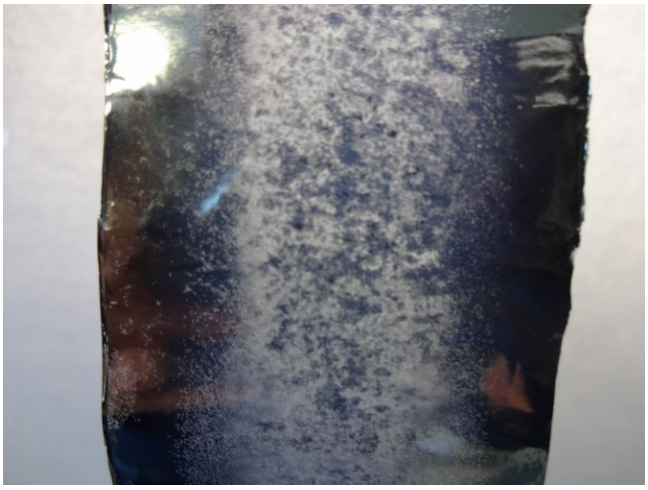

Fig. 3: Electrode corrosion due to the presence of moisture

The first is electrode corrosion (see Fig. 3) [6-8], where the series resistance will slowly increase over time. The effect is a loss factor increase due to the electrode thickness reduction and a heat dissipation increase. The elevation of the temperature will accelerate the capacitance loss because of the reduction of the dielectric strength with temperature, ending with the loss of functionality of the capacitor.

The second effect (see Fig. 4), today known as 'corona' [9-11], is due either to a decrease of the dielectric strength of the gas present in the capacitor in the gaps between the dielectric films or to a poor space factor control of the films. The bigger the gap, the more severe the problem. The thickness of the gap is characterized by the space factor, which is the ratio of the dielectric thickness to the total distance between the electrodes. This space factor is very difficult to control in curves of flat windings, leading manufacturers to build either round winding or stacks. Only performant winding machines can achieve good space factor control by managing the mechanical tension of the films during the winding. The consequence of this is a fast capacitance decrease due to the appearance of corona discharges on the electrode edges, i.e., the locations where the electrical field is more intense due to the point effect. In the case of segmented metallization, the corona failure mode may also propagate from the non-metallic lines which separate the active electrode metallic areas.

Fig. 4: Demetallized electrodes by corona arcing in the gas gap between the films

The third failure mode is a reduction of the insulation resistance, which is the parallel resistance of the capacitor. A decrease in insulation resistance leads to an increase in current leakage from one electrode to the other. This phenomenon is present at low frequency. It may be measured via either the

loss factor (tan δ) or the d.c. resistance R_p. The relation between the two parameters is given by the following relation (only true at very low frequencies):

$$\tan \delta_p = \frac{Z_R}{Z_i} = \frac{1}{R_p \omega C}. \quad (2)$$

This later failure mode may have a runaway behaviour. The more the insulation resistance decreases, the more heat is produced, and the more the temperature increases, which leads to a new insulation decrease. This phenomenon may end with the appearance of chimneys and melting of the dielectric.

3 Lifetime expectancy

The lifetime [12] of a capacitor is the time to failure, where failure is defined as the lack of ability of a component to fulfil its specified function. The failure modes are classified into two main categories: 'early failures' and 'wear out failures', which are reflected in the curve known as the 'bathtub' curve (Fig. 5): at the beginning of the component's existence, in its 'infancy', the failure rate is rapidly decreasing. These 'youth' failures are normally screened by routine tests performed by the manufacturer. They are due to design and process weaknesses which have not been detected by the design and process failure modes and effects analysis FMEA performed during the development. They are more probably due to production process variations or to changes in material quality. The process variations are due to tool wear, operator change, and lack of formation. This early failure mode is not taken into account by the Weibull model theory. In normal operation this failure process should not be observed in the field of applications. If it occurs, the capacitors are normally covered by manufacturer's product warranty.

Once the 'early failures' regime is past, the failure rate starts to follow a statistical prediction law which depends on several parameters that may be defined experimentally as a function of the voltage, the temperature, and the environmental humidity. It has been shown that a Weibull statistic can provide a good prediction of the capacitor lifetime expectancy.

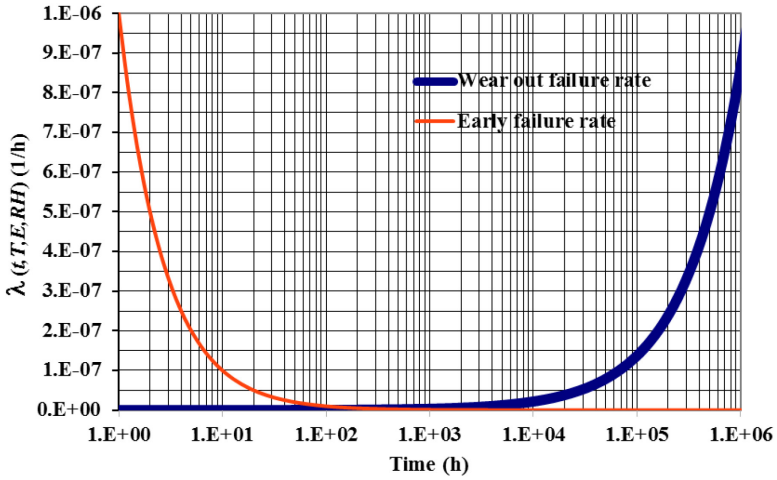

Fig. 5: Bathtub curve of the failure rate function showing the infancy or early failures occurring at the beginning of the component's life (in red) and the wear out curve (in blue) which is defined by aWeibull law with 2 parameters: the power factor p = 1.8 and the inverse of the time necessary for 63% of the sample to fail $\lambda_0 = 1/1{,}500{,}000\ h^{-1}$.

The failure rate $\lambda(t)$ may be given in FIT (failure in time), which is the number of failures occurring during 10^9 h of working of one object, i.e., $3E^{-7}$ h^{-1} corresponds to 300 FIT. The Weibull failure rate is given by

$$\lambda(t) = \lambda_0 \; p\,(\lambda_0 t)^{p-1}, \tag{3}$$

where λ_0 must not be confused with $\lambda(t)$. λ_0 is a constant (independent of time, but dependent on temperature, voltage, and humidity) which corresponds to the inverse of the time necessary for 63% of the sample to fail, and $\lambda(t)$ is the inverse of the mean time to failure (MTTF). In the wear out failure region, $\lambda(t)$ increases with time. The manufacturer specifications give the maximum value of $\lambda(t)$ within the announced lifetime: for example, 150 FIT and 100,000 h of lifetime expectancy in Fig. 5. The slope parameter of the Weibull law is denoted by p.

The survivor or Weibull reliability function $R(t)$ is the probability that a capacitor has not failed or has not lost its function at time t and is still working. The survivor function is given by

$$R(t) = \mathrm{e}^{-(\lambda_0 t)^p} \; . \tag{4}$$

When multiplied by the number of capacitors N in the batch, this gives the expected number of capacitors still working after time t. There are capacitor manufacturers [13] that use a simple exponential model instead of the more complex Weibull model. Actually the exponential model corresponds to a Weibull model where $p = 1$. In this exponential model the failure rate is constant over the time $\lambda(t) = \lambda_0$. To fit this model to the actual statistical behaviour of capacitors, manufacturers limit the exponential model to a time period which they call the 'service life of the product'. After that time period the failure rate starts to increase.

Weibull statistics can also be used to predict the capacitance evolution of a metallized capacitor under electrical, thermal, and humidity stresses. In such cases, the failure definition will be, for example, 1% or 1‰ capacitance loss, depending on the available resolution of the measurement device. The capacitance will be given straightforwardly by the survivor function. The Weibull reliable life, which gives the expected lifetime of a capacitor for a given reliability level (the proportion of remaining working objects, in our case capacitance) is

$$T_{\mathrm{R}} = \frac{1}{\lambda_0}\left\{-\ln(R)\right\}^{1/p}, \tag{5}$$

where λ_0 is the failure rate for the special case when 1/e, or 36.8%, of the samples still remain.

Table 1: Capacitor lifetime expectancy factor as a function of the required capacitance minimum in an exponential model.

Reliability (%)	**Lifetime, $1/\lambda_0$ (h)**
36.8	1
50	0.693
63.2	0.500
80	0.223
90	0.105
95	0.051
98	0.020

If the manufacturer gives a capacitor failure rate of 50 FIT at 40°C and $U_n/2$ for an exponential model, it means that the lifetime expectancy for a capacitance drop tolerance of 10% will be 2.1×10^6 h in these conditions.

4 Aging acceleration factors

The speed of capacitance drop depends on the temperature, the voltage, and the humidity. The increases in these parameters are considered as aging acceleration factors. These factors are determined experimentally based on the following theories.

4.1 Temperature

It has been shown [14] that capacitor aging as a function of the temperature follows an Arrhenius law, in other words an exponential law

$$t(T) = t_{T_n} \exp\left(\frac{E_a}{k_B}\left(\frac{1}{T} - \frac{1}{T_n}\right)\right), \tag{6}$$

where t_{T_n} is the expected lifetime at a reference temperature, 70°C or 85°C for example, k_B is the Boltzmann constant, and E_a is an activation energy. A relatively good fit of Epcos/Vishay factors (see Fig. 6) may be obtained with a ratio $E_a/k_B = 7000$ K [15]. Between 40°C and 70°C there is an acceleration factor of 7.1 with the parameters considered.

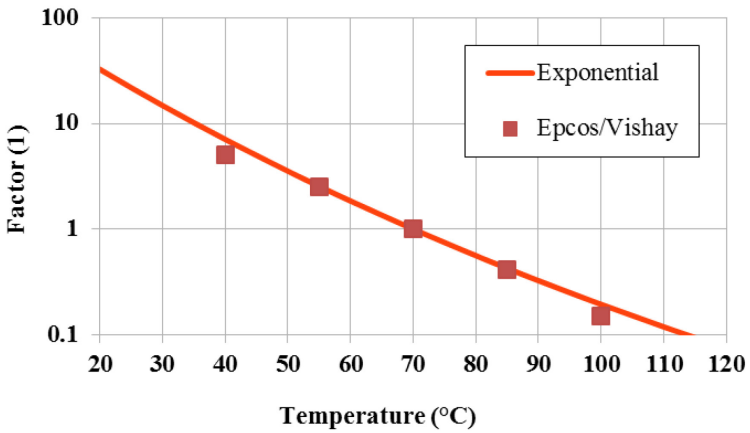

Fig. 6: Temperature acceleration factor

4.2 Voltage

Regarding voltage dependency, authors use either an inverse power law

$$t = t_{U_n}\left(\frac{U}{U_n}\right)^{-n} \tag{7}$$

or an exponential law

$$t = t_{U_n} \exp\left(-\alpha \frac{(U - U_n)}{U_n}\right), \tag{8}$$

where t_{U_n} is the expected lifetime at the nominal voltage or reference voltage and t/t_{U_n} is the voltage acceleration factor.

A careful examination shows that these laws do not differ much when considered between 0.7 and $1.3U_n$. To sketch Fig. 7, n and α have been both set to 3.5.

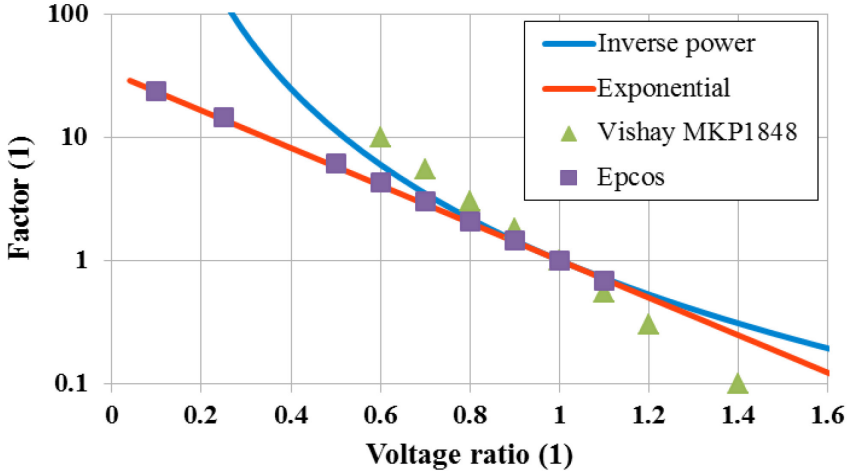

Fig. 7: Acceleration factor of the aging as a function of the voltage level. In this diagram the inverse power law and the exponential law are both parameterized with a factor 3.5. The Vishay data would fit better with an exponential law with factor 5 [16, 17].

Between $U_n/2$ and U_n there is an acceleration factor of approximatively 5 (Epcos) to 10 (inverse power) with the parameters considered. The discrepancy between the values may be attributed to the different technologies produced by the different manufacturers. It is interesting to note that the Vishay display on p. 6 of Ref. [18] has almost the same accelerating factors as Epcos.

4.3 Humidity

Humidity is a concern for capacitors contained in plastic because moisture can permeate through this type of material. Once inside the capacitor, the moisture has several effects: first, it decreases the electrical strength of the gas in the case of oil-free capacitors, leading to corona demetallization of the electrode, and secondly it corrodes the electrode. When moisture is present in the dielectric film, the loss factor is increased, because of the presence of water dipoles, and the insulation resistance is reduced, leading to current leakage and generation of heat. The lifetime as a function of the humidity level can be estimated using the following relation [19]:

$$t(RH) = t_{H_n}\left(\frac{RH_n}{RH}\right)^m, \tag{9}$$

where t_{H_n} is the expected lifetime at a reference humidity level.

4.4 Capacitor lifetime expectancy calculation

To design and size a capacitor correctly engineers must work through two steps. First, they must determine the law parameters: E_a for the temperature, n for the voltage, and m for the humidity. This is basically achieved by defining a plan of the experiment with three different temperatures, voltages, and humidity levels. The second step is the calculation of the lifetime expectancy as a function of the customer specifications. For example, for a solar inverter, half of the time there is no voltage and the temperature is 20°C, 20% of the time the voltage is maximum and the temperature reaches 90°C, and 30% of the time the voltage is 80% of the maximum and the temperature is 60°C. Each stress condition must be converted to a reference condition value. The sum of the contributions will determine the lifetime expectation.

Table 2: Lifetime expectancy with indicative data

Duration (%)	Voltage (U_n)	Temperature (°C)	Converted aging weight @ reference conditions(%)
50	0	20	5
30	0.8	60	25
20	1	90	70

In most applications, in the first step the required dielectric thickness is calculated at the reference temperature for the specified voltage distribution. In the second step the temperature distribution is used to adapt the dielectric thickness to the temperature profile requirement. In the section 'Power cap sizing' of the site http://www.garmanage.com [20], there is a tool which allows the user to calculate the lifetime expectancy with ten different stresses.

Taking again the example of a failure rate of 50 FIT in an exponential model, which gives a lifetime expectancy of 2.1×10^6 h at 40°C and $U_n/2$, it may be calculated by multiplication of Eqs. (7), (8), and (9)

$$t(T,U,RH) = t_{T_n,U_n,RH_n} \exp\left(\frac{E_a}{k_B}\left(\frac{1}{T}-\frac{1}{T_n}\right)\right)\left(\frac{U}{U_n}\right)^{-n}\left(\frac{RH_n}{RH}\right)^{m} \tag{10}$$

that the lifetime at 70°C and U_n may be estimated to be approximatively equal to 60,000 (h) or nearly 7 years.

5 Technology qualification

The next thing to do is to evaluate the confidence level that, in operation, a given number of capacitors k in a batch of N capacitors are fulfilling the defined condition (for example, a proportion $p > 90\%$ of remaining capacitance after 100,000 h of operation).

The confidence level is given by a binomial law (failed/not failed) and will improve with the number of capacitors which pass the tests. The reverse question is: how many pieces have to be tested to get a given confidence level? The simple relation

$$n = \frac{\log(1-\mathrm{CL})}{\log(p)} \tag{11}$$

yields the number of pieces which must tested without failure to get a confidence level CL. For example, in an accelerated test at 70°C and $1.4U_n$, $n = 16$ pieces must be tested, and none must fail during a 2000 h test, to get a confidence level of CL = 80%; in other words, 80% of all the capacitors will have a remaining capacitance greater than $p = 90\%$ in these conditions. Considering the acceleration factors, the test will state that 80% of all the capacitors will have more than 90% of their capacitance after 60,000 h of operation at U_n and 40°C.

In order to introduce the new technology of oil-impregnated metallized film with an electrical field rated at 200 V/μm, the company Montena Components (today called Maxwell Technologies), in collaboration with the French railways company (SNCF), ran comparative accelerated tests during the 1990s, alongside the tests defined by the IEC 61071 standard [21]. The TGV high speed train input filter capacitor bank has a nominal voltage of 1800 V d.c. and a capacitance of 8 mF. The requested lifetime is 20 yr with a capacitance tolerance ±10%. The bank is built with four 2 mF capacitors.

The volume and weight of the capacitors vary inversely with the square of the electrical field. The first generation was operated at 150 V/μm, and each capacitor had a mass of 44 kg. In a TGV in normal commercial use, a bank at 200 V/μm (four capacitors of mass 22 kg with film thickness of 9 μm) was mounted in one of the tractors, and a bank at 240 V/μm (four capacitors of mass 17 kg with film thickness of 7.4 μm) was mounted on the other side of the train. The voltage and climatic conditions were therefore the same for the two batteries.

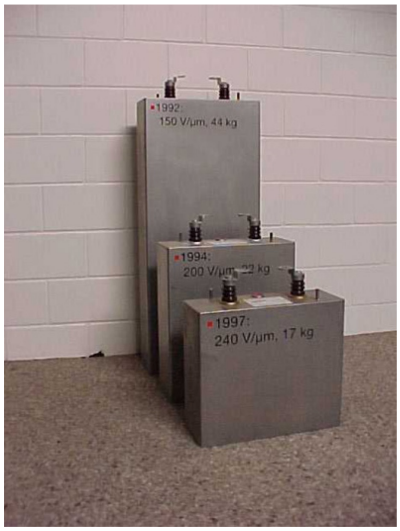

Fig. 8: A 2 mF 1800 V d.c. capacitor for input filters of TGV application. The sizes correspond to 150, 200, and 240 V/μm in the dielectric.

In parallel with the field experiment, a 2 mF capacitor, made with 9 µm thick film, has been tested in an oven at 70°C in the manufacturer's laboratory at 2500 V d.c., a voltage which corresponds to an electrical field of 280 V/μm. The capacitors in the TGV have been measured before the test and after 6 months and one, two, and four years, the capacitors in the laboratory have been measured weekly at the beginning and monthly at the end of the test.

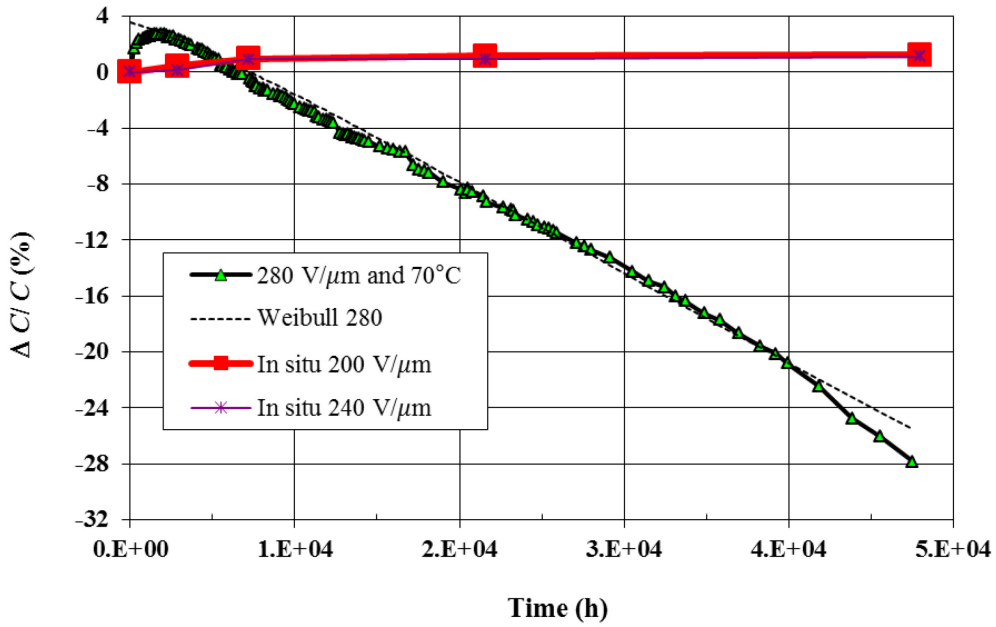

Fig. 9: Capacitance loss as a function of time for 280 V/µm laboratory test at 70°C and TGV in situ tests at 200 and 240 V/mm film [22].

At the beginning of the stress application a slight capacitance increase is observed because of the electrostatic compression of the films. It is also interesting to note that during four years the two capacitor batteries mounted in the TGV in commercial use are still in the compression phase.

The capacitance loss of a metallized film capacitor may be fitted by a Weibull law. In the case of an electrical field of 280 V/μm and an oven temperature of 70°C, a good fit is obtained with $p = 1.2$ and $\lambda_0 = 1/120{,}000\ h^{-1}$. The 10% capacitance loss has been reached after 20,000 h at 70°C and 280 V/μm; tan δ was smaller than $70E^{-4}$, whereas it was $30E^{-4}$ at the beginning.

With a very rough estimation of mean temperature of 35°C inside the TGV tractor, a temperature acceleration factor of 10 between 35 and 70°C and a voltage acceleration factor of 10 between 200 and 280 V/μm, one may expect a lifetime of 2,000,000 h to reach 10% capacitance loss at 35°C and 200 V/μm. With an acceleration factor of 3 between 240 and 280 V/μm, the expected lifetime at 240 V/μm would be 'only' 600,000 h.

6 Conclusion

Capacitors often represent a small part of the cost of an installation. Their failure however may have huge physical and financial consequences. A typical example is a small capacitor of cost 1p connected in series in the electronic control of a freezer which leads to almost all these devices having to be scrapped when they fail. When capacitors have to be used in highly reliable applications, they should be tested in advance.

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Power Converters and Power Quality

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Abstract
This paper discusses the subject of power quality for power converters. The first part gives an overview of most of the common disturbances and power quality issues in electrical networks for particle accelerators, and explains their consequences for accelerator operation. The propagation of asymmetrical network disturbances into a network is analysed. Quantitative parameters for network disturbances in a typical network are presented, and immunity levels for users' electrical equipment are proposed. The second part of this paper discusses the technologies and strategies used in particle accelerator networks for power quality improvement. Particular focus is given to networks supplying loads with cycling active and reactive power.

Keywords
Disturbances; flicker; harmonics; Static Var Compensator; POPS.

1 Introduction

Network disturbances and power quality are issues of increasing importance, as the share of sensitive electronic equipment is steadily increasing in modern power systems. Due to their complex nature and the highest requirements for precision, power converters for particle accelerators are extremely sensitive to network disturbances. A large percentage of all unwanted accelerator stops, so-called major events, is related to such disturbances. Several cases of particle beam instabilities that were caused by power quality issues have been observed. This paper discusses the principal aspects of power quality, with a particular focus on power converters for particle accelerators.

The main objectives of this paper are to raise awareness amongst power converter specialists about this subject, and to discuss the technologies and main engineering principles that can be applied to reduce the impact of power quality issues on particle accelerator operation.

2 Classification of disturbances

The most critical disturbances are discussed below [1-9].

2.1 Voltage dips

Voltage dips are two-dimensional phenomena, characterized by their amplitude and duration. They are typically caused by short-circuits in the electrical network upstream or downstream of the observation point. Voltage dips have a typical duration of 50–200 ms (in some cases up to 1000 ms), and an amplitude typically of −5% to −100%.

Voltage dips are the principal cause of power quality issues related to particle accelerators, and for this reason it is essential to define the immunity levels of the electrical equipment in order to 'survive' most of these disturbances without tripping the particle accelerator.

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2.2 Short supply interruptions

Short supply interruptions can be seen as voltage dips to zero. They are typically caused by short-circuits in overhead lines, which are cleared when the protection systems reclose. Short supply interruptions can last up to 180 s. For short supply interruptions, the concept of immunity of equipment is not applicable, simply because most equipment will not be able to function without its energy supply even for short periods of time.

2.3 Flicker

Flicker is defined as the impression of unsteadiness of visual sensations induced by a light stimulus whose luminance fluctuates with time. A typical example is the visible change in the brightness of a lamp due to rapid and repetitive fluctuations of the network voltage. These voltage fluctuations are typically caused by variations in load current passing through the source impedance of the electrical network upstream.

The repetitive active and reactive power cycles of the main power converters of a particle accelerator are a typical cause of flicker. The voltage drop caused by the load current flowing through the impedances of the upstream network has a major influence on the voltage amplitude and phase angle at a particular busbar. Depending on the network inductances and resistances upstream, as well as the amplitude of active and reactive power of the load, the voltage drop is calculated as follows:

$$\Delta U = RI\cos\phi + XI\sin\phi\,, \tag{1}$$

$$\frac{\Delta U}{U} = \frac{R.\Delta P + X.\Delta Q}{U^2}. \tag{2}$$

Equation (2) shows that any variation of load active and reactive power, as well as any change in network inductance or resistance, will result in a change in voltage drop and hence a variation of operating voltage at a given busbar. The most prominent example is the cycling power of thyristor converters for synchrotron accelerators.

The voltage fluctuations are defined as changes of r.m.s. voltage evaluated as a single value for each successive half-period of the network voltage. The short-term flicker indicator P_{st} specifies the severity of the flicker evaluated over a short period (e.g. 10 min); and P_{st} = 1 is the conventional threshold of irritability. The long-term flicker indicator P_{lt} defines the flicker severity evaluated over a long period (typically 2 h) using the cubic average of successive P_{st} values. Typically, the admissible long-term flicker factor is 60% of its short-term equivalent. Figure 1 shows the limits for a short-term flicker factor of 1.

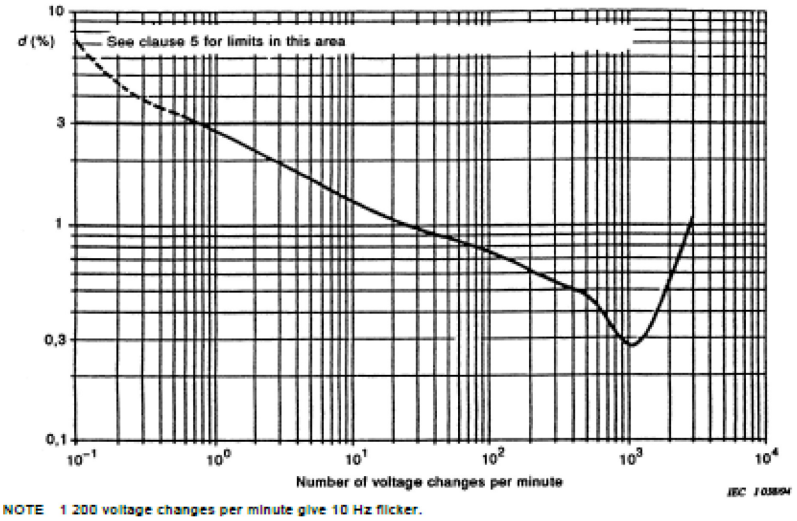

Fig. 1: Flicker limits for short-term flicker factor P_{st} = 1 (source: IEC 61000-3-3, Fig. 4)

These flicker limits are based on the empiric definitions of the human eye's sensitivity to luminance fluctuations. At the point of connection with the external network, the flicker level represents a contractual constraint and needs to be strictly respected.

The irritating effects of flicker can be reduced by applying a combination of the following measures:

- strictly separate general services and power converter loads;
- reduce the network impedance (increase short-circuit power) at the load busbar;
- reduce the amplitude of the (active and) reactive power variation;
- install technologies for flicker mitigation.

2.4 Fast transient overvoltages

Fast transient overvoltages (surges) are typically caused by lightning strikes into overhead lines, hence having a much lower probability in buried cable networks. They can also be caused by network switching operations, such as switching off large or small inductive loads, as well as short-circuits. The amplitude of fast transient overvoltages can easily reach multiples of the nominal system voltage, and hence they need to be taken into consideration for insulation coordination of the electrical network. For the power equipment itself, an appropriate choice of component voltage rating combined with simple mains input filters are suitable measures to obtain immunity against fast transient overvoltages.

2.5 Temporary power frequency variations

Temporary power frequency variations are less critical for most electrical equipment, and there are no specific countermeasures required.

The fundamental frequency of an electrical network is an expression of balance between power generation and consumption:

$$\mathrm{d}E_\mathrm{k}/\mathrm{d}t = P_\mathrm{g} - P_\mathrm{c}\ , \tag{3}$$

where E_k is the kinetic energy of all rotating machines ($= ½\, J\, \omega^2$); P_g is total generated power, P_c – total consumed power; J is the torque of the rotating machines; and ω is angular speed (rad/s).

The frequency of the European 400 kV network of the Union for the Co-ordination of Transmission of Electricity (UCTE) network is closely controlled, with typical fluctuations of only ±0.1 Hz around the nominal value of 50 Hz. The overall network power frequency characteristic of the 400 kV UCTE network is about 27 000 MW/Hz. As a simplified example (static point of view), an increase of power consumption by 270 MW would cause a drop in frequency of 10 mHz, if the power generation was not simultaneously increased.

Due to its three-level frequency control system, the large scale of generation systems, and the synchronous interconnection with other HV networks on a continental scale, the UCTE network has ample reserves to cope with load power variations under normal operating conditions.

However, in rare cases of breakdown of major interconnections and/or large groups of generation systems, the stability and continued operation of the entire network might be at risk. In such situations, the network operators could allow larger frequency variations in order to prevent runaways that would result in large-scale blackouts. In such exceptional situations the temporary frequency variations could be in the order of several hertz, being the result of larger imbalances between power generation and consumption.

2.6 Harmonics

Harmonics are conducted low-frequency disturbances of integer multiples of the system frequency. According to IEC standards [3–9], the total harmonic distortion is calculated taking into account all harmonics up to the 50th harmonic order.

The principal causes of harmonics in electrical networks are non-linear loads such as large thyristor power converters or diode rectifiers. During transformer energization, the transformer magnetizing currents (inrush) also generate significant temporary harmonic distortion.

The generated harmonic spectrum of thyristor power converters on the AC input side is as follows:

$$\text{Order of harmonics} = n \times p \pm 1 \ , \tag{4}$$

where n = 1, 2, 3… and p = 6- or 12-pulse converters.

Harmonic distortion typically changes only slowly over time for stable loads; however, for fast cycling loads such as pulsating particle accelerators they change rapidly during each power cycle. For rapidly changing harmonics the conventional definitions according to the IEC are not meaningful, and smaller time windows (e.g. 100 ms) for the calculation of the harmonic distortion need to be defined.

These harmonic currents create harmonic voltage drops when passing through the upstream network impedances, which are then superimposed upon the fundamental frequency network voltage. These are the most common techniques to reduce the harmonic levels in a network:

- strict separation of general services and power converter loads;
- reduction of source impedance (increase short-circuit power) at the load busbar;
- installation of passive or active harmonic filters (see Section 6.1.1).

2.7 Temporary overvoltage

A temporary overvoltage has a typical duration of 10–500 ms, and can occur during a single-phase earth fault in the healthy phase(s) of a medium voltage network with non-effectively grounded neutral. The voltage increase is typically between +30% and +70%. Temporary overvoltages also occur during the energization of large capacitor banks, where the capacitive inrush current passing through the inductances of the upstream network causes a temporary voltage increase. These overvoltages have a much shorter duration of 10–20 ms, and typical amplitude of up to +50%.

2.8 Voltage imbalance

In the event of a voltage imbalance, the fundamental frequency voltage amplitude or angle between phases are not equal for all three phases. The imbalance is usually expressed as the ratio of negative to positive sequence components, using the following approximation:

$$\text{Voltage imbalance} = \sqrt{6\frac{U_{12}^2 + U_{23}^2 + U_{31}^2}{U_{12} + U_{23} + U_{31}} - 2} \ , \tag{5}$$

where U_{12}, U_{23} and U_{31} are the fundamental frequency line–line voltages.

3 Power quality statistics

It is important to have a good understanding of the power quality of the electrical network. In particular, the duration and amplitude of voltage disturbances play a critical role in accelerator operating reliability. Statistics for the CERN electrical networks are presented below as an example [10].

3.1 Voltage dips

Table 1 shows the number of voltage dips recorded during the reference period (mid June–mid November) at CERN.

Table 1: Number of voltage dips recorded at different voltage levels (period mid June–mid November)

Network	Substation	Machine	Number of voltage dips
400 kV	BE	All of CERN	37
18 kV	EMD1/BE	SPS	104
0.4 kV	ERD1/8R	LHC	184

Network disturbances at the 400 kV level are usually seen also in the 18 kV and 0.4 kV networks, while disturbances generated at the 0.4 kV level do not propagate upwards into the HV networks.

Network disturbances at CERN that cause one of the accelerators to stop are called ‘major events’, and are marked in red in Figs. 2–4. Although there are only limited statistical data available, it seems that the duration of network disturbances is not the critical parameter for accelerator trip; rather, it is the voltage amplitude. The data also indicate that most disturbances causing major events originate from the 400 kV network. Figures 2–4 show the statistics for network disturbances over a reference period (mid June–mid November):

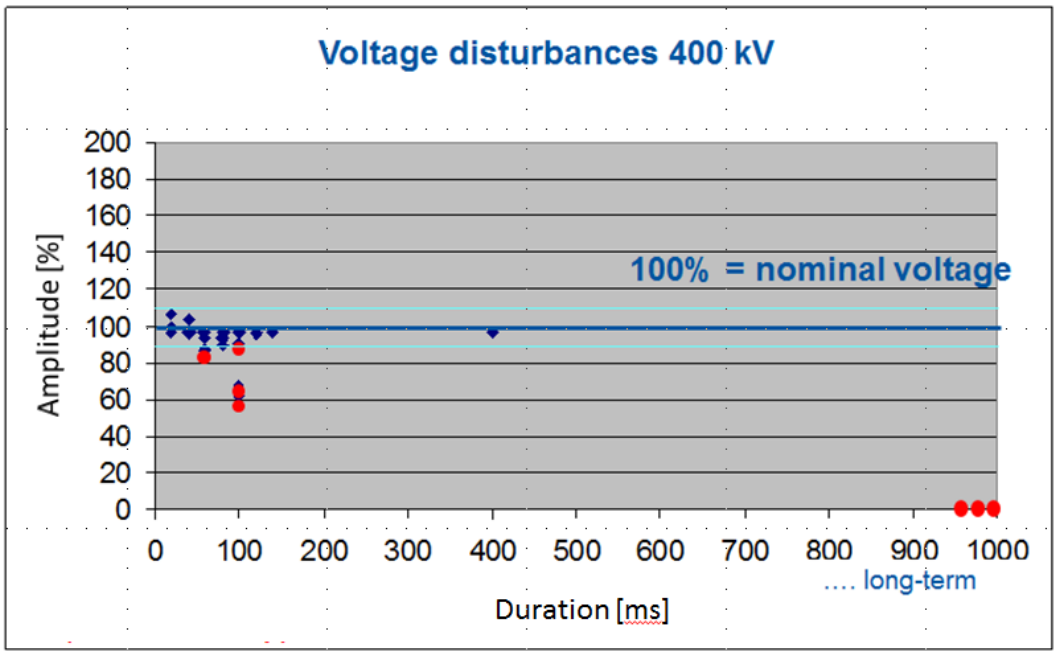

Fig. 2: Recorded disturbances in the 400 kV network. The events marked in red are major events, leading to a stoppage of an accelerator.

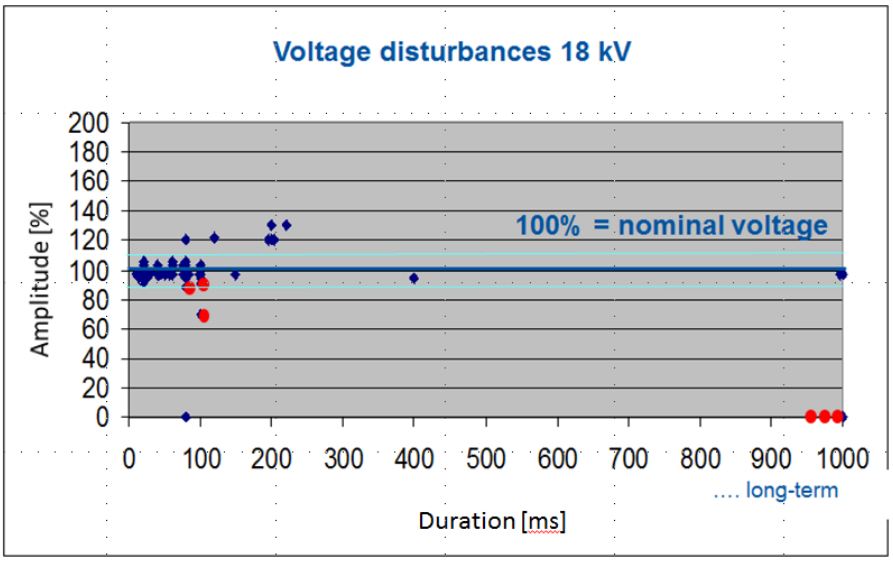

Fig. 3: Recorded disturbances in one of the 18 kV networks. The events marked in red are major events, leading to a stoppage of an accelerator.

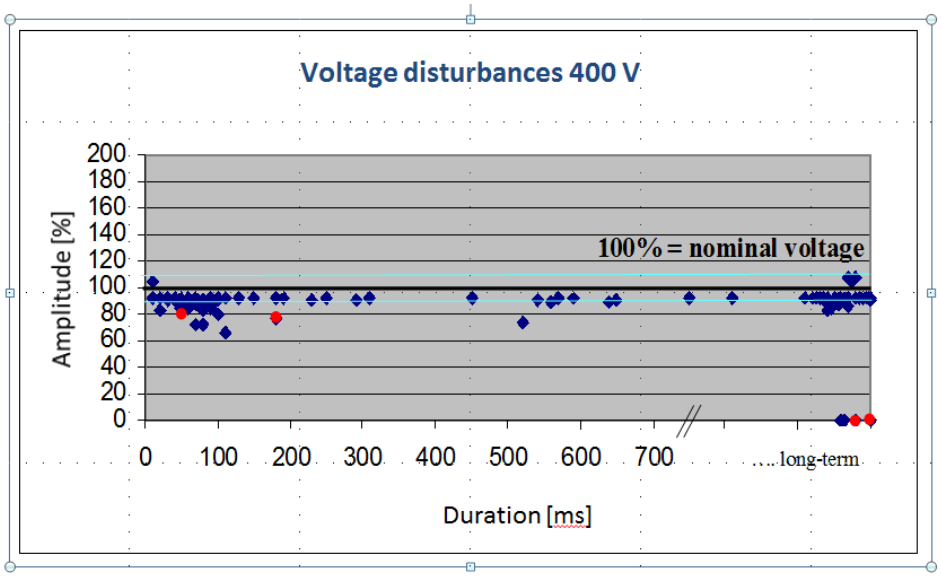

Fig. 4: Recorded disturbances in one of the 400 V networks. The events marked in red are major events, leading to a stoppage of an accelerator.

3.2 Propagation of external 400 kV voltage disturbances into the downstream voltage levels

Symmetrical 400 kV network disturbances propagate symmetrically into the subsequent (lower) voltage levels, and the relative amplitude of the disturbance remains the same for all voltage levels.

This article explains the propagation of asymmetrical 400 kV network disturbances into the downstream voltage levels, as found with computer simulations. All disturbances originating from the 400 kV network are transmitted to the lower voltage levels according to the vector groups of the transformers. Figure 5 graphically represents the vector relationships between the different voltage levels.

Based on the vector diagrams in Fig. 5, the asymmetrical disturbances propagate into the lower voltage levels (Tables 2, 3, 4 and 5). During this propagation, the faulty phase is partially recovering, while the healthy phases experience a decrease in voltage amplitude. Due to this effect, the symmetry

of the three phases is improved even during asymmetrical conditions. For example, a 50% voltage dip in phase R of the 400 kV network results in a 66% dip in phase T of the LV network, and 94% dips in phases R and S. The causes of this effect are the vector groups of the transformers and the reduction of zero sequence voltage components during the transformation 400/66/18 kV, and thus the symmetrization of the three phase voltages. During the transformation 18/0.4 kV there is no reduction of zero sequence voltage components (0.4 kV starpoint directly grounded) and thus no symmetrization effect.

Table 2: Propagation of single-phase voltage dip in 400 kV network, −50% in phase R

		R	S	T	R-S	S-T	R-T
400 kV		50%	100%	100%	75%	100%	75%
66 kV		58%	97%	96%	78%	100%	77%
18 kV		77%	100%	77%	95%	96%	65%
18/0.4 kV	0.4 kV	94%	94%	66%	100%	77%	77%
18/3.3/0.4 kV	3.3 kV	94%	94%	66%	100%	75%	78%
	0.4 kV	94%	94%	66%	100%	76%	76%

Table 3: Principle of propagation of single-phase voltage dip from 400 kV to 0.4 kV

Voltage level	Faulty phase
400 kV	R
66 kV	R
18 kV	R-T
3.3 kV	T
0.4 kV	T

Table 4: Propagation of double-phase dip in 400 kV network, −50% in phases R and T

		R	S	T	R-S	S-T	R-T
400 kV		50%	97%	50%	76%	76%	50%
66 kV		57%	87%	58%	76%	76%	50%
18 kV		76%	76%	50%	83%	60%	60%
18/0.4 kV	0.4 kV	83%	60%	60%	77%	50%	77%
18/3.3/0.4 kV	3.3 kV	84%	66%	64%	77%	53%	77%
	0.4 kV	83%	65%	65%	78%	54%	78%

Table 5: Principle of propagation of double-phase voltage dip from 400 kV to 0.4 kV

Voltage level	Healthy phase
400 kV	S
66 kV	S
18 kV	R-S
3.3 kV	R
0.4 kV	R

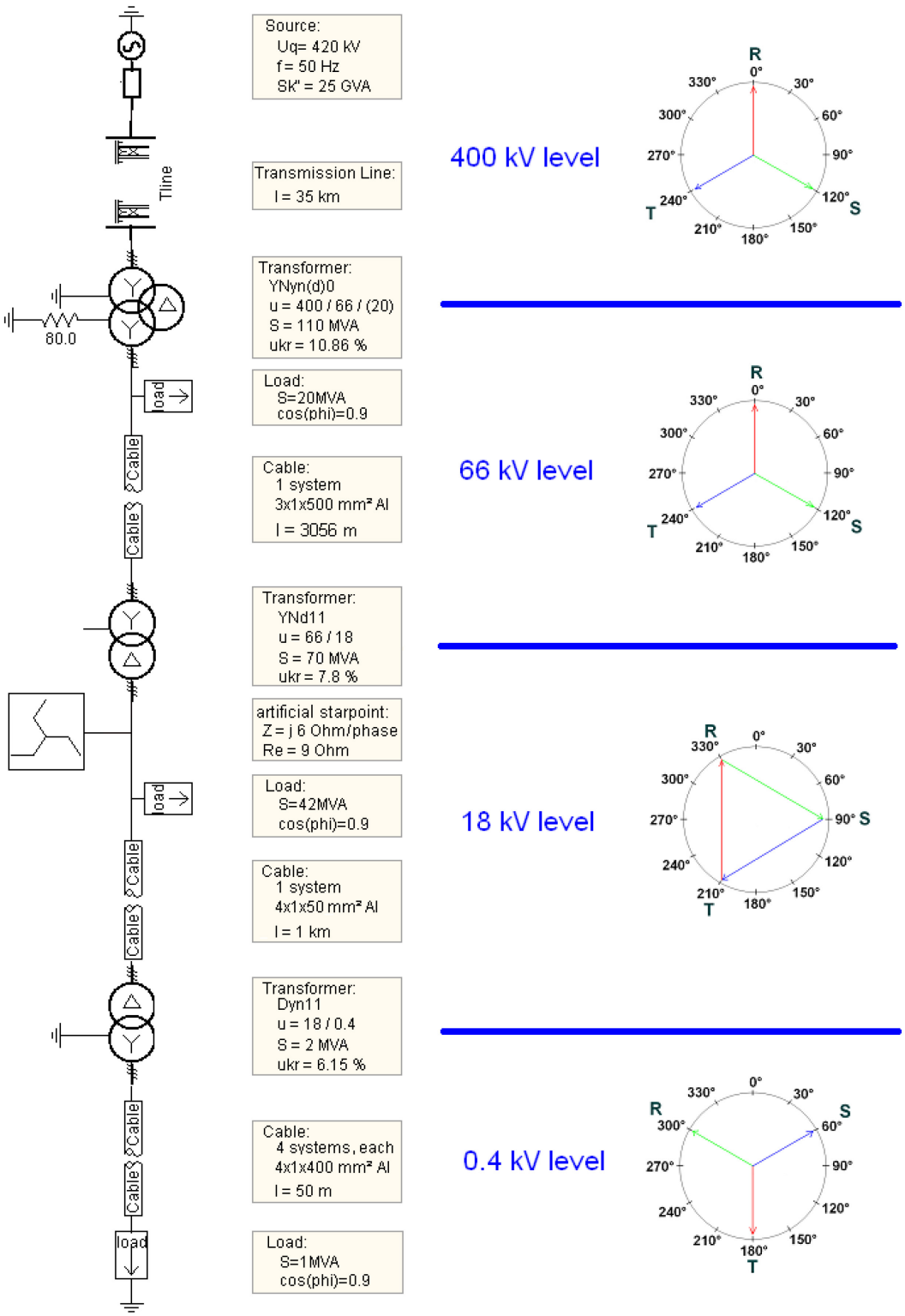

Fig. 5: Simplified CERN network and vector relations between voltage levels

In the case of a single-phase interruption of the 400 kV network, the voltage in the faulty phase remains close to 100% due to the 400/66 kV vector group YNyn with delta compensation winding. In this case, the compensation winding provides the magnetizing flux for the missing phase such that the voltage remains close to 100% (Table 6).

Table 6: Propagation of single-phase interruption 400 kV (after opening of breaker, phase R)

	R	S	T	R-S	S-T	R-T
400 kV	(97%)	100%	100%	100%	100%	100%
66 kV	91%	102%	95%	100%	100%	89%
18 kV	99%	100%	89%	103%	93%	92%
0.4 kV	103%	94%	91%	100%	89%	98%

Single-phase short-circuits on the 400 kV overhead line from Genissiat to BoisTollot caused, for example, by a flash-over due to lightning strike, result in a single-phase voltage dip in the faulty phase and an increase of voltage amplitude in the two healthy phases. The voltage rise of the healthy phases is related to the distance, and increases if the short-circuit happens closer to CERN. For a single-phase short-circuit directly at BoisTollot, the impedance ratio Z_0/Z_1 is the highest; and the worst-case voltage increase in the healthy phases could reach up to +17% (voltage phase–ground) when CERN is only supplied from Genissiat 400 kV. In the case of parallel infeed from Genissiat and Chamoson, the voltage rise in the healthy phases is +11% during a single-phase short-circuit. Again, the propagation into CERN follows the vector relationships as described above.

3.3 Harmonic voltage distortion

Repeated measurements of harmonic distortion were done in different 0.4 kV substations in CERN's electrical distribution network, showing that in all network supplied substations the harmonic distortion remained below 5%, corresponding to IEC 61000-2-2 (class 1). Generally, harmonics are lowest in switchboards for general services (EBDxx/xx). Higher harmonic voltage distortions are present in switchboards supplying rectifier loads (ERDxx/xx). At one UPS-supplied EODxx/xx switchboard, a harmonic distortion of 8% was measured. Figure 6 shows the total harmonic voltage distortion (THD) measured at different LV substations at CERN during accelerator operation.

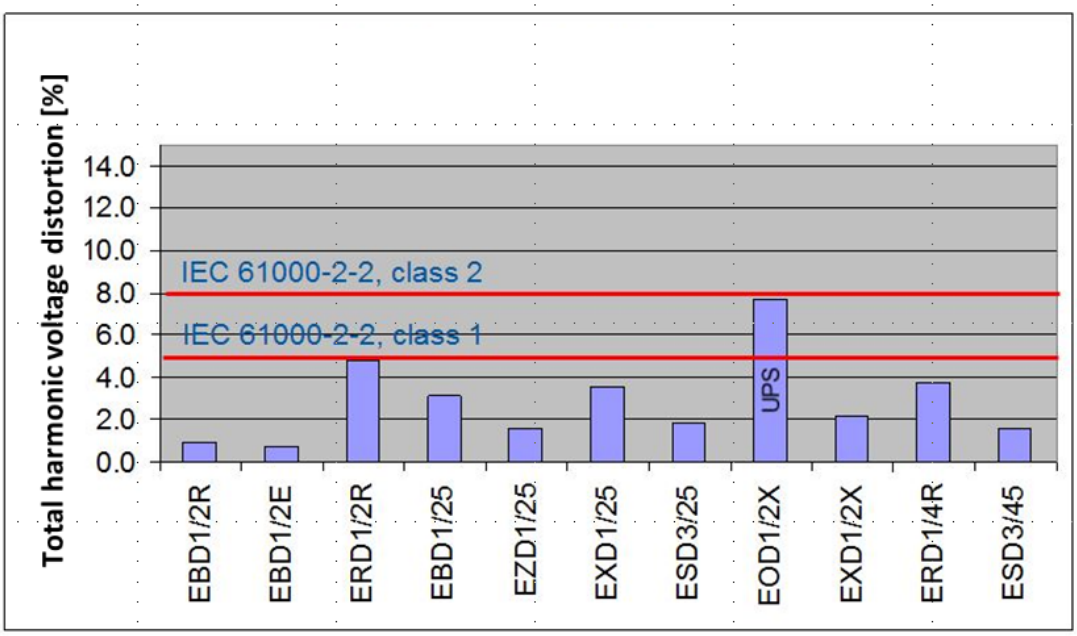

Fig. 6: Measured harmonic distortion at different LV substations

4 Electromagnetic environment classes

The electromagnetic environment classes are defined by IEC 61000-2-4:

– class 1: protected supplies for compatibility levels lower than those on public networks… for very sensitive equipment;

- class 2: environments of industrial and other non-public power supplies… and generally identical to public networks;
- class 3: industrial environments, in particular when a major part of the load is power converters and/or the load varies rapidly (e.g. particle accelerators!).

Table 7 quantifies what these three classes actually mean, and also compares them with the LHC Engineering Specification for LV networks [11] and the example of a static Var compensator (SVC) from the SPS machine network.

Table 7: Parameters of the electromagnetic environment classes (IEC 61000-2-4)

	Class 1	**Class 2**	**Class 3**	**LHC Engineering Specification [11]**	**Example: SVC for SPS (18 kV)**
Voltage tolerances	±8%	±10%	−15%/+10%	Typical ±5%, maximum ±10%	±0.75% (transient)
THD (400 V)	5% (short-term 7.5%)	8%	10% (short-term 15%)	Typically 2%, maximum 5%	0.75% (transient)
Frequency tolerances	±1 Hz	±1 Hz	±1 Hz	±0.5 Hz	±0.5 Hz

Power converters for particle accelerators represent the roughest type of load, comparable to heavy industry such as large arc furnaces, rolling mills, etc. (class 3). However, to operate them correctly and with the required precision, power converters for particle accelerators require power quality levels sometimes better than the most sensitive equipment (class 1)!

The most common technologies for power quality improvement, used for particle accelerators, are explained in the second part of this publication.

5 Definition of immunity levels for equipment (LHC Engineering Specification)

Based on the statistics for past network disturbances, combined with considerations of technical feasibility, the minimum immunity levels for electrical equipment were defined before the beginning of LHC construction [11], covering the main parameters of CERN's low voltage systems, their variations, and power quality issues. Users' equipment should be designed to correctly function within the limits detailed in Table 8.

Table 8: User equipment specifications

Nominal voltage	400 V/230 V
Maximum voltage variations	±10%
Typical voltage variations	±5%
Transients (spikes)	1200 V for 0.2 ms
Voltage swells	+50% of U_n, 10 ms
Voltage dips	−50% of U_n, 100 ms
Total harmonic voltage distortion (THD)	5%

These voltage limits are visualized in Fig. 7:

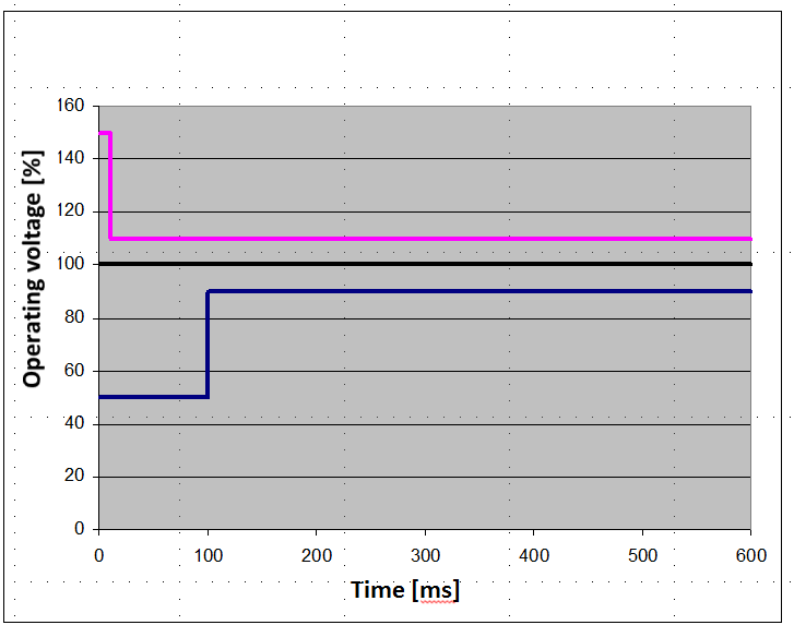

Fig. 7: Immunity levels for voltage disturbances as per the engineering specification for LV networks

6 Technologies for power quality improvement

This article discusses measures and technologies used in accelerator networks for power quality improvement. Particular focus is given to the improvement of power quality in networks supplying cycling loads.

6.1 Systems without integrated energy storage

6.1.1 Static Var compensators

Static Var compensators (SVCs) are part of a larger classification of equipment called flexible AC transmission systems (FACTS). An SVC typically consists of a combination of harmonic filters for the generation of (capacitive) reactive power and for harmonic filtering, as well as thyristor controlled reactors (TCR) to allow for the control of variable reactive power output. Figure 8 shows a very simplified topology for an SVC, consisting of a fixed capacitance (e.g. harmonic filters) and a TCR [12, 13].

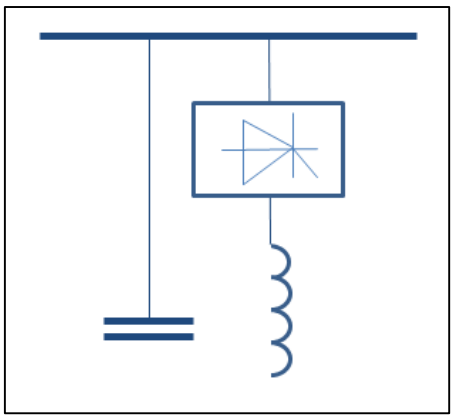

Fig. 8: Very simplified topology of an SVC

Optimum performance is achieved by connecting the SVC to the same MV substation as the cycling power converter load, typically directly downstream of the feeding HV/MV transformer. In most cases, the MVar ratings of the harmonic filters and of the TCR are identical; however, for certain applications a slightly increased TCR might be an interesting option.

The current in capacitor banks (or harmonic filters) cannot be continuously controlled by thyristors; capacitors can only be switched on or off, e.g. by means of thyristors or mechanical switches. The step-wise switching of individual capacitor banks (or harmonic filters) would generate transient overvoltages and other disturbances in the electrical network, which could potentially disturb the operation of the particle beam. Instead, and to follow the cycling reactive power of the load, the current in the thyristor-controlled reactors is adapted continuously by variation of the firing angle of the thyristors. Therefore, the capacitor banks (or harmonic filters) permanently generate a constant amount of reactive power, while the TCR follows the load pulse. As shown in Fig. 9, the reactive power of the TCR is controlled in the opposite way with respect to the reactive power cycles of the load: during the flat top of the load cycle the TCR current is low, and during low load the TCR current is at maximum. Figure 19 shows the qualitative functions of reactive power, while Fig. 13 represents measurements of a real system.

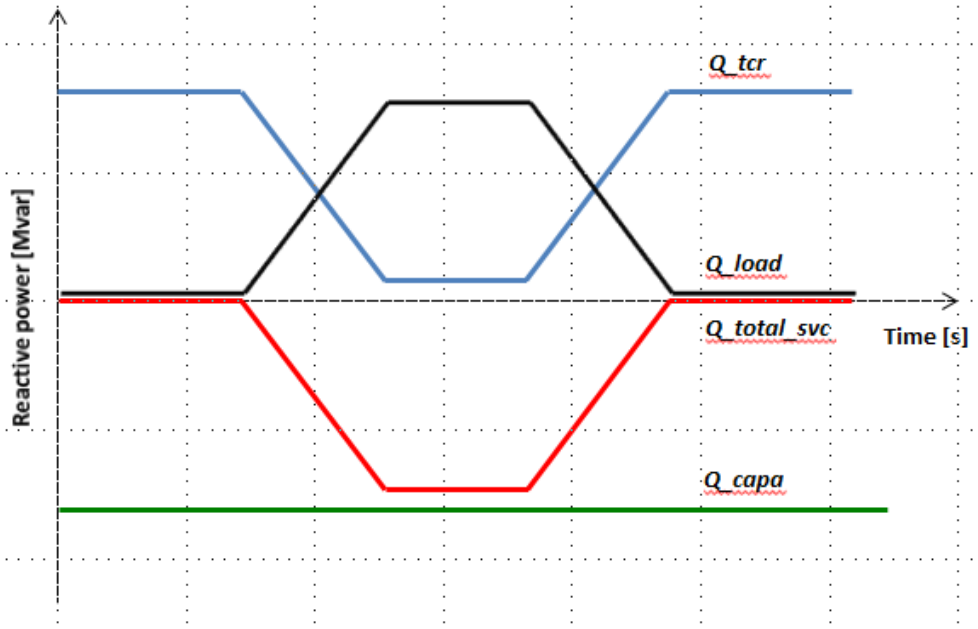

Fig. 9: Reactive power control of an SVC

It is a common misperception that SVCs store energy that is then used for the accelerator magnet load cycles. This is not the case! The reactive power circulation between the SVC (MVar generation) and the magnet power converters (MVar absorption) is a pure 50 Hz AC phenomenon, and no energy is stored or recovered between power cycles beyond one fundamental AC period of 20 ms.

An SVC cannot assure perfect voltage stabilization and perfect reactive power compensation at the same time. For most particle accelerators, power of the highest quality precedes the need for perfect reactive power compensation. The variable reactive power output of the SVC therefore needs to compensate not only the cycling reactive power of the load, but also correct the voltage variations caused by the cycling active power. Equation (6) defines the required reactive power function of the SVC.

$$Q_{\mathrm{SVC}} = Q_{\mathrm{load}} + \frac{P_{\mathrm{load}}^2}{2S_{\mathrm{cc}}} + kP_{\mathrm{load}}\,, \tag{6}$$

where $k = R/X$ of the network.

6.1.1.1 Harmonic filter design

The total number of capacitors required for reactive power compensation are split into groups and then connected in series with air-core reactors to achieve the required harmonic tuning. The harmonic filters need to be designed taking into account the three major sources of harmonics:

- the 12-pulse thyristor power converter load (harmonic current source where n = 11, 13, 23, 25);
- the TCR (harmonic current source where n = 5, 7, 11, 13, 17, 19);
- the supplying external network, which is a harmonic voltage source typically where n = 5 and 7 in steady-state, and n = 3 during transients.

The harmonic filters are tuned precisely to their corresponding harmonic frequency by adjusting the taps on the air-core filter reactors. Equation (7) calculates the resonance frequency of an L-C circuit:

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{L_{\text{filter}} C_{\text{filter}}}} \ . \tag{7}$$

The total quantity of the capacitors will create a parallel resonance with the inductances of the supplying network. Equation (8) calculates the frequency of this parallel resonance:

$$f_{\text{res}} = f_0 \sqrt{\frac{S_{\text{cc}}}{Q_{\text{SVC}}}} \ . \tag{8}$$

For reliable SVC operation under all steady-state and transient conditions, the impedance of this parallel resonance needs to be controlled carefully. For large SVCs, it is typically in the range of 100–150 Hz, and hence would introduce instabilities during transient conditions. The installation of damped second and/or third harmonic filters can prevent or reduce amplification of these harmonics.

Based on the discussion above, an SVC for particle accelerators should hence consist of harmonic filters for n = (2, 3,) 5, 7, 11, 13 and high-pass. A typical topology is shown in Fig. 10. An impedance diagram for the harmonic filter topology shown in Fig. 10 is given in Fig. 11.

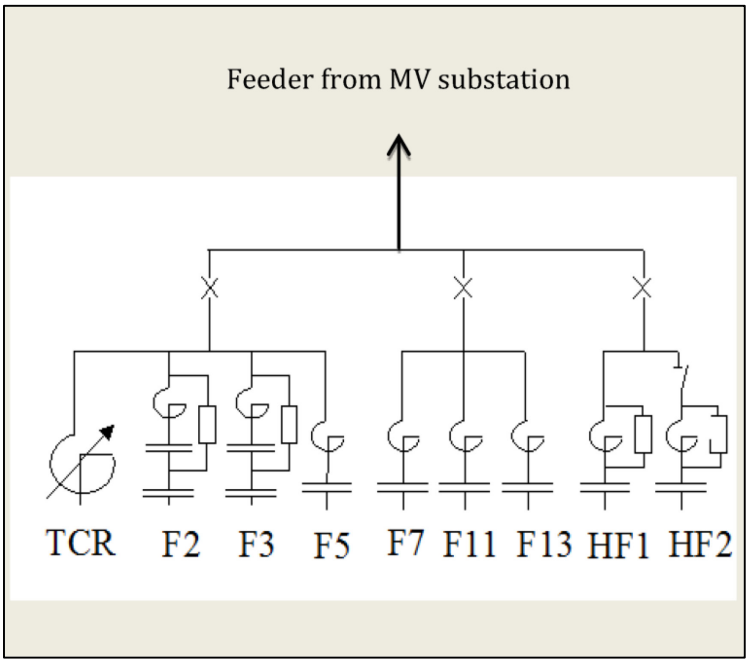

Fig. 10: Typical topology of an SVC for a particle accelerator

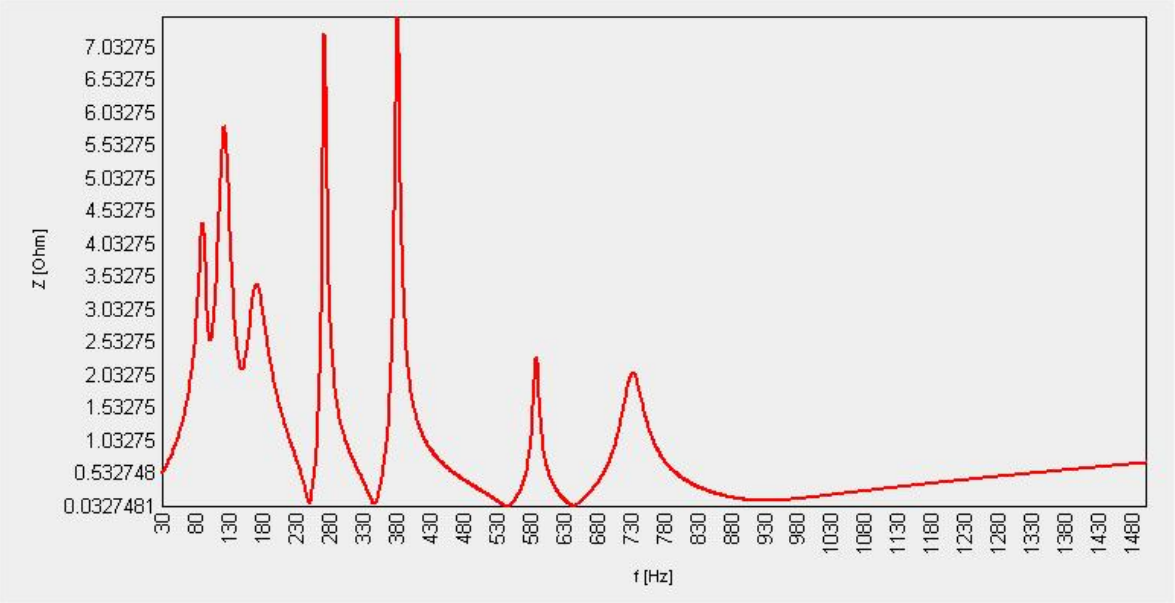

Fig. 11: Impedance diagram for the harmonic filter topology shown in Fig. 10

6.1.1.2 Control system

A typical SVC control system consists of a proportional integral (PI) AC voltage feedback controller and a direct compensation of disturbance to improve transient responses. As shown in Fig. 12, it includes three signals: load reactive power (Q_{load}), load reactive power differential (dQ_{load}/dt), and load active power (P_{load}), with all load variables being measured on the AC side of the power converter.

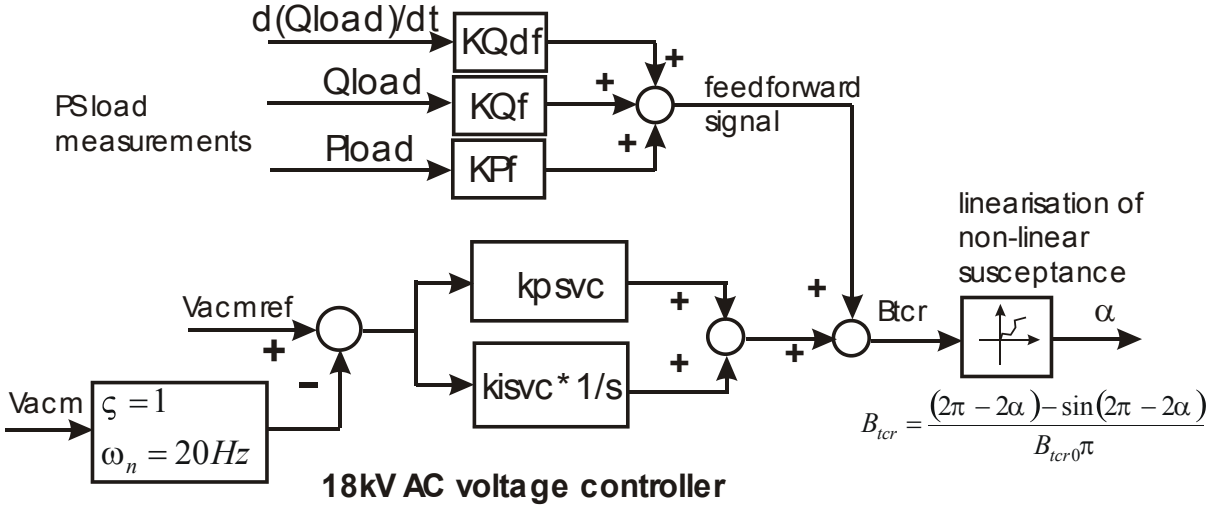

Fig. 12: Typical TCR control system

6.1.1.3 SVC performance

Typical SVC performance is discussed below, based on the example of the SPS accelerator. Figure 13 shows the cycles of active and reactive power for the load, the SVC, and the supplying network.

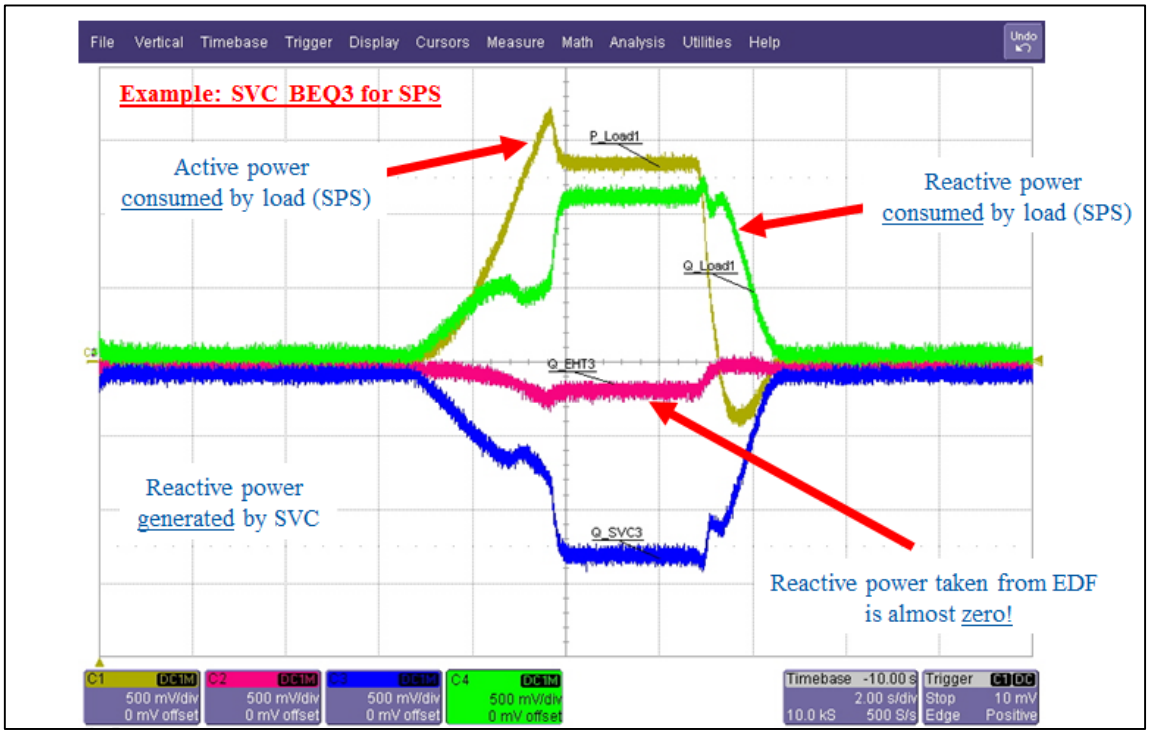

Fig. 13: Measured active and reactive load power cycles and reactive power output of the SVC (scale: 30 MW/MVar per division).

A well-tuned harmonic filter design as presented above would typically keep the THD of the bus voltage at the SVC connection point below 1%, during all phases of the cycling load pulse. Figure 14 shows the harmonic voltage distortion during the flat top of the cycle.

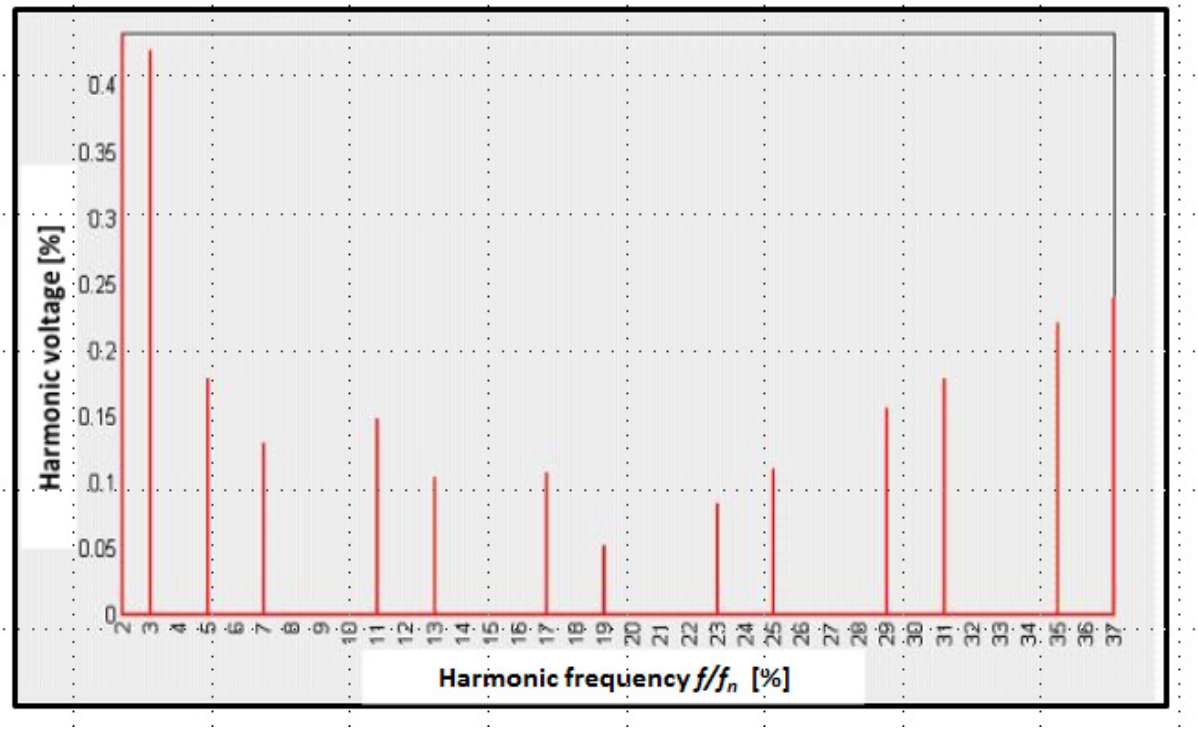

Fig. 14: Typical harmonic performance of an SVC with six harmonic filters, during flat top

The transient performance of the SVC response greatly depends on the response time of the control system, and also on the amplitude, shape, and rate of rise/fall of the active and reactive load cycles. Typically, the response time of an SVC is 50–100 ms. Figure 15 shows the measured voltage response of CERN's 18 kV network during SPS operation, with the SVCs in service. The voltage variations are within a limit of ±0.3% for most parts of the load cycle, and within ±0.75% during the transition points at the beginning and end of the load cycle.

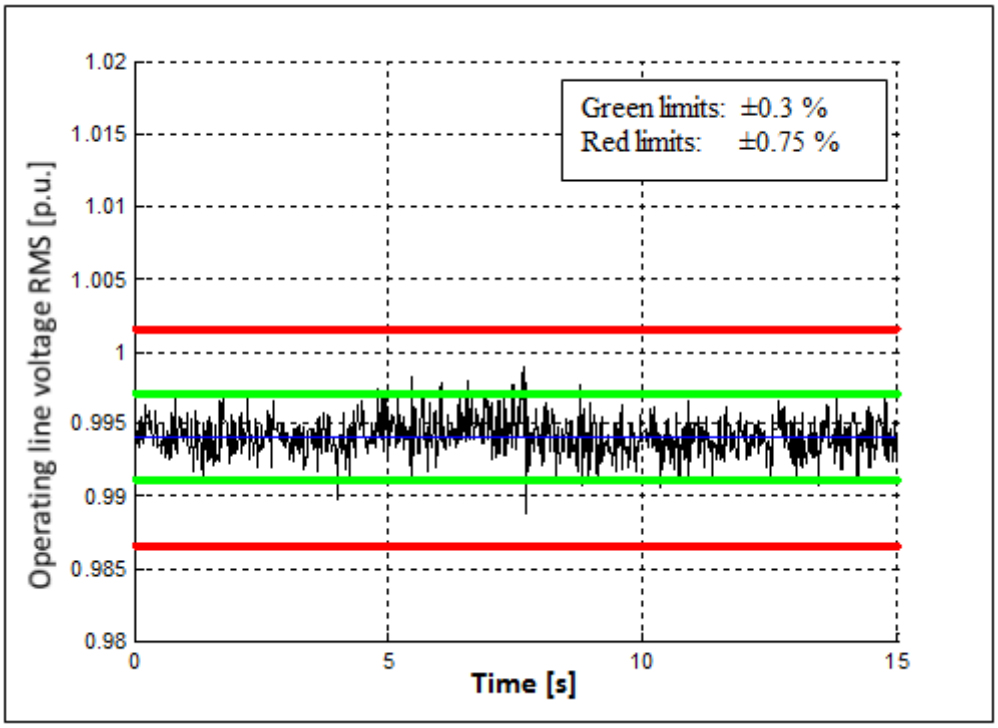

Fig. 15: Typical voltage response of an SVC compensating a large cycling load (e.g. SPS)

6.1.2 Static synchronous compensator without energy storage

A static synchronous compensator (STATCOM) without energy storage covers functions similar to an SVC. Due to its switched-mode technology, its performance for voltage stabilization is superior when compared to an SVC. It is therefore an interesting technology for very fast cycling applications.

6.2 Systems with integrated energy storage

6.2.1 Power converters with integrated DC capacitor energy storage

A novel approach for the decoupling of the load from the electrical network is the installation of power converters with integrated energy storage. The most prominent example of this technology is the new power supply for the PS (POPS) [14-16].

The POPS system consists of two active front end (AFE) rectifiers supplied from the 18 kV AC network, and six DC/DC converters. Associated with each DC/DC converter is one large DC capacitor bank for energy storage.

The six DC/DC converters are connected to the power system in two ways: two of them, being directly connected to the output of the two AFE's, are so-called 'chargers'. The four other DC/DC converters are 'floating'. The power part of these six DC/DC converters is identical; however both types of converters are controlled differently. Figure 16 shows the topology of the POPS system.

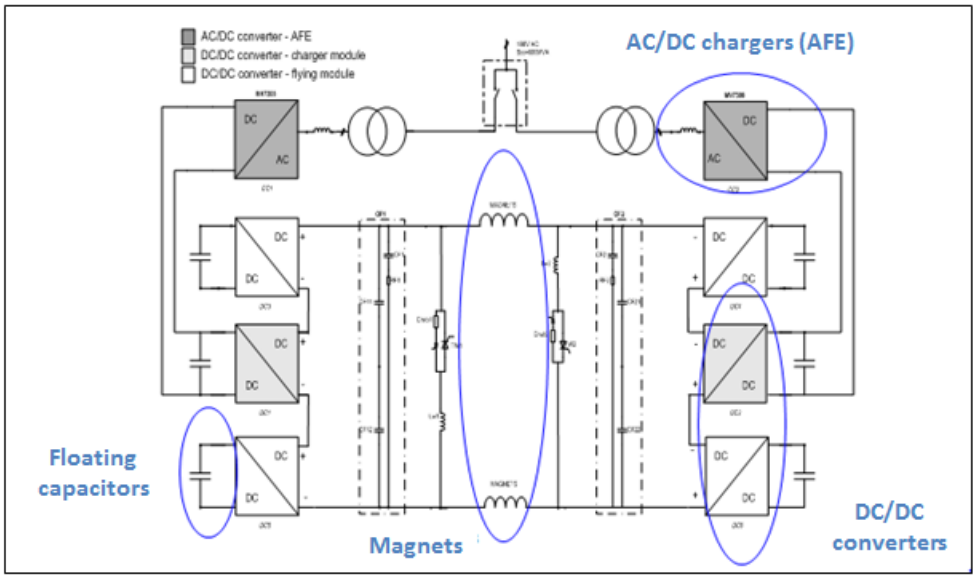

Fig. 16: POPS topology

On its DC output side POPS provides the current cycles required for the PS magnets (10 kV peak/6 kA peak). At the beginning of each cycle the DC storage capacitors are fully charged. During the load cycle they discharge, and then finally they recover a major part of the energy during the ramp-down of the accelerator magnet current towards the end of each cycle.

The two AFEs only cover the electrical losses of the power converters and accelerator magnets. To the electrical network, they represent an electrical load with a power factor of unity, and with only small variations in amplitude. As a consequence, the system does not generate any noticeable flicker in the electrical network.

The principal advantage of POPS is its modular design. Several degraded modes are integrated into its topology, permitting the filling of the LHC beam in the event of the failure of one power transformer, one AFE, or one DC/DC converter.

The POPS AFE and DC/DC converters are installed inside a dedicated power converter building. The cast-resin power transformers are installed outdoors, in metallic enclosures. The DC storage capacitor banks are installed in six sea shipping containers. A photograph of the POPS system is given in Fig. 17.

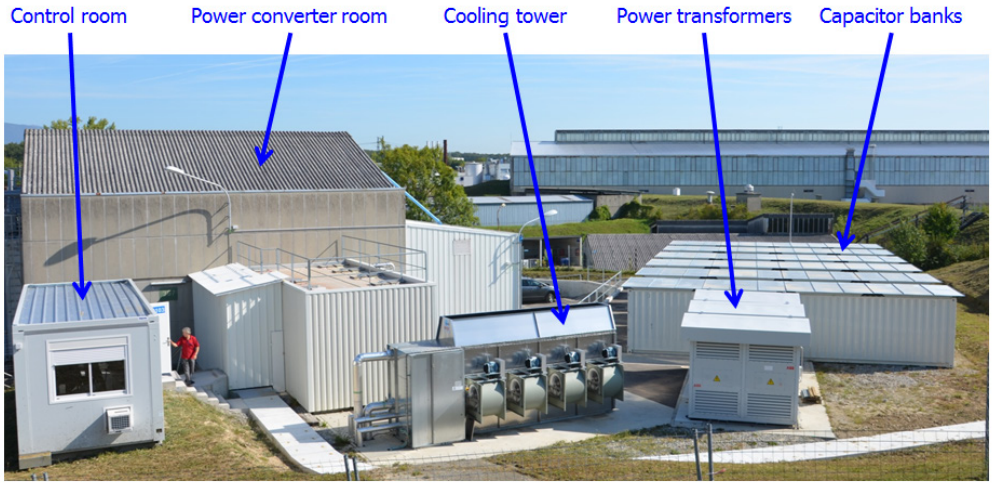

Fig. 17: POPS

Figure 18 shows the output voltage and current of POPS over one load cycle. One can distinguish three phases. During the ramp-up of the current (first phase), POPS operates at maximum output voltage. In the second phase, the current flat top, the voltage drops down to only cover the resistive losses of the magnets. Finally, during the third phase, the voltage is inversed to ramp down the current as quickly as possible. This inversion of voltage, while the current is still positive, corresponds to an inversion of power flow (from the magnets to the POPS system).

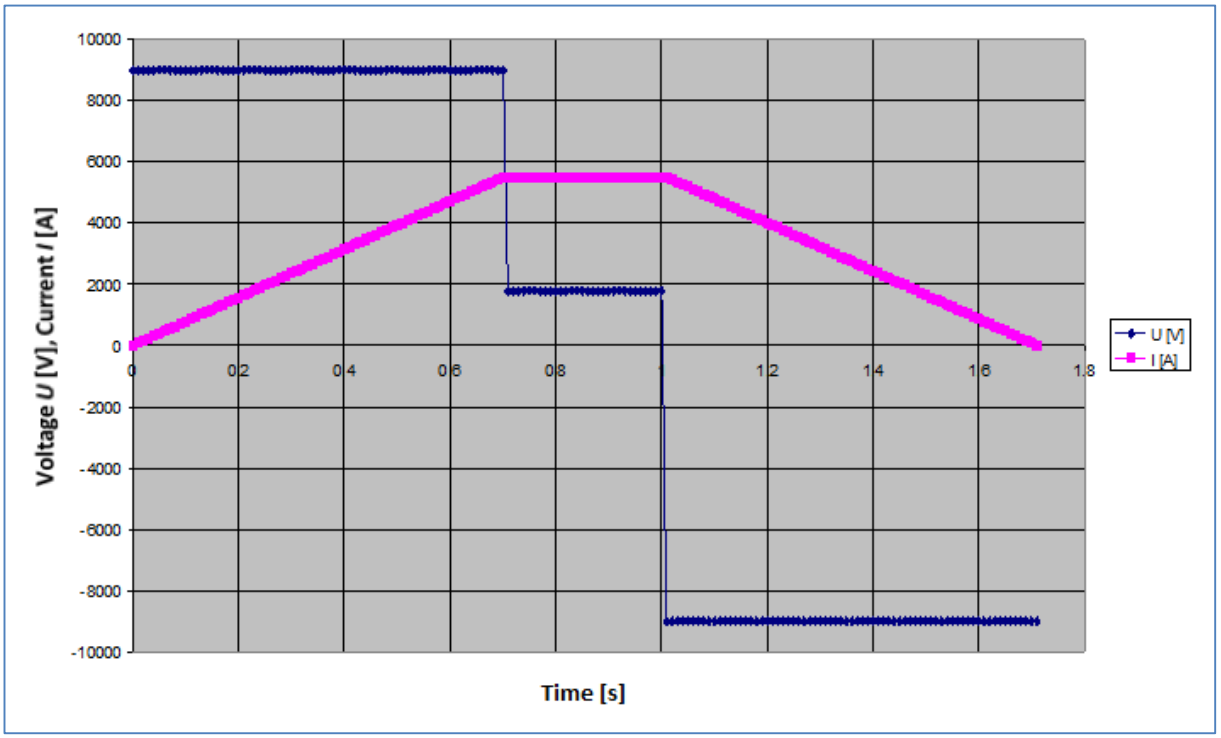

Fig. 18: POPS voltage and current output cycle

Figure 19 shows the active power cycle of the PS magnets, with a peak value of ±50 MW.

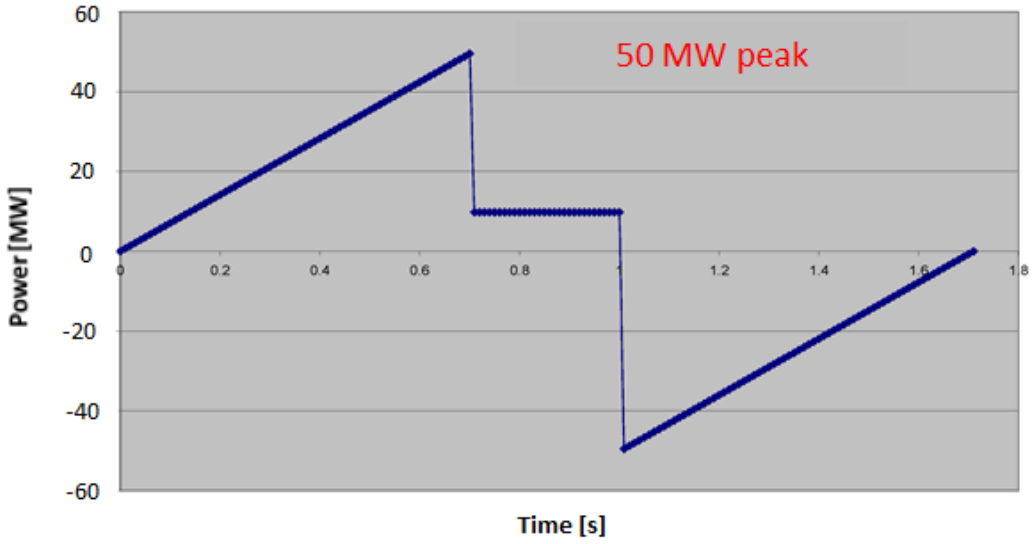

Fig. 19: Active power of the magnets

Figure 20 shows that the capacitors are fully charged at 5 kV DC at the beginning of the load cycle. They discharge during the power cycle and then recharge when the energy is fed back from the magnets to the POPS system.

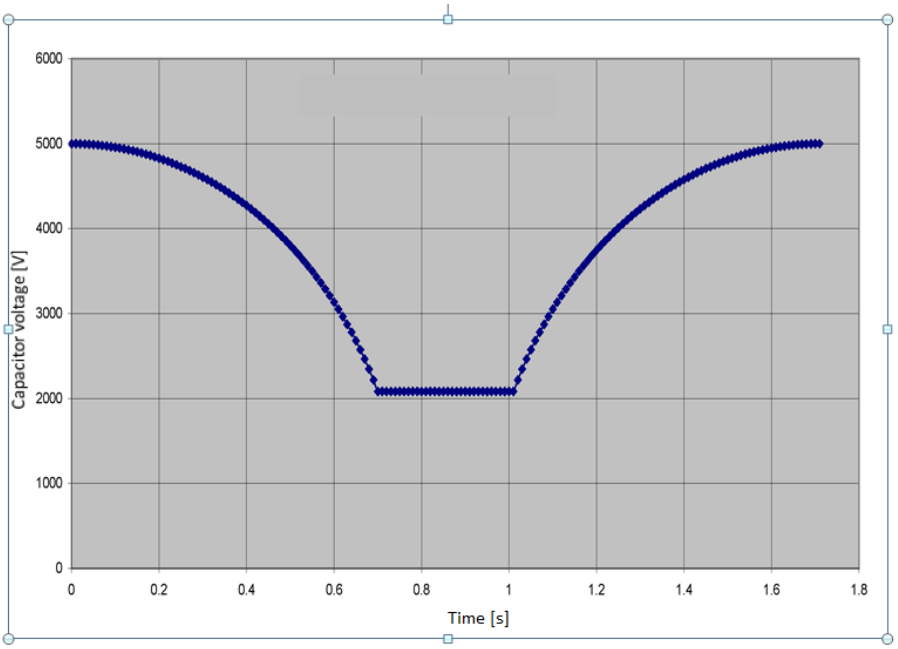

Fig. 20: Voltage profile of POPS DC storage capacitors during one load cycle

6.2.1.1 Converter topology

The AFE and DC/DC power converters consist of standardized industrial drives. To obtain the required current rating of 6 kA, three legs, each rated at 2 kA, are connected in parallel via coupling inductors. Each leg represents a three level neutral point clamped (NPC) branch.

Each AFE consists of one three-legged unit. Each DC/DC converter is an H-bridge with a three NPC leg unit on either side of the bridge for positive and negative polarity, as shown in Fig. 21. Each NPC leg consists of four insulated-gate bipolar transistors (IGBTs) and six diodes. The switching structure is supplied by two capacitors charged to $V_{dc}/2$. Each NPC leg allows the application of three voltage levels at the output ($V_{dc}/2$, 0, $-V_{dc}/2$).

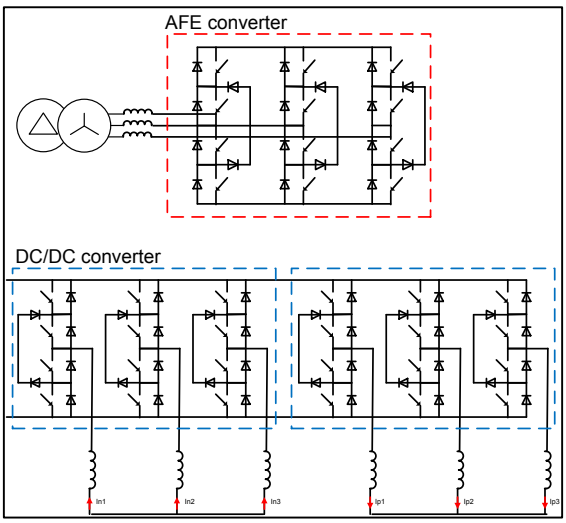

Fig. 21: AFE and DC/DC converter topologies

The different legs are interleaved, as are the converters, in order to increase the equivalent output ripple frequency, to reduce the size of the output filters, and to obtain better dynamics of the output voltage. For PS particle beam operation, the minimization of current ripple in the magnets is very critical. By using the principle of interleaving, an equivalent switching frequency of 4 kHz is obtained by using a basic switching frequency of 333 Hz for each individual leg. The interleaving between legs is obtained by shifting the modulation index of each leg by $2\pi/3$.

By using this topology, it was possible to assemble the entire POPS system by combining 14 standard industrial motor drives of 3.3 kV, 8 MW.

6.2.1.2 Choice of semiconductors

The PS represents a cycling load with a period of 1.2 s. POPS is specified for a lifetime of 15 years, corresponding to 100 million power cycles. The cycling character of the load is particularly important when choosing the type of semiconductor: the thermal time constant of the junction is in the order of 100 ms. During each load cycle longer than a few multiples of this time constant, the electrical connections to the junction will experience a certain ageing process due to thermal expansion. The prospective life time of the IGBT is a function of two conditions: the amplitude of junction temperature variation and the number of thermal cycles. Classical IGBTs, using very fine wire bonding for their electrical connections, are very susceptible to premature ageing due to these thermal cycles. Press-pack IGBTs, on the other hand, are a much better choice for cycling applications because they have no internally bonded wires. Here the internal electrical and thermal connections are done by applying very high compression forces by means of a clamp.

6.2.1.3 Energy storage DC capacitor banks

Each of the six capacitor banks has a rating of 0.25 F, 5 kV, and consists of 126 capacitor units in parallel. Each capacitor bank is installed inside a standard sea shipping container. The containers are air-conditioned to assure controlled ambient operating conditions for the capacitor banks. Figure 22 shows the inside of one of the containers.

Fig. 22: Photo of one of the six DC storage capacitor banks inside its container

The DC capacitors are dry capacitors with polypropylene (PP) film. Small dielectric defects of the PP film are automatically repaired by ‘self-healing’, e.g. evaporation of the metalized electrode material around the dielectric defect. As an additional protection, in particular for major cases of capacitor failure, the capacitor bank is equipped with a fuse and an automatic discharge system.

6.2.1.4 Performance

Accuracy in B-field regulation is of particular importance during particle injection into and extraction from the PS. Figures 23 and 24 show the magnetic field in the dipole magnets during one load cycle.

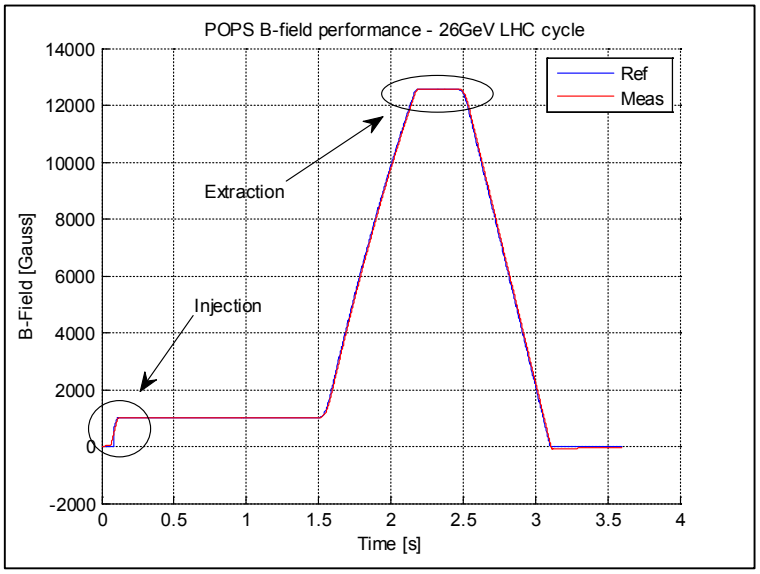

Fig. 23: POPS B-field regulation

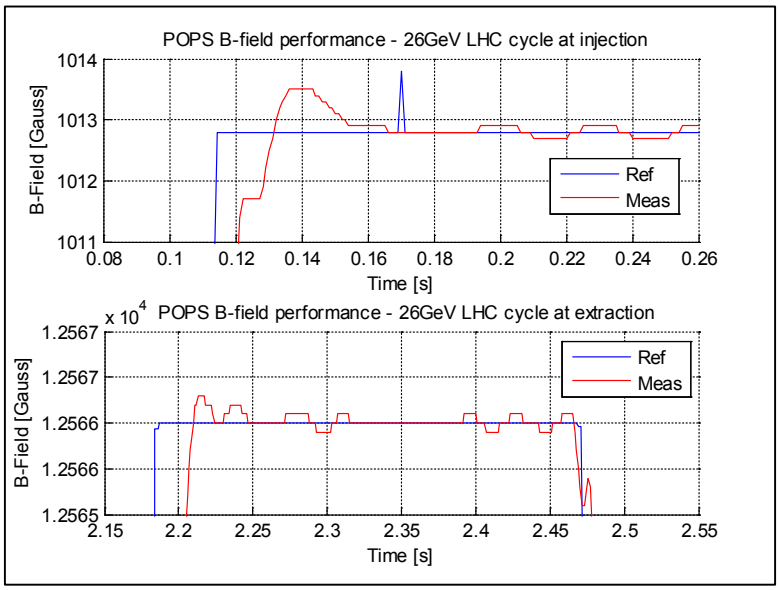

Fig. 24: Zoom of POPS B-field regulation

The digital RST controller reduces the error in magnetic field regulation of the magnets to 0.5 Gauss over an absolute value of 12000 Gauss, corresponding to an overall precision of 40×10^{-6}.

6.2.2 Rotating machines for large cycling loads

Another possibility for decoupling a cycling load from the electrical network, and to reduce flicker in the network, is the supply of a particle accelerator machine network via a rotating machine. This configuration is used for the AGS machine at BNL, and the PS rotating machine, which was in operation for 40 years before the commissioning of POPS.

A motor drives a large synchronous generator that supplies the cycling power converter load. Due to the kinetic energy stored in the rotation of the motor-generator set, the power drawn from the electrical network by the motor follows the accelerator cycles with relatively small power variations.

These systems have reliably operated for many years; however they always represent a considerable risk as a single point of failure. A major failure of the rotor could easily stop the operation of the machine for at least six months. Figure 25 shows a single-line diagram of the PS rotating machine at CERN, while Fig. 26 gives one of its typical load cycles.

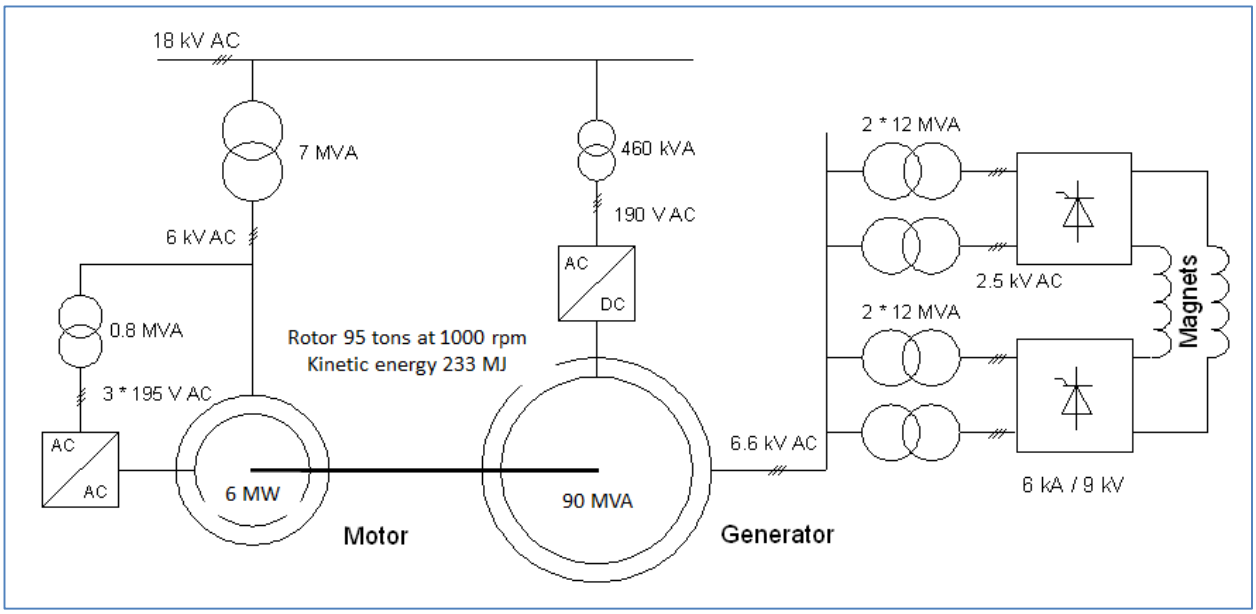

Fig. 25: Single-line diagram of the PS rotating machine at CERN

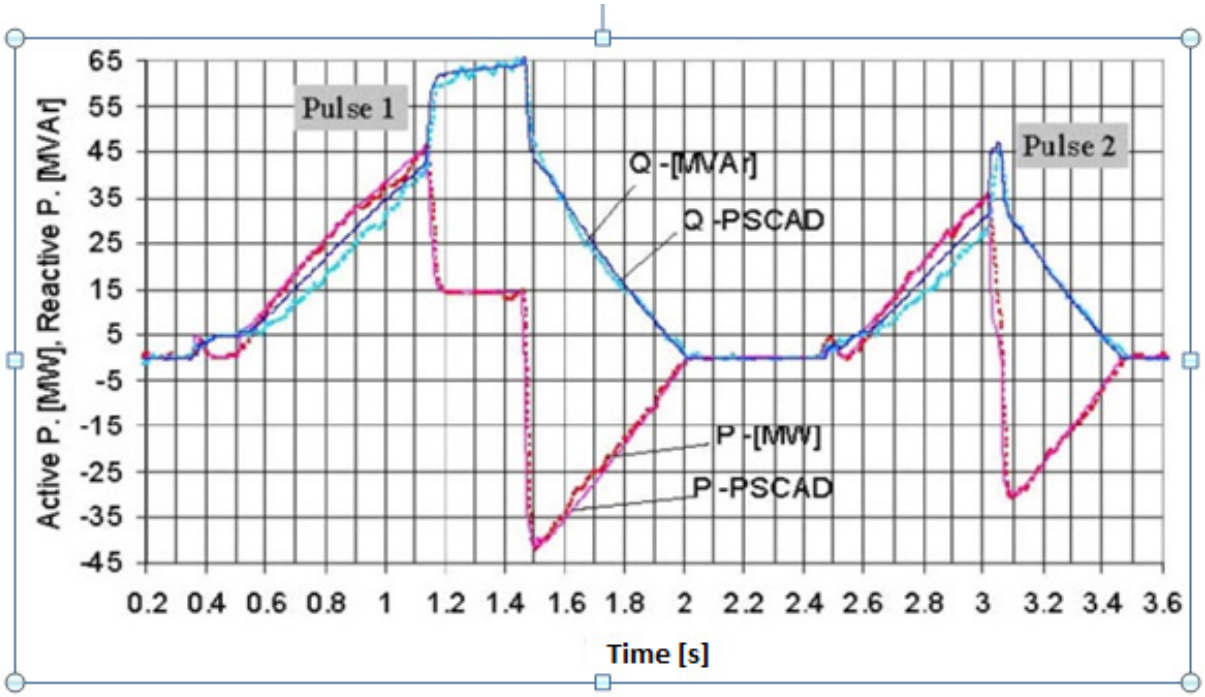

Fig. 26: Typical active and reactive power cycle of the PS main power converter

(a) (b)

Fig. 27: (a) AGS machine at BNL; (b) PS machine at CERN

6.2.3 Flywheel system to compensate external network disturbances

Physics laboratories often suffer from electrical network disturbances, and many of these events result in particle accelerator stoppages. Due to its geographical location in Grenoble, surrounded by the French Western Alps, ESRF is particularly exposed to disturbances caused by thunderstorms, which are most frequent during the summer months. Figure 28 shows the seasonal distribution of voltage disturbances [17].

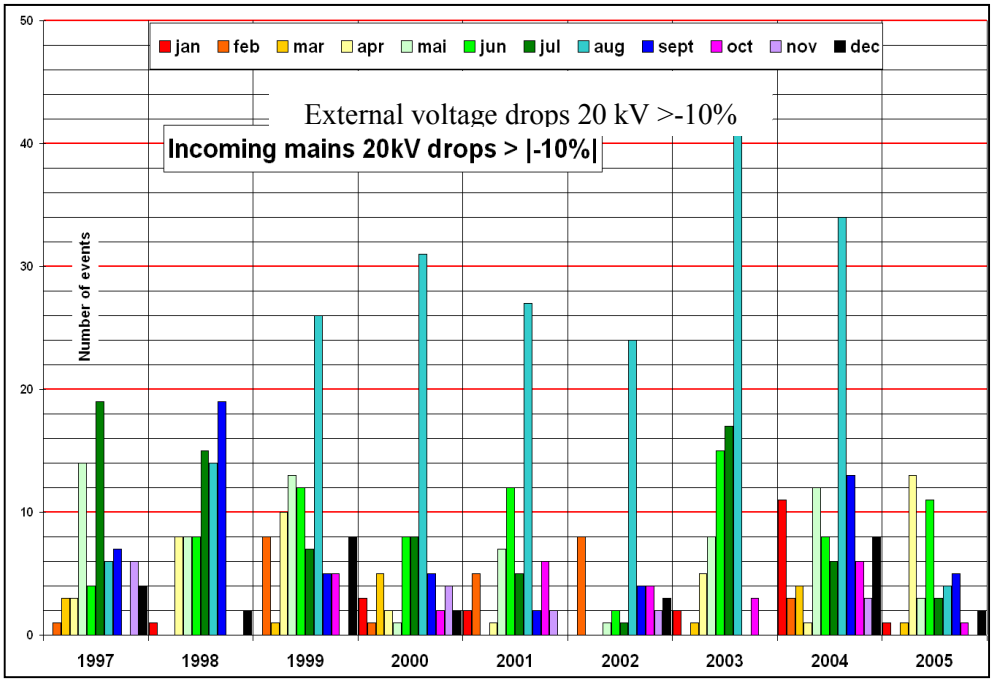

Fig. 28: Recorded frequency of voltage disturbances

In order to increase the mean time between failure (MTBF), ESRF decoupled the 20 kV accelerator network from the external supply by installing several sets of rotating machines, each consisting of an alternator and rotating mass (accumulator).

For smaller voltage disturbances (conditioning zone), the rotating machines just provide the difference to re-establish a fully balanced system with 100% of the voltage amplitude. In the event of disturbances with a larger amplitude or longer duration (disconnection area), the accelerator network is automatically disconnected from the mains and fully supplied by the rotating machines. The total stored kinetic energy of all machines is 100 MJ, and the system can compensate for 100% of missing power for 12 s. Figure 29 shows the limits of the conditioning and disconnection areas [17].

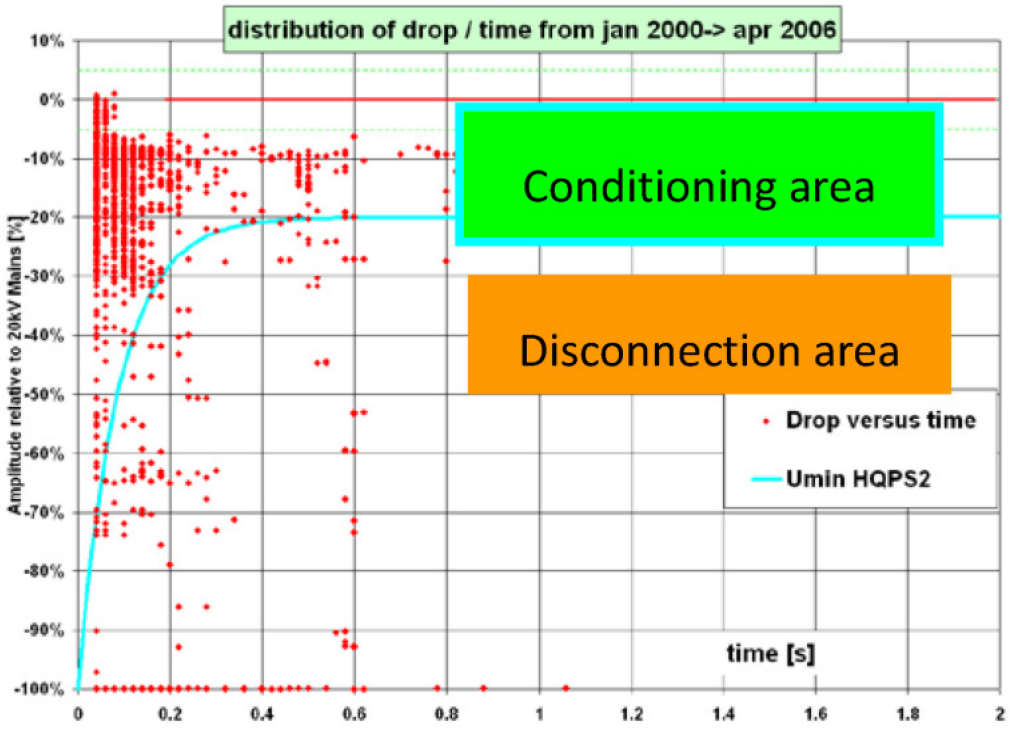

Fig. 29: Conditioning and disconnection area

Due to the combination of several machines, the system has a built-in redundancy and will also continue to operate in the event of the unavailability of one or two units. Figure 30 shows a general diagram of the system [17].

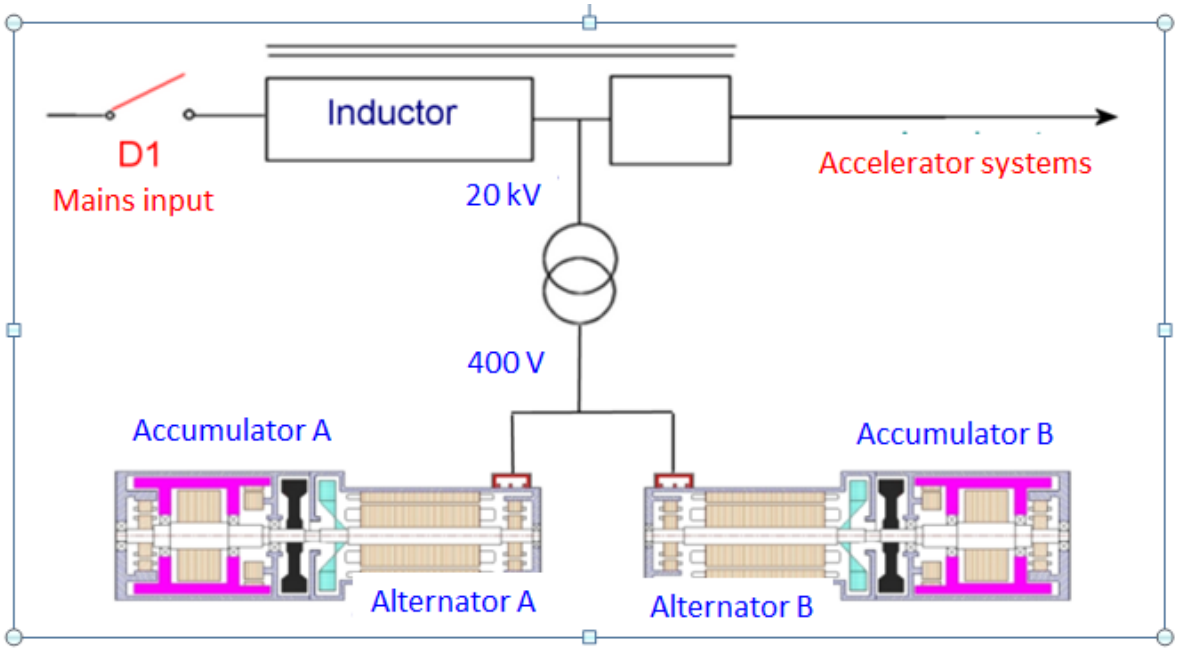

Fig. 30: Electric diagram of the network conditioning system

Fig. 31: Two twin rotablocs (four accumulators and four alternators in one cell)

6.2.4 Static synchronous compensator with energy storage

The STATCOM controls a variable output of active and reactive power, and hence completely decouples the cycling load from the electrical network. The energy could be stored in HV DC capacitors or in a superconducting magnet coil (SMES). The STATCOM technology is particularly suitable for connecting large cycling power converter loads to relatively weak electrical networks. A STATCOM could potentially also be used to compensate for transient voltage disturbances in an accelerator network.

This technology has not yet been applied for a particle accelerator network, however technical studies have commenced to evaluate the potential for this technology at CERN [18, 19].

7 Summary and recommendations

Particle accelerators require the control of the magnet current with the highest precision, sometimes to a few parts per million. To make excellent physics, excellent power quality is required! The most important aspects and recommendation of this document are summarized below.

- Voltage disturbances are part of the normal operation of electrical networks. They are frequent, and equipment must possess a certain immunity to correctly function in this environment.
- International standards such as IEC 61000 define major aspects of electromagnetic compatibility and power quality. However, in some cases they do not sufficiently cover the specific needs of your physics laboratory. In those cases *you* need to define the principal immunity levels for your electrical equipment!
- Identify the type and frequency of network disturbances that cause most of your accelerator stops, and establish detailed statistics to better understand them.
- All groups installing and operating electrical equipment need to be involved in power quality considerations, right from the beginning of a project.
- Strictly separate (cycling) power converter loads from general services loads; supply these networks from separate power transformers.
- Minimize network impedances (inductances!) to reduce voltage variations and harmonic distortion in your networks.
- When choosing a power converter topology, aim to minimize the amplitude of *cycling* reactive and active power to minimize the generation of flicker.

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Electromagnetic Compatibility of Power Converters

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Abstract
This paper describes the main challenges related to power converters in a scientific environment. It proposes some methods of EMC analysis, design, measurement, and EMC troubleshooting.

Keywords
Power converters; electromagnetic compatibility; EMC design; EMC troleshooting.

1 Introduction

This report details and completes the Baden presentation on May 9, 2014.

Electromagnetic compatibility (EMC) is, broadly speaking, nothing but a control of electrical signals. Power converters, including uninterruptible power supplies (UPS), are particularly concerned with EMC.

Converters generate high-level conducted disturbances, mainly by large converters. A converter may be upset by its own disturbances (self-immunity) or disturb its environment (scientific equipment for instance), usually due to common-mode (CM) currents.

Converters (even low-power ones) may also radiate high-frequency electromagnetic energy that can upset nearby equipment (near-field coupling) or radio receivers (far-field coupling).

1.1 Beware of unreasonable EMC standards

A scientific environment looks like an industrial one, so the relevant standards use industrial EMC limits. The conducted emission limits of many EMC standards for large equipment (UPS, inverters, speed drives, arc welders, lifts…) are objectively too high, especially for equipment with rated current over 100 A.

Mains terminal disturbance voltage limits for class A equipment measured on a test site

Frequency band	Class A equipment limits dB(μV)					
	Group 1		Group 2		Group 2 [a]	
MHz	Quasi-peak	Average	Quasi-peak	Average	Quasi-peak	Average
0,15 – 0,50	79	66	100	90	130	120
0,50 – 5	73	60	86	76	125	115
5 – 30	73	60	90 Decreasing linearly with logarithm of frequency to 70	80 Decreasing linearly with logarithm of frequency to 60	115	105

a Mains supply currents in excess of 100 A per phase when using the CISPR voltage probe or a suitable V-network (LISN or AMN).

Fig. 1: Example of a defective standard (here EN 62040-2 for UPS)

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As can be seen in Fig. 1, the allowed relaxation in quasi-peak detection for a UPS over 100 A per phase is more than 50 dB higher (i.e., more than 350 times in amplitude) than for a UPS with a rated current up to 16 A. Moreover, the level of CM conducted emission up to 30 MHz corresponds to a value over 60 dB (1000 times) above the limit of radiated level over 30 MHz!

1.2 Conducted emission levels are frequently too high

A reasonable conducted emission limit for an industrial environment is CISPR class A. This limit is rather easy to meet up to 100 A per phase. For equipment with currents larger than 100 A per phase, class A + 10 dB is a reasonable objective (both in quasi-peak and average detection).

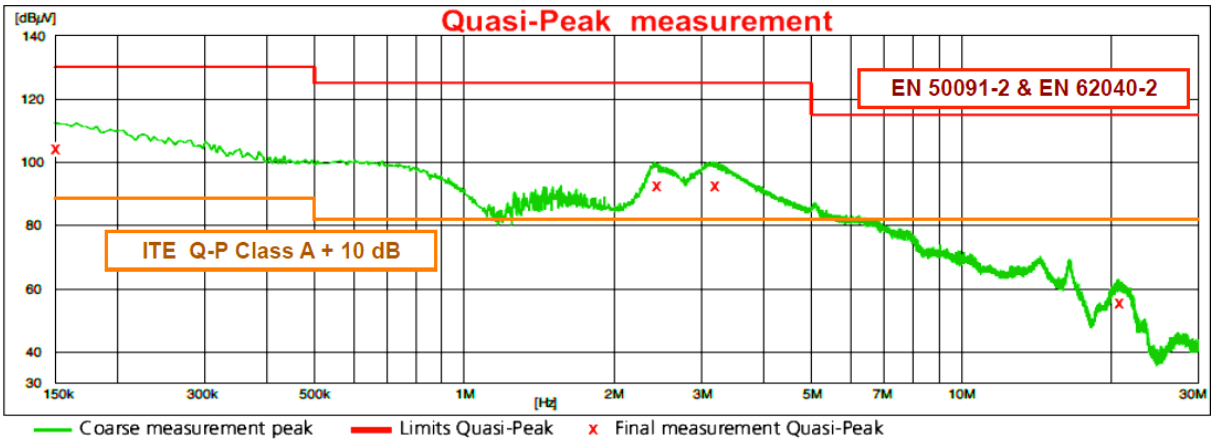

Fig. 2: Example of excessive conducted emission (80 kVA UPS, quasi-peak detection)

1.3 Beware of low-frequency band (from 2 kHz to 150 kHz)

Up to 2 kHz, the harmonic standard limits the emission levels to very low levels: no trouble.

Over 150 kHz, to meet a reasonable standard avoids most troubles.

But from 2 kHz to 150 kHz, there is still no limit for civilian standards. This band is jokingly called 'the Wild West'! Most of the troubles we meet on site appear at the switching frequency, between 4 kHz and 20 kHz. A CISPR draft is under consideration to complete the conducted voltage limit from 50 Hz to 150 kHz.

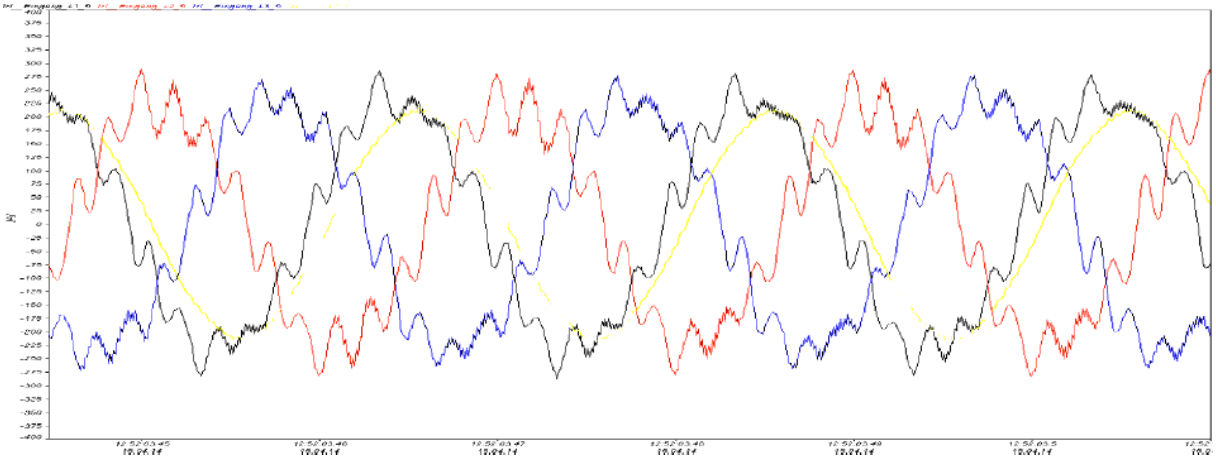

Fig. 3: Example of generated current (here the switching frequency is 5 kHz)

Pending normalized emission level, the ITER Organization at Cadarache specified a conducted emission limit based on a military standard (MIL-STD 461) for any cable (including signal cables).

This test, which uses a current probe, is easy to implement on site. The level fits CISPR limit current per phase over 150 kHz.

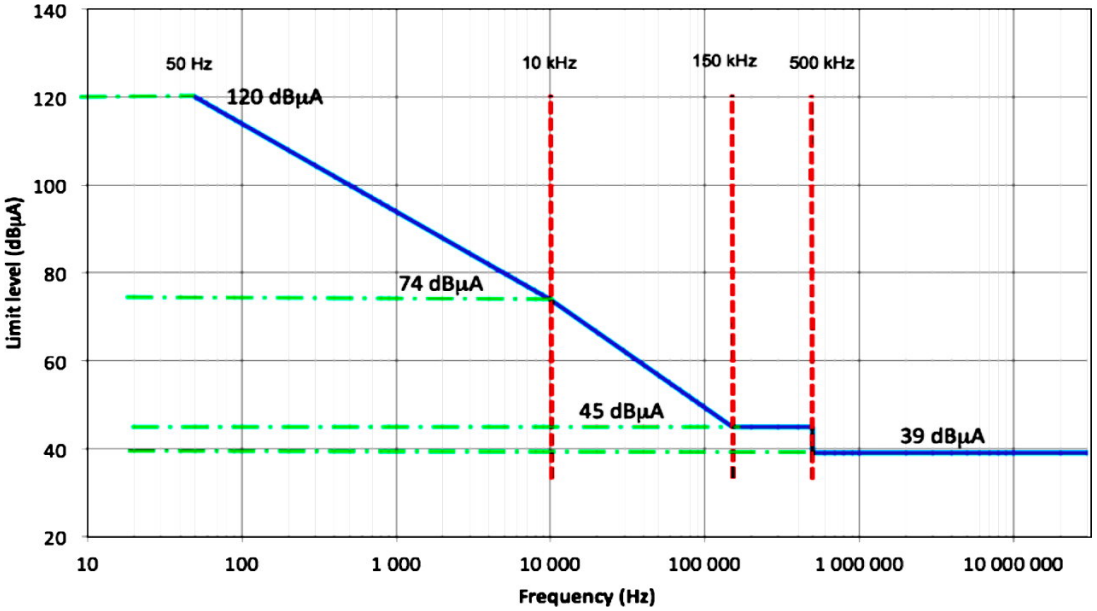

Fig. 4: Conducted emission limit for ITER Facility (here below a rated current of 1 A)

1.4 A missing immunity test

The generic immunity standard for an industrial environment, EN IEC 61000-6-2, specifies many (too many perhaps) immunity tests: electrostatic discharge, electromagnetic field immunity over 80 MHz, electrical fast transient in burst (an excellent revealing test), surges, CM immunity from 150 kHz to 80 MHz, voltage drops, and voltage fluctuations. But no immunity test is required in the frequency band from d.c. to 150 kHz. An abnormal vulnerability in this band may be ignored.

Yet a standard exists: IEC 61000-4-16. Cenelec plans to add this test for industrial environments.

2 EMC concerns of power converters

2.1 The negative impedance behaviour

Most d.c./d.c. converters have a high-voltage input dynamic range, frequently larger than a factor of 3. This means that an input-voltage reduction creates an input-current increase. This is called a ‘negative impedance’ phenomenon; it should not be confused with a possible transient output overvoltage.

The consequences of this—now well-known—behaviour, when the power supply distribution is not very low, can be varied:

- no start,
- start, but oscillates with the wrong output voltage (usually too low),
- output voltage seems correct, but the maximum output current is reduced,
- switching frequency instability, which can lead to destruction of the converter.

Fixes may be simple:

- add a larger input capacitor;

- reduce the power distribution impedance (using several pairs in parallel, for instance);
- reduce the converter regulation bandwidth.

2.2 Immunity of an optocoupler

Optocouplers and opto-isolators are components commonly used in power converters. Incredible as it may seem for electrical isolation components, the immunity of analogue optocouplers to CM disturbances is never specified (but in d.c.). Most digital optocouplers are specified for maximum dV/dt. Let us read the data sheet and comply with the limits, especially the maximum absolute ratings.

Many MOSFETs or IGBTs have a switching slope from 20 kV/μs to 50 kV/s, while most isolators are only specified up to a voltage rate immunity of 10–15 kV/μs. This doesn't lead to a destruction, but creates high-frequency oscillations that increase switching loss and radiated emissions, and may compromise reliability (due to IGBT second breakdown voltage, for instance).

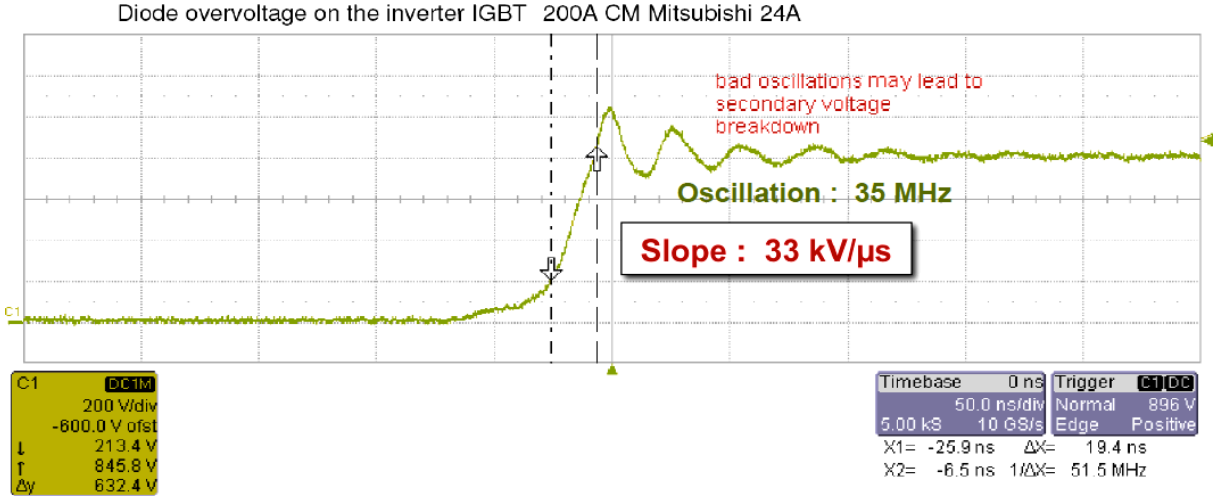

Fig. 5: Oscillation due to a voltage slope higher than opto-driver immunity (typically 15 kV/m)

2.3 Immunity and on-site fixes

The immunity of a power converter is usually correct. Nevertheless, some concern may occur regarding:

- cross-conduction of both transistors of the same arm of the H-bridge,
- instabilities or regulation faults (usually due to CM current on internal cables),
- transmission failure (usually due to CM current on transmission cable).

Fortunately, effective fixes—without drawback risks—can be applied on site:

- adding bonds between chassis or cabinet ground,
- using a shielded cable with its braid grounded at both ends,
- connecting the unused wires of a cable to chassis ground at both ends,
- adding a ferrite toroid (of a few turns) over a sensitive cable (or flat ribbon cable).

It is easy and revealing to measure the CM current on cables. For large converters, the usual useful bandwidth of the current clamp is 5–30 MHz. The maximum peak-to-peak current is typically 2 A, but—for a pretty good margin—we recommend limiting this value at 400 mA.

2.4 Input-to-output common-mode current for an isolated power supply

Most d.c./d.c. converters are isolated, using an insulating transformer. Despite this galvanic insulation, some common-mode current can flow through the stray capacitance of the transformer.

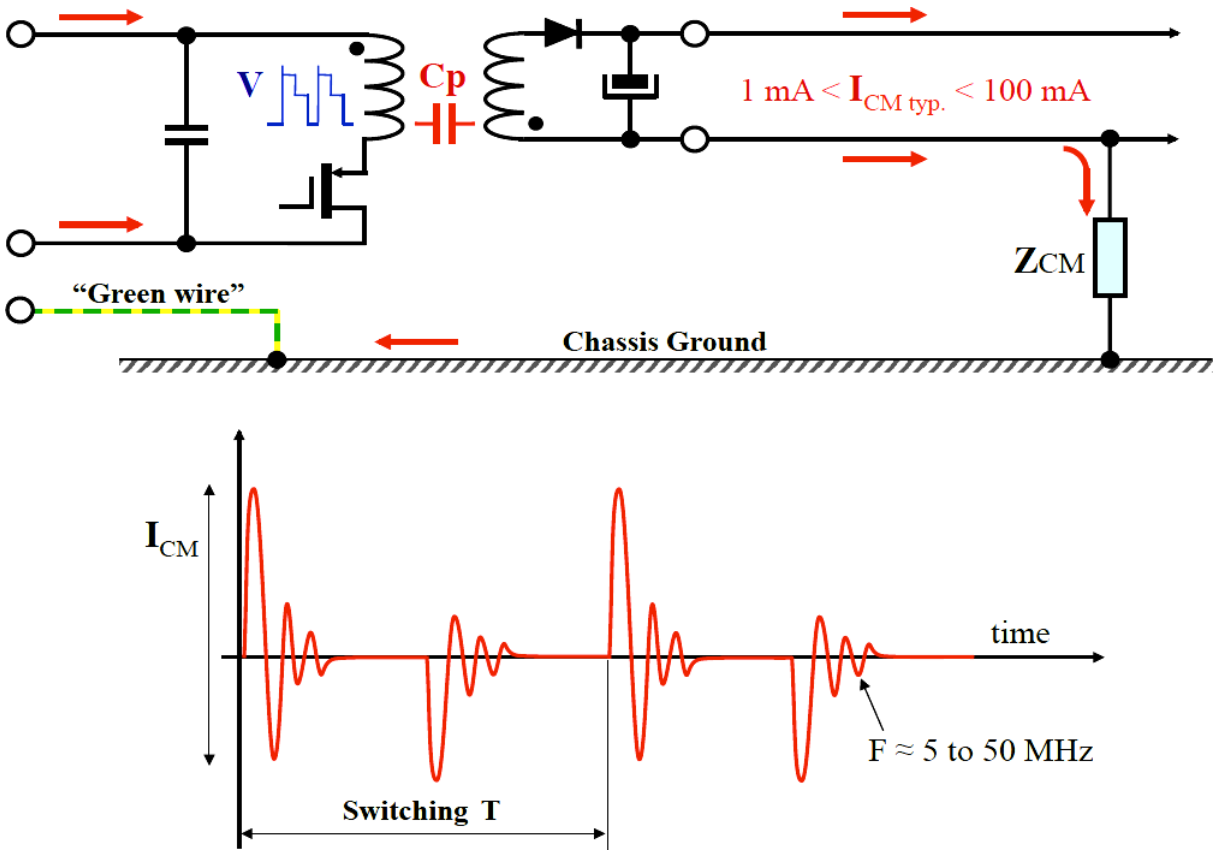

Fig. 6: Principle of primary-to-secondary CM current (typical waveform)

The amplitude of the CM current generated by an isolated d.c./d.c. converter may be as low as 1 mA (for a properly filtered power supply), or as large as 100 mA (for a poorly filtered d.c./d.c. converter). The waveform is a damped sine wave with a pseudo-frequency of 5–10 MHz for a large Switched Mode Power Supply (SMPS), reaching 25–50 MHz for a small SMPS. The repetition frequency is twice the fundamental frequency of the SMPS.

This CM current may disturb any sensitive equipment in the vicinity, starting with the supplied circuit itself. A simple solution to reduce this current is to add a CM choke or, if possible, to add capacitors from the output to the chassis ground. The total length of this connection—including the length of the metal column—must remain as short as practicable (less than 2 cm if possible).

2.5 Input-to-output CM current of an H-bridge

A single or three-phase H-bridge create large amount of common noise voltage. The CM impedance of an H-bridge is very low, so the external ground loop impedance limits the CM current.

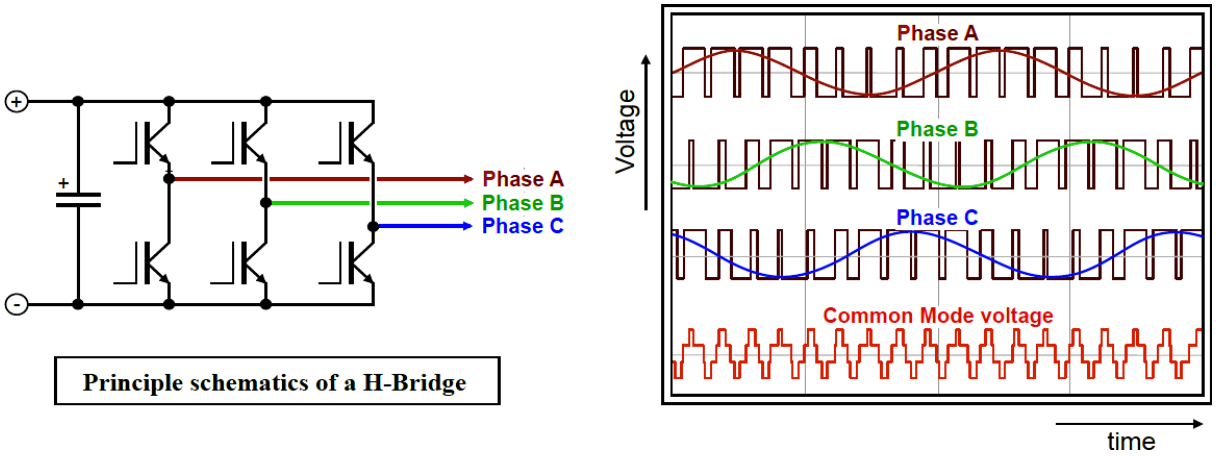

Fig. 7: Principle of a CM voltage generated by an H-bridge (here a three-phase H-bridge)

The amplitude of the CM current generated by the H-bridge may be as low as few milliamps (for a properly shielded output cable), or as large as 10 A (for a high-power motor drive). The waveform is a damped sine wave with a pseudo-frequency of 2–5 MHz for a large H-bridge, reaching 10–25 MHz for a small one.

The two common solutions to limit CM current are:

- to shield the output cable (connected to the chassis ground at both ends),
- to filter the output (but then a large filter is needed).

2.6 Common-mode disturbances depending on the topology

Common-mode disturbances emitted by a power converter depend greatly on its topology. Three main architectures can be analysed.

2.6.1 Case 1: The output of the converter is grounded

If the output of the power converter (usually a SMPS) is connected to the chassis ground, no CM current flows out of the cabinet. Also, no CM currents should flow through the internal circuits. The electromagnetic interference (EMI) mains filter is easy to optimize because the high-frequency (HF) resonances are reproducible. The CM paths are mainly primary to chassis ground (through the heat sink stray capacitance) and primary to secondary (through the transformer stray capacitance).

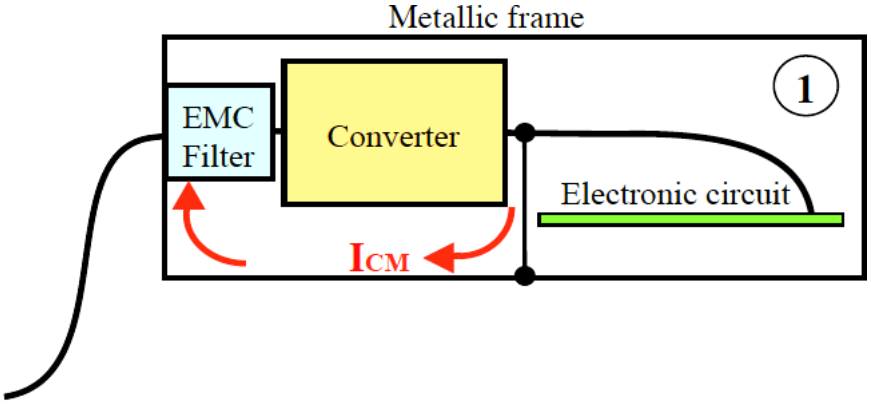

Fig. 8: Case 1: Best case—the converter output is grounded

2.6.2 Case 2: The converter output is floating, but no other cable goes out

If the output of the converter is floating, no CM current flows out of the cabinet. Nevertheless, some current may flow through the internal circuits and generate some noise. The EMI mains filter is harder to optimize because HF resonances depend on the equipment cabling (so are difficult to control, due to input-to-output variable HF impedance).

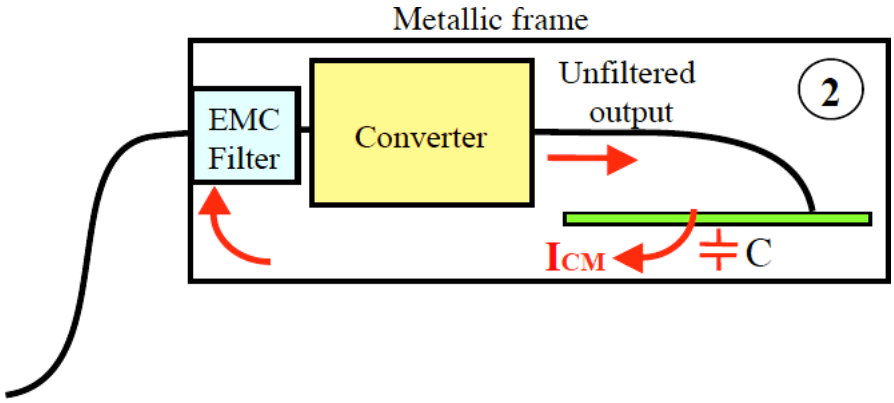

Fig. 9: Case 2: The converter output is floating but no other cable is routed out of the cabinet

2.6.3 Case 3: A noisy cable goes out of the cabinet

If a 'dirty' cable goes out of the cabinet (for instance, the cable from a variable frequency drive to its motor or to the battery of an inverter), then concerns may be severe.

First of all, the radiation of the equipment may be large and may upset other apparatus in the vicinity. Furthermore, the EMI filter is impossible to optimize because the CM currents return by any cable, even a perfectly filtered one.

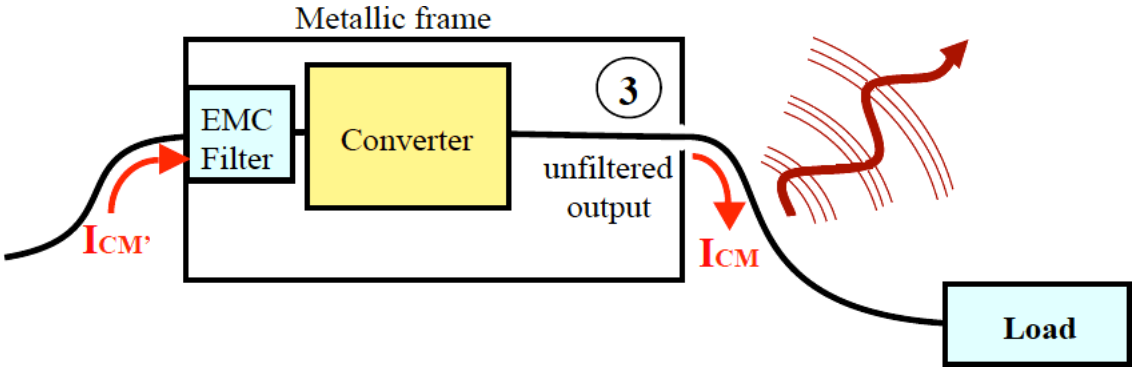

Fig. 10: Case 3: Worst case—a noisy cable is routed out of the cabinet

The usual solutions are:

- shield the noisy cable (with the braid connected to chassis ground at both ends),
- filter the cable (if possible, because such a filter may be a huge one).

3 EMC precautions in the design stage

Most of EMC concerns are easy to avoid during design. Let us consider the three most usual precautions.

3.1 Converter topology analysis

The easiest way to understand this is to take the example of a UPS schematic diagram.

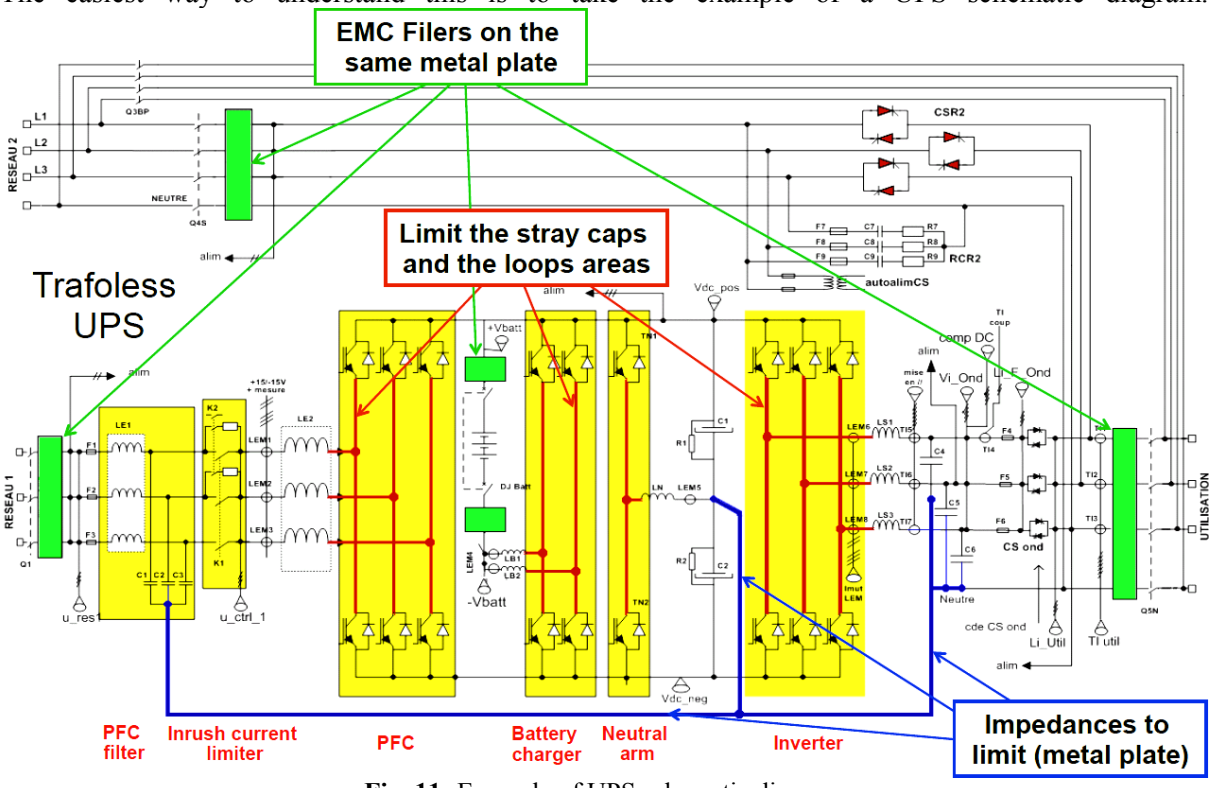

Fig. 11: Example of UPS schematic diagram

Figure 11 shows the schematic of a classical 'trafoless' (without an internal transformer) three-phase UPS. Three points need to be seriously controlled.

3.1.1 The 'hot' conductors

A 'hot' conductor is a piece of circuit submitted to high dV/dt, to high dI/dt, or both. First, we need to identify all of them (essentially the H-bridges in the upper part of Fig. 11).

The stray capacitance between high dV/dt and chassis ground must be reduced to reduce CM current generation by:

- suppressing any localized capacitor,
- floating 'hot' heat sinks,
- increasing the distance to chassis ground,
- adding 'electrostatic' shields connected to the d.c. bus (not to ground).

The loop area of high dI/dt must be reduced to limit H-field radiation by:

- using bus bars,
- using sandwich structures,
- reducing the size of the loops.

3.1.2 The 'equipotential' conductors

An 'equipotential' conductor is a conductor that must create a very low voltage drop despite a significant current in it. We must identify all of them. An example in Fig. 11 is the neutral conductor.

An equipotential conductor must be:

- wide (avoid wires, straps are preferred),
- short (place the connected components close to each other),
- of sufficient thickness—the best is a metal plate, but a short copper bar may be used.

3.1.3 The external cables

Any external cable must be identified and properly installed during EMC testing. Correct filtering effectiveness needs at least:

- an EMI mode filter on any external unshielded cable,
- a filter with the correct structure (for instance, without saturated chokes),
- all the filters should connect directly to the same chassis ground metal plate (to limit CM emission),
- to control the crosstalk between the 'dirty' and 'clean' sides of all those filters.

3.2 Cabling control

In HF, the geometry of the cabling greatly affects EMI emission. One major trap is crosstalk between the upstream and downstream of an EMI filter. It is possible to improve the effectiveness of a filter by adding capacitors, but if a star-grounding scheme is used the crosstalk between the branches of the star makes the situation worse than without added capacitors.

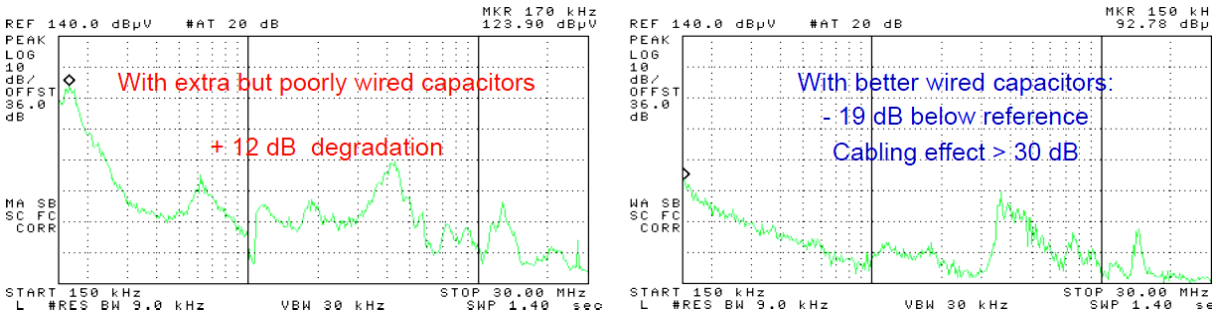

Fig. 12: Example of conducted EMI with poor (left) and better cabling geometry (right)

3.3 Risk of oscillations

Any H-bridge may oscillate if it is poorly wired or poorly controlled. Such an oscillation typically appears between 30 and 300 MHz. The effects are a loss and radiated emission increase. The risks of oscillations increase with:

- the gate trace (or cabling) length,
- the d.c. bus voltage (typically over 100 V),
- a fast dV/dt or dI/dt switching rate (due to a high control current),
- a fast transistor (with low parasitic capacitors),
- a low (or no) reverse blocking voltage.

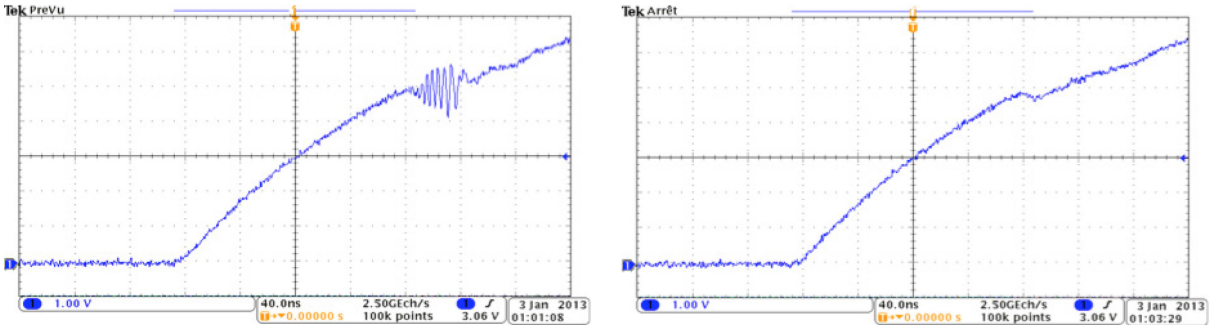

Fig. 13: Example of oscillation at 200 MHz (left) stopped with a ferrite bead in series with gate (right)

Solutions to an oscillation concern may be rather simple:

- the addition of a small resistor or a ferrite bead in series with the gate,
- the addition of a push–pull stage close to the gate,
- the use of a negative voltage block.

3.4 Immunity testing

The design of a power converter needs to control the thermal behaviour, the dynamic margins, the transient stability, and EMI emission. Those checks are usually done well. But at least two immunity tests should be done:

- a surge immunity test according to IEC 61000-4-5 standard (lightning immunity),
- an electrical fast transient in burst (EFT/B) test according to 61000-4-4 standard.

The low-frequency surge immunity may be simulated if we pay attention to non-linear effects (at least saturation of inductances and voltage clamping by MOV or Transzorb).

The HF EFT/B test cannot be correctly simulated, so a test is needed. This CM test, over each external cable, is simple, reproducible, and revealing.

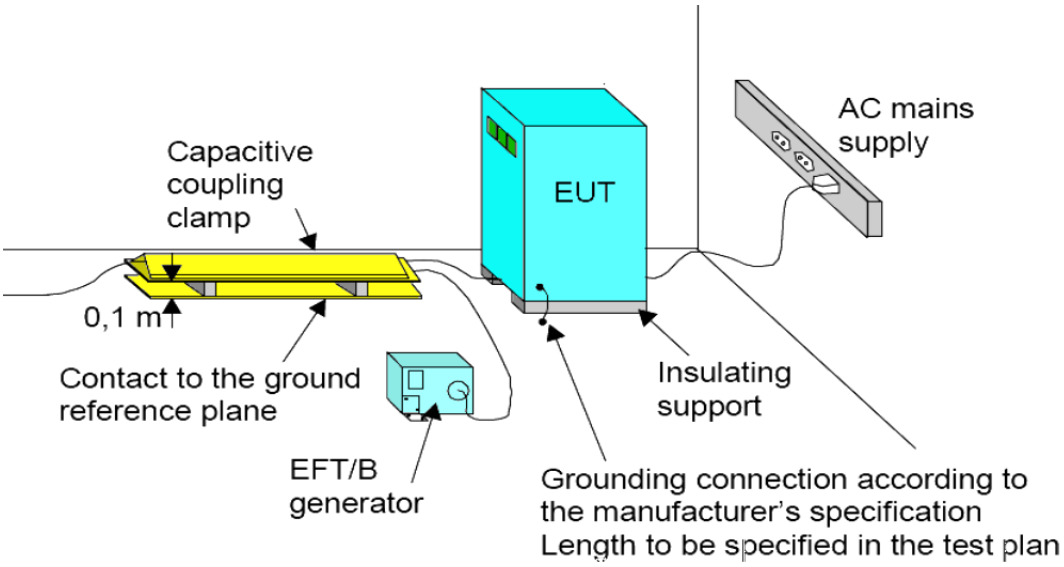

Fig. 14: Typical EFT/B test setup

4 Measuring equipment

4.1 Measuring equipment for development

Power converter development essentially uses time-domain measurement apparatus (data channel).

4.1.1 Digital oscilloscope

A digital oscilloscope is needed with, at least, the following features:

- bandwidth ≥ 300 MHz,
- single shot sampling frequency ≥ 1 Gs/s,
- fine and precise triggering threshold,
- with the possibility of screenshot.

4.1.2 Current probes

During development, two current probes may be used:

- active d.c. (Hall effect) current probes (if possible with a bandwidth ≥ 60 MHz),
- passive HF current clamp (if possible with a bandwidth ≥ 300 MHz).

Both can be used without any particular problems; we just have to pay attention to the risk of saturation and verify that the bandwidth is sufficient.

4.1.3 Voltage probes

During development, we need an active differential probe with, at least, the following features:

- primary voltage swing ≥ 1000 V,
- bandwidth ≥ 100 MHz (so a 50 Ω output impedance is needed),
- CM rejection ratio > 50 dB at 1 MHz (≥60 dB recommended),
- division factor of 1/200 to 1/2000,
- noise as low as possible, but <1 V peak-to-peak brought to high-voltage side.

Unfortunately, most differential voltage probes do not meet all these requirements.

4.2 Measuring equipment for EMC testing

EMC testing and validation essentially uses frequency-domain data channels.

4.2.1 Spectrum analyser or measuring receiver

A spectrum analyser is a fast, easy-to-use, and reasonably low-cost piece of equipment. Unfortunately spectrum analysers may saturate easily and usually do not display log-log results (dB vs. log of frequency). With its pre-selector and numerous simultaneous detectors, an EMI receiver may be preferred. In both cases, the following features are required:

- input overvoltage protection (both are fragile),
- minimum frequency band 150 kHz to 1 GHz,
- MIL or CISPR normalized bandwidths.

4.2.2 LISN and 1500 Ω probe

Up to 16 A per phase, a Line Impedance Stabilization Network (LISN or artificial network) is required. For high currents, however, a CISPR 1500 Ω probe is required.

The implementation of a LISN requires the taking of some precautions:

- an isolation transformer to limit current leakage at 50 Hz,
- a very short ground connection to the voltage reference plate,
- voltage control of the output,
- some ventilation for high power,
- removal of the magnetic field radiated by the power converter.

A 1500 Ω voltage probe may be homemade. Its use requires the taking of some precautions:

- a short connection to chassis ground,
- the absence of interfering equipment in the environment,
- the acceptance of deviations from a measurement with an artificial network.

4.2.3 Current probe

For EMI measurements, we need at least two current clamps:

- A low-frequency clamp (say from 5 kHz to at least 30 MHz). This current probe should not saturated by a large 50 Hz component. Its transfer impedance may be derivative up to about 1 MHz.
- A high-frequency probe (say from 10 MHz to 300 MHz). This probe should have a flat transfer impedance. The recommended value is 5–10 Ω. Such a sensitive clamp may also be homemade.

4.2.4 Other near-field homemade probes

Some near-field (non-calibrated) probes are very useful for EMC analysis when developing power converters. Those E-field and H-field may be homemade. Their size will be adjusted as required.

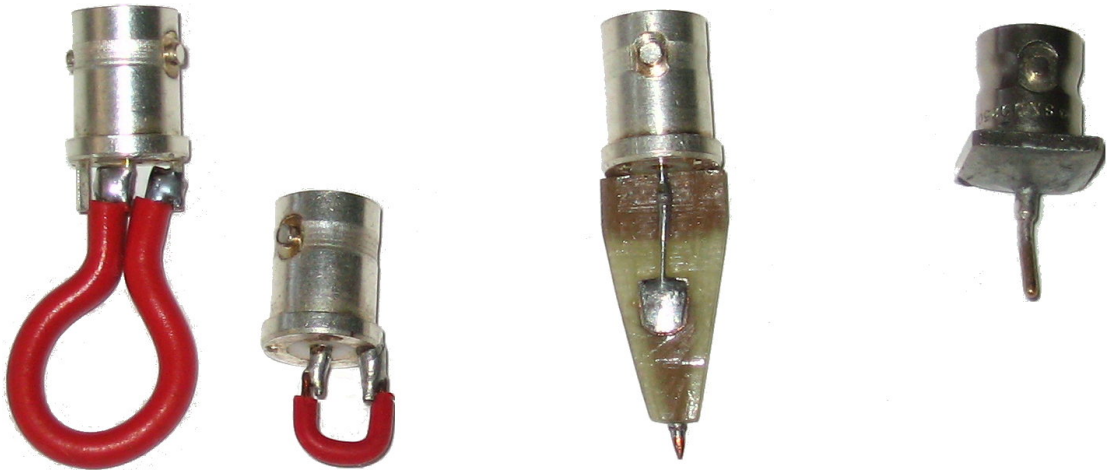

Fig. 15: Some examples of homemade $\Delta B/\Delta t$, $\Delta V/\Delta t$, and Zt measurement probes

5 Conclusions

Power converters may generate a large amount of electromagnetic noise. They must be filtered and, possibly, shielded. Some features can be correctly simulated, for instance low-frequency stability or transient behaviour. Unfortunately, some EMC features can only be measured at the end of the design. For instance, conducted or radiated behaviour over 1 MHz for a large converter (10 MHz for a small one) is quite difficult to simulate correctly.

The EMC of a power converter is quite easy to control if we correctly:

- foresee phenomena during an early part of the design stage,
- plan the time to analyse and understand the measurements after development,
- plan the time to fix the troubles and to optimize the EMC solutions (filters and shields).

Recall that most large converters (UPS or motor drives) meet European standards but not the requirements of the EMC directive. That is the reason why the CISPR standard should be reviewed:

- to suppress the 'Wild West effect' (from d.c. to 150 kHz) in both emission and immunity,
- to reduce the permitted conducted emission level for equipment over 100 A per phase.

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Double-Frame Current Control with a Multivariable PI Controller and Power Compensation for Weak Unbalanced Networks

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Abstract
The handling of weak networks with asymmetric loads and disturbances implies the accurate handling of the second-harmonic component that appears in an unbalanced network. This paper proposes a classic vector control approach using a PI-based controller with superior decoupling capabilities for operation in weak networks with unbalanced phase voltages. A synchronization method for weak unbalanced networks is detailed, with dedicated dimensioning rules. The use of a double-frame controller allows a current symmetry or controlled imbalance to be forced for compensation of power oscillations by controlling the negative current sequence. This paper also serves as a useful reminder of the proper way to cancel the inherent coupling effect due to the transformation to the synchronous rotating reference frame, and of basic considerations of the relationship between switching frequency and control bandwidth.

Keywords
Asymmetric networks; weak networks; PLL; double frame control; multivariable PI control; power theory.

1 Introduction

In the field of grid-connected power converters that interface a DC link to an AC three-phase network, the control of the current taken or injected presents challenges that are not taken into account when infinite networks are considered. In fact, networks are becoming weaker and weaker owing to the multiplication of decentralized power sources and islanded systems. As a consequence, there is a strong need for a synchronization system that can handle the disturbances inherent in weak networks, and the harmonics produced in the controlled power converter itself.

Moreover, the need for operation in an unbalanced network implies a need to control the second-harmonic component that appears more generally when an asynchronous network is operated in a synchronous reference frame. Also, being generally limited in bandwidth because of the very low switching frequencies used on the network side, the current controller is unable by itself to compensate for second-harmonic perturbation.

A common solution, not focused on any particular application, must be found for any grid converter connected to a weak network [1]. This paper offers a simple method that is applicable over a wide range of fields, including industrial drives, wind generators, ship applications such as hybrid propulsion and onboard network supplies, electric vehicles (with support for smart grids), aircraft AC and DC onboard networks, and any islanded system, moving or not.

2 Converter and grid considerations

The typical voltage source inverter connects a DC link to the grid through a transformer with a filter on its secondary side. As illustrated in Fig. 1, the grid transformer may be modelled by its leakage impedance added to the filter inductance. The main purpose of the converter is to control the current, either to maintain the DC link voltage V_{DC} or to maintain the voltage on the network side. The interfaced

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signals and system parameters are described in Table 1. The network as seen from the power converter side may be modelled as a voltage source V_{NET} and its grid impedance Z_{NET} as seen from the converter side, reflecting its strength as in Ref. [2].

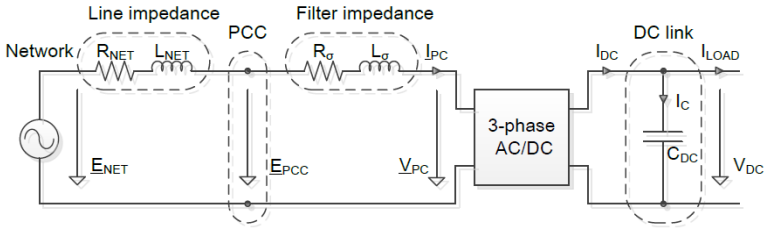


Fig. 1: Grid-connected power converter on system level

The converter is operated using a vector control strategy. The grid voltages E_{PCC} measured at the point of common coupling and the converter currents I_{PC} can be described in the synchronous reference frame computed by the well-known Park transformation; here, proper decoupling with respect to network perturbations is a key requirement for a stable controller. The synchronization with the grid, which is done with a dedicated phase-locked loop (PLL) that provides the reference for the vector controller, is detailed in the following section.

Table 1: List of signals and parameters in the system

Signal	Units	Description
$\underline{E}_{\mathrm{NET}}$	V	Three-phase network voltage
$\underline{E}_{\mathrm{PCC}}$	V	Three-phase voltage measured at PCC
ω_{N}	Hz	Angular frequency of the synchronous rotating frame
θ_{N}	rad	Position angle of the synchronous rotating frame
$\underline{V}_{\mathrm{PC}}$	V	Power converter voltage on grid side
$\underline{I}_{\mathrm{PC}}$	A	Power converter current on grid side
V_{DC}	V	DC link voltage
I_{DC}	A	Feeding current from grid converter
I_{C}	A	DC link capacitor current
I_{LOAD}	A	Load current
Parameter	**Units**	**Description**
C_{DC}	F	DC link capacitance
L_{σ}	H	Equivalent line inductance on the converter side
R_{σ}	Ω	Equivalent line resistance on the converter side
Z_{σ}	Ω	Equivalent total line impedance on the converter side
L_{NET}	H	Equivalent line inductance of the network
R_{NET}	Ω	Equivalent line resistance of the network
Z_{NET}	Ω	Equivalent total line impedance of the network
f_{NET}	Hz	Frequency of the network
ϕ_{NET}	rad	Angle of equivalent network impedance phasor
S_{SCC}	VA	Short-circuit power of the network

2.1 Strength of the grid

The strength of a network is defined by its short-circuit power S_{SCC} as it appears at the point of common coupling (PCC). It may also be expressed as a ratio relative to the nominal power of the grid converter.

Strong networks typically have a nominal power higher than 20 times that of the grid converter, and very weak networks, such as networks in ships and remote microgrids, have less than 8 times that of the grid converter. This value defines the influence of a power converter on a given network. In the case of a converter connected to a weak network, Z_{NET} is not negligible compared with Z_{σ}, and then the voltage E_{PCC} as measured at the point of common coupling is different from the idealized network voltage V_{NET}, as illustrated in Fig. 2. In such a case, harmonics injected by the power converter appear in the measured voltages, which significantly disturb the controller as illustrated in Fig. 3(b). Under conditions of phase voltage imbalance, the approximate circle in the Cartesian plane becomes an ellipse as in Fig. 3(c), in which case filtering as in Fig. 3(d) can only be performed by applying the decoupling principles described in the following section. To assess the equivalent impedance of the network as seen from the PCC, one can use the relations given in Eq. (1):

$$\begin{cases} Z_{\mathrm{NET}} = \dfrac{E_{\mathrm{NET}}^2}{S_{\mathrm{SCC}}}, \\ R_{\mathrm{NET}} = Z_{\mathrm{NET}} \cos \phi_{\mathrm{NET}}, \\ L_{\mathrm{NET}} = \dfrac{Z_{\mathrm{NET}} \sin \phi_{\mathrm{NET}}}{2\pi f_{\mathrm{NET}}}. \end{cases} \tag{1}$$

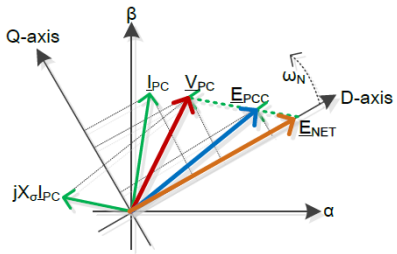
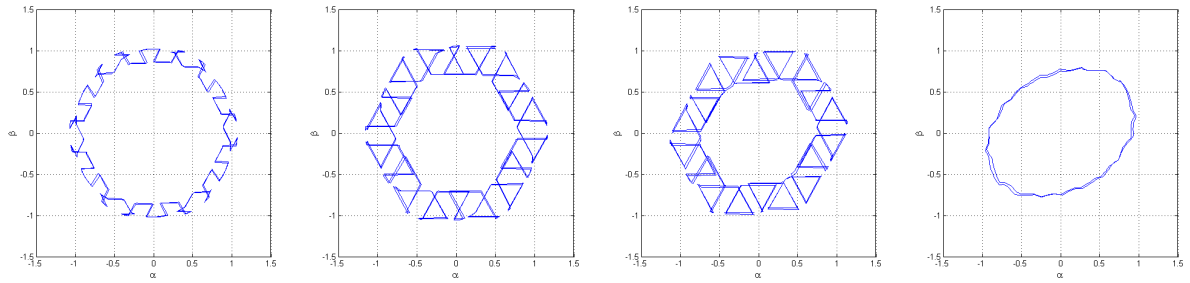


Fig. 2: Principle of network synchronization and vector control



(a) (b) (c) (d)

Fig. 3: $\alpha\beta$ representation of voltages at PCC (a) for a strong network (20×) under balanced conditions, and for a weak network (5×) under (b) balanced and (c) unbalanced conditions; (d) its recomposition from decoupled filtered values.

3 Grid synchronization

The most common way of synchronizing a controller with an alternating signal is to use a PLL. The quadrature part of the network voltage, transformed into the synchronous reference frame, is used as the rotating-frame phase error input to a PI controller. However, the use of simple filters is not adequate for synchronization with weak networks with harmonics and asymmetric disturbances. Several methods

for improving the robustness of the synchronization of the system with the network have been presented [3–6]. In the work presented in this paper, the method implemented for decoupling the second harmonic inherent in a voltage imbalance was inspired by Ref. [7], where decoupling of the positive and negative sequences of the voltage allows all perturbations in each reference frame to be properly filtered, and then the sequences are recombined to obtain a clean representation of the network with selected harmonics.

3.1 Phase-locked loop

The control principle of the synchronous-reference-frame PLL was based on the minimization of the phase error between the rotating frame and the network, as illustrated in Fig. 4. The quadrature component of the voltage was used directly as the phase error, since one can take the sine of a small quantity as almost equal to that quantity. Using a simple PI controller, the resulting value was filtered to obtain the state variable ω_{N}, which was integrated to obtain the phase function θ_{N}.

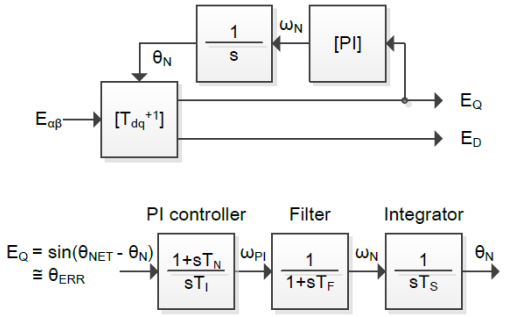


Fig. 4: Equivalent control structure of the PLL

The parameters of the PI controller were set using a magnitude optimum criterion given by the transfer functions of the filter, $G_{\mathrm{F}}(s)$ (Eq. (2)), the plant, $G_{\mathrm{S}}(s)$ (Eq. (3)) (which was actually the integrator), and the controller itself, $G_{\mathrm{R}}(s)$, as described in Eq. (4). The time constant T_{N} of the controller was set in order to compensate the dominant time constant of the system T_{S} (Eq. (5)), and the integral time constant T_{I} was set as a function of the filter time constant T_{F} (Eq. (6)):

$$G_{\mathrm{F}}(s) = \frac{1}{1+sT_{\mathrm{F}}}, \tag{2}$$

$$G_{\mathrm{S}}(s) = \frac{1}{sT_{\mathrm{S}}}, \tag{3}$$

$$G_{\mathrm{R}}(s) = \frac{1+sT_{\mathrm{N}}}{sT_{\mathrm{I}}}, \tag{4}$$

$$T_{\mathrm{N}} = T_{\mathrm{S}} = \frac{1}{\omega_{NET}}, \tag{5}$$

$$T_{\mathrm{I}} = 2K_{\mathrm{F}}K_{\mathrm{S}}T_{\mathrm{F}} = 2T_{\mathrm{F}}. \tag{6}$$

As a result, the open-loop transfer function $G_0(s) = G_{\mathrm{R}}(s)G_{\mathrm{F}}(s)G_{\mathrm{S}}(s)$ crossed the zero axis with a slope of -20 dB/dec and eliminated all higher frequencies, as illustrated in Fig. 5. By computing the optimal parameters using the magnitude optimum criterion, we obtained a phase margin of 63° that ensured stability of the system. The time constant T_{F} of the PLL filter, which defines the overall dynamics of the system, was chosen as a function of the utility grid frequency and the harmonics that we wanted to eliminate.

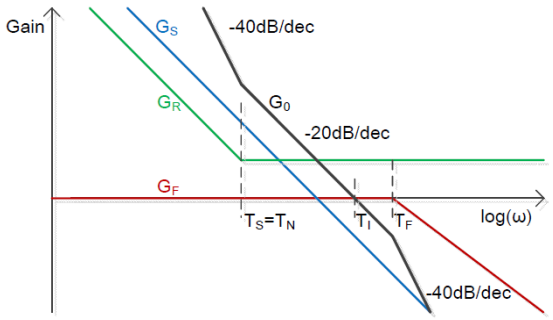


Fig. 5: Bandwidth of the control structure of the PLL

3.2 Synchronization with a weak network

The PLL described above was tested in a hardware-in-the-loop (HIL) simulation model recreating a real industrial control platform, with its own individual sampling systems connected to a model of the power components as described in Fig. 1. The PI controller was tested with a phase step in the phase voltages, which corresponds to a situation where a reactive load is connected to a network with which a converter must be synchronized. This phase step could be performed in the rotating frame itself to test a PLL in a real system.

As illustrated in Fig. 6(b), the PLL became synchronized with the network phase after one and a half periods, corresponding to the time constant of the PLL filter. The harmonics due to converter switching were entirely rejected as long as the phase voltages were balanced. When a phase voltage imbalance occurred, as in Fig. 6(c), the inherent second harmonic appeared in the angular frequency ω_N of the reference frame, and also appeared in the phase θ_N.

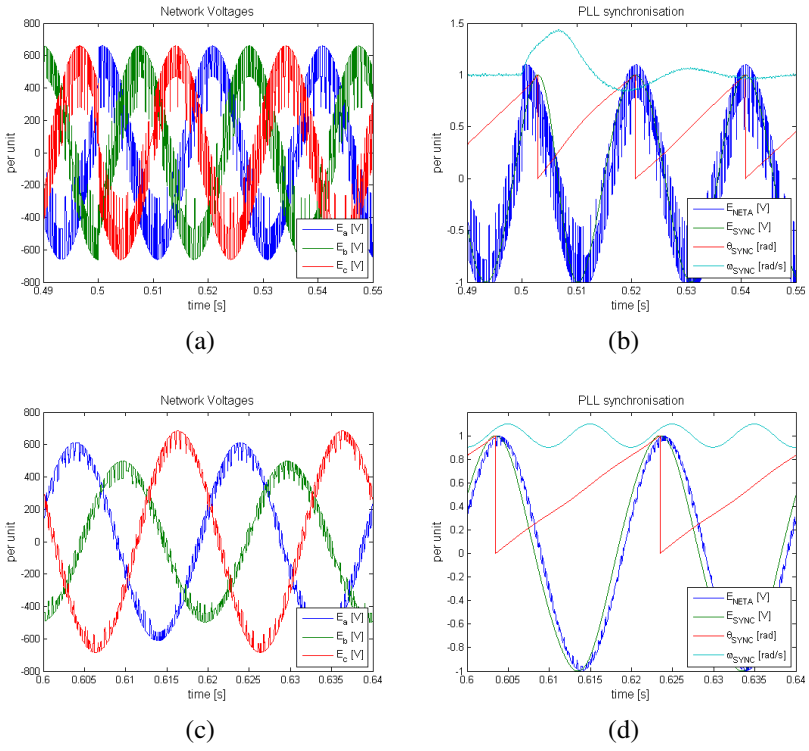


Fig. 6: (a) Phase step in the phase voltages of a weak network, (b) response of PLL to phase step, (c) asymmetric phase voltages in a strong network, and (d) effect of second harmonic in the PLL signals due to asymmetry.

3.3 Synchronization with an asymmetric network

To operate with signals containing a strong second-harmonic content, one needs to apply a decoupling strategy in two reference frames, namely the positive- and negative-sequence synchronous rotating frames. The decoupling of the two sequences, as introduced in Ref. [7], uses the core principle that the vector projection onto a reference rotating frame results in a DC component in the frequency content of a signal corresponding to that reference rotating frame. A signal containing several harmonics can be described in the Cartesian plane by the addition of several vectors of a fixed length rotating at a fixed frequency.

According to the decoupling principle illustrated in Fig. 7, one can separate the reference signal into a fundamental component and its second harmonic, described individually in two different rotating reference frames. Once the two rotating vectors have been found, one can decouple them from each other in order to consider the second-harmonic perturbation separately from the fundamental harmonic. The benefit for a PLL that is synchronized with the rotating reference frame lies in the possibility of using a reference signal from the positive sequence decoupled from the second-harmonic perturbation. Its implementation is not as difficult as is stated in Ref. [8] and does not require the use of notch filters, which are not reliable. Moreover, the function of the decoupling is not restricted to the PLL controller; it also provides four decoupled voltage components that can be used in current control as voltage feedforward signals, and can possibly be used to compute current references for the compensation of power oscillations occurring during phase voltage asymmetries.

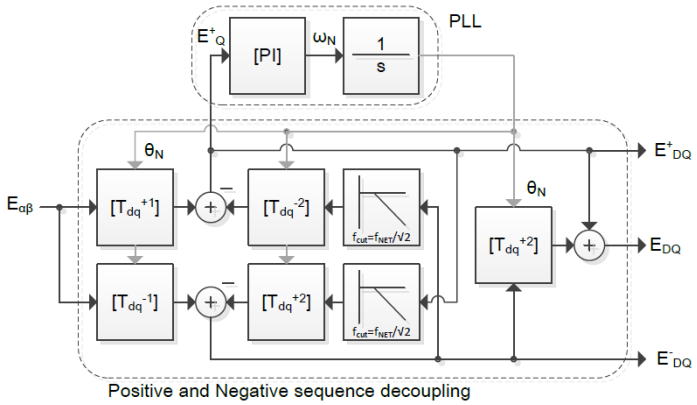


Fig. 7: Double-decoupled synchronous-reference-frame PLL

A mathematical proof supporting this decoupling scheme can be found in Ref. [7], but the overall operation principle is illustrated in Fig. 8. The phase voltages are first transformed to both positive- and negative-sequence rotating reference frames, giving the four blue curves E^{+}_{DCP}, E^{+}_{QCP}, E^{-}_{DCP}, and E^{-}_{Q}. From each of them is subtracted the projection of the decoupled value from the opposite reference frame, E^{+}_{DDECNEG}, E^{+}_{QDECNEG}, E^{-}_{DDECPOS}, and E^{-}_{QDECPOS}, respectively, shown here in red. This operation results in voltages in two reference frames decoupled from the opposite reference frame, E^{+}_{DDEC}, E^{+}_{QDEC}, E^{-}_{DDEC}, and E^{-}_{QDEC}, shown in green. These decoupled voltages are filtered to obtain the cyan curves E^{+}_{DFILT}, E^{+}_{QFILT}, E^{-}_{DFILT}, and E^{-}_{QFILT}, and transformed into the opposite rotating reference frame to produce again the red curves E^{+}_{DDECNEG}, E^{+}_{QDECNEG}, E^{-}_{DDECPOS}, and E^{-}_{QDECPOS}, which are used to subtract the coupling from the input voltages. The filter is necessary in order to avoid the infinite-gain loop inherent in the decoupling system. The implementation in a digital controller requires a buffer for feeding back the filtered decoupled values.

When an imbalance occurs, as in the DQ representation of the voltages in Fig. 9(a), the decoupling of the two opposite sequences is computed using a time transient due to the filtering of the feedback signal. The results of recombination of the two filtered and decoupled signals (Figs. 9(b) and 9(c)) contain

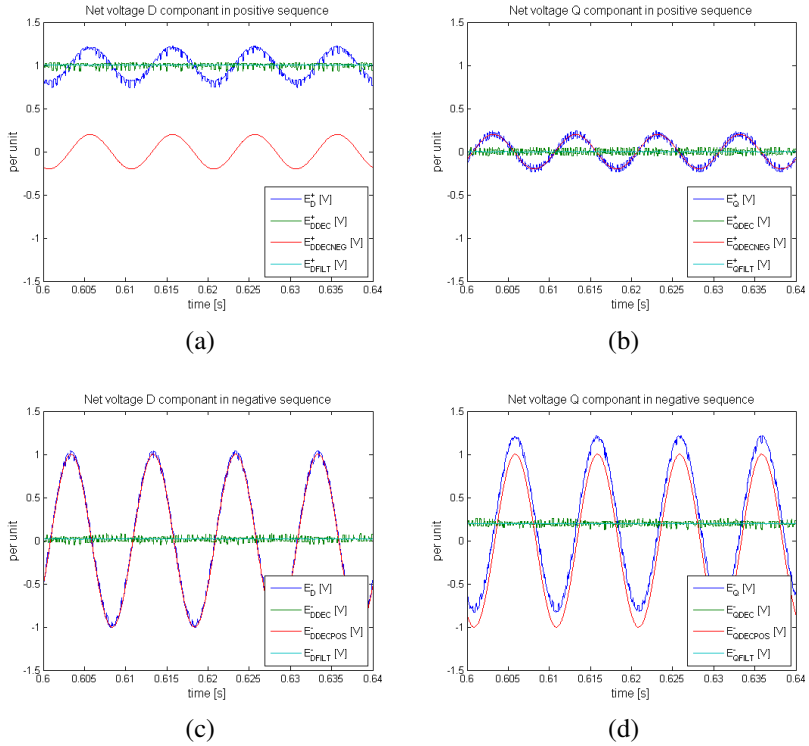


Fig. 8: Decoupling illustrated with values of (a) the positive-sequence D components, (b) positive-sequence Q components, (c) negative-sequence D components, and (d) negative-sequence Q components.

only the fundamental frequency from the positive-sequence rotating frame and the second harmonic from the negative-sequence rotating frame. As the filtered signal provides a clean description of the second harmonic with no phase errors (Fig. 9(d)), this filtered signal can be used as an accurate feedforward value at the output of the current controller.

4 Current control

The current controller for the voltage source inverters that was used in this work was similar to the classic PI controller operating in the synchronous rotating reference frame, but had superior decoupling characteristics [9, 10]. Dimensioning rules will be given for the optimal parameters as a function of the bandwidth of the whole system. For grid-connected converters operating at lower switching frequencies, the bandwidth does not allow one to compensate the second harmonic due to phase voltage imbalance. In the present work, an approach similar to that used for the decoupling of the second-harmonic component of the network voltages was adopted for the measured phase currents. In the positive sequence, the current vector is given by I_{D}^{+} and I_{Q}^{+}, and the current vector in the negative sequence is given by I_{D}^{-} and I_{Q}^{-}. If the currents are well balanced, the negative components I_{D}^{-} and I_{Q}^{-} are zero; if the currents are in phase with the voltages, the positive component I_{Q}^{+} is zero. Feeding the decoupled voltages in the positive and negative sequences forward helps the controller to compensate the current imbalance [11]. However, for full control of the current (im)balance, we suggest a double-frame control approach, with one frame controller for each of the two sequences. This method is well known in the literature [12–16]; however, the proper decoupling of the sequences in the two rotating frames was introduced only in Ref. [17], and details were given in Ref. [18]. Other control methods exist in the stationary reference frame [19], but will not be considered here.

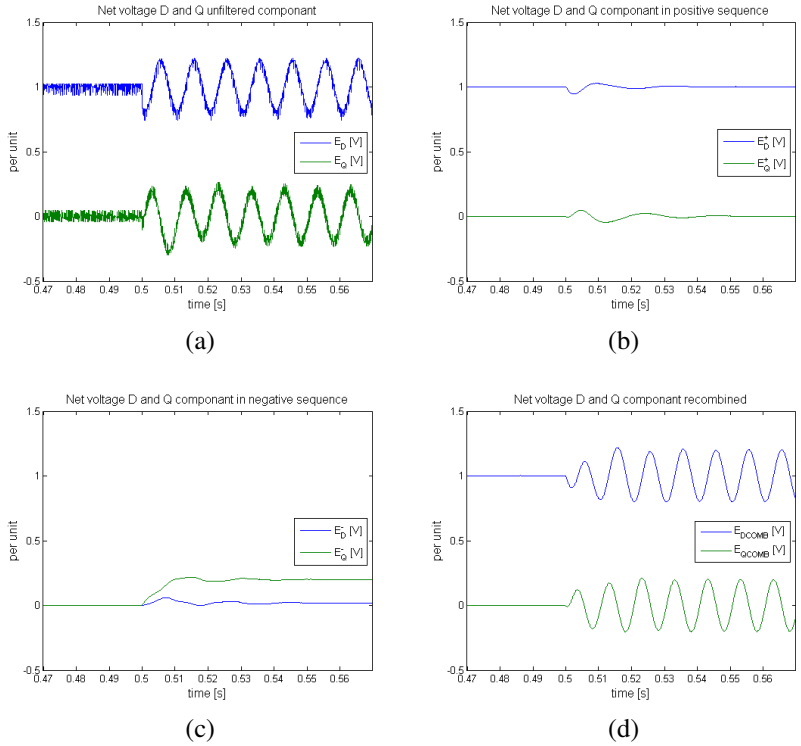


Fig. 9: (a) Decoupling of the second-harmonic component in positive-sequence reference frame, (b) decoupled positive sequence, (c) decoupled negative sequence, and (d) recombination of decoupled sequences.

4.1 Multivariable current controller for voltage source inverters

The plant is described in the stationary reference frame as a function of the voltage phasor $\underline{U}$, the current phasor $\underline{I}$, and the passive elements R_σ and L_σ as in Eq. (7). The transformation to the rotating reference frame causes the voltage $\underline{U}_\mathrm{S}$ to appear as a component $j\omega L_\sigma \underline{I}_\mathrm{S}$ as in Eq. (8), which is the inherent coupling between the direct and quadrature components. In the classic PI controller, this component is compensated by a proportional term ωL_σ, but mathematical analysis shows that the full compensation contains a cross-coupling with integrators, as demonstrated in Refs. [9, 10], when the principle of the multivariable PI controller is applied:

$$\underline{U} = R_\sigma \underline{I} + L_\sigma \frac{\mathrm{d}(\underline{I})}{\mathrm{d}t}, \tag{7}$$

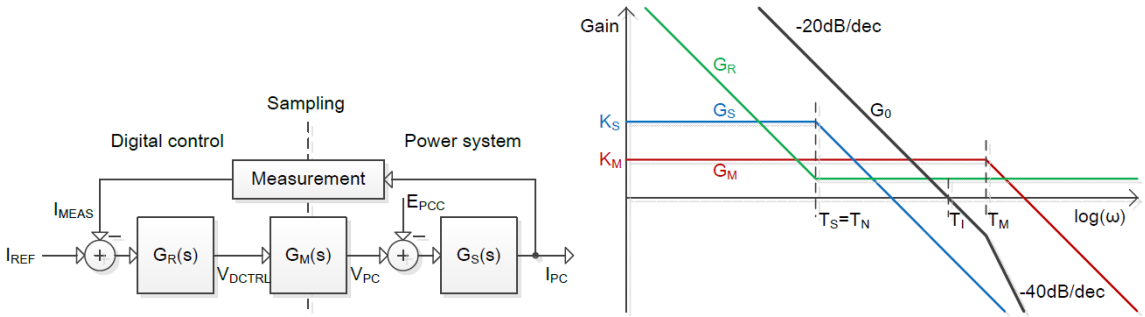
$$\underline{U}_\mathrm{S} = R_\sigma \underline{I} e^{j\omega t} + L_\sigma \frac{\mathrm{d}(\underline{I} e^{j\omega t})}{\mathrm{d}t} = R_\sigma \underline{I}_\mathrm{S} + L_\sigma \frac{\mathrm{d}\underline{I}_\mathrm{S}}{\mathrm{d}t} + j\omega L_\sigma \underline{I}_\mathrm{S} = [R_\sigma + (s + j\omega)L_\sigma]\underline{I}_\mathrm{S}. \tag{8}$$

The feedback control principle is illustrated in Fig. 10(a). The block elements of the system, considered in the Laplace domain, describe the plant $G_\mathrm{S}(s)$, the modulator $G_\mathrm{M}(s)$, and the measurement of the current. The controller $G_\mathrm{R}(s)$ was defined in order to compensate the plant time constant T_N. The integral time constant T_I was defined using the magnitude optimum criterion as given by Eq. (9):

$$\begin{cases} G_\mathrm{S}(s) = \dfrac{K_S}{1 + (s + j\omega)T_\mathrm{S}}, \; G_\mathrm{M}(s) = \dfrac{K_\mathrm{M}}{1 + sT_\mathrm{M}}, \\ G_\mathrm{R}(s) = \dfrac{1 + (s + j\omega)T_\mathrm{N}}{sT_\mathrm{I}} = \dfrac{1 + sT_\mathrm{N}}{sT_\mathrm{I}} + \dfrac{j\omega T_\mathrm{N}}{sT_\mathrm{I}}, \end{cases} \quad \begin{cases} T_\mathrm{N} = T_\mathrm{S}, \\ T_\mathrm{I} = 2K_\mathrm{S}K_\mathrm{M}T_\mathrm{M}, \end{cases} \quad \begin{cases} T_\mathrm{S} = \dfrac{L_\sigma}{R_\sigma}, \\ K_\mathrm{S} = \dfrac{1}{R_\sigma}, \end{cases} \tag{9}$$

$$G_0(s) = G_\mathrm{R}(s)G_\mathrm{M}(s)G_\mathrm{S}(s) = \frac{1 + (s + j\omega)T_\mathrm{N}}{sT_\mathrm{I}} \frac{K_\mathrm{M}}{1 + sT_\mathrm{M}} \frac{K_\mathrm{S}}{1 + (s + j\omega)T_\mathrm{S}} = \frac{1}{s2T_\mathrm{M}} \frac{1}{1 + sT_\mathrm{M}}. \tag{10}$$

The open-loop transfer function $G_0(s)$ of the whole system is given by Eq. (10) and is illustrated in Fig. 10(b). The controller time constants were set in such a way that the open-loop transfer function crossed the zero axis with a slope of -20 dB/dec and a phase margin of 63° was kept, ensuring the stability of the system. The bandwidth of the system was limited by the time constant of the modulator.

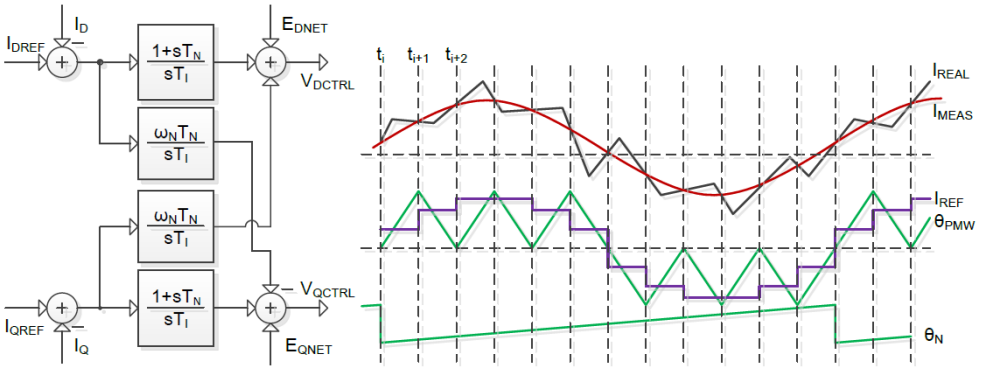


(a) (b)

Fig. 10: (a) Principle of feedback control; (b) system bandwidth

Finally, the control principle of the multivariable PI controller, leading to the control equation described in Eq. (11), is illustrated in Fig. 11(a). The sampling of the measurement and the control is synchronized with the triangle of the pulse width modulation (PWM), which is synchronized with the PLL as illustrated in Fig. 11(b), as described in Ref. [20]. In such a way, one can operate the power converter at low frequencies by ensuring symmetry in the current signal. Moreover, the current measurement is performed between two switching events, where an average value between two peaks is considered naturally and additional filters adding unnecessary phase shifts are not required:

$$\begin{cases} V_{\mathrm{D}} = \dfrac{1+sT_{\mathrm{N}}}{sT_{\mathrm{I}}} I_{\mathrm{Derr}} + \dfrac{\omega T_{\mathrm{N}}}{sT_{\mathrm{I}}} I_{\mathrm{Qerr}}, \\ V_{\mathrm{Q}} = \dfrac{1+sT_{\mathrm{N}}}{sT_{\mathrm{I}}} I_{\mathrm{Qerr}} + \dfrac{\omega T_{\mathrm{N}}}{sT_{\mathrm{I}}} I_{\mathrm{Derr}}. \end{cases} \tag{11}$$



(a) (b)

Fig. 11: Principle of (a) the multivariable PI controller and (b) sampling/modulation

4.2 Control of the current in an asymmetric grid

An approach similar to the decoupling of network voltages presented in the previous section was adopted to obtain four decoupled components from the measured currents. The current controller presented in this paper was implemented in the HIL simulation model. The control platform had its own individual

sampling system, but the controller sampling and the pulse width modulator were synchronized with the PLL of the network, as illustrated in Fig. 11(b), for all switching frequencies tested in the work described in this section. The second-harmonic component appearing in the voltages can be compensated by the current controller only if the bandwidth of the system allows it. As shown in the previous section, the control loop bandwidth depends mainly on the modulator, and specifically on the converter switching frequency.

To illustrate the bandwidth limitations of the controller, the power converter was operated at 450 Hz. The current controller was tested with two current steps under conditions of phase voltage imbalance. As illustrated in Fig. 12(b), the measurement of the four voltage components was not affected by the low switching frequency. One can see in Fig. 12(c) the accuracy of the decoupling between the direct and the quadrature components performed by the multivariable PI controller. Also, the currents do not seem to be affected by the transient that appears when the voltage imbalance occurs. However, Fig. 12(d) shows a negative sequence appearing in the currents, indicating that current balance is not ensured owing to a lack of bandwidth on the controller side.

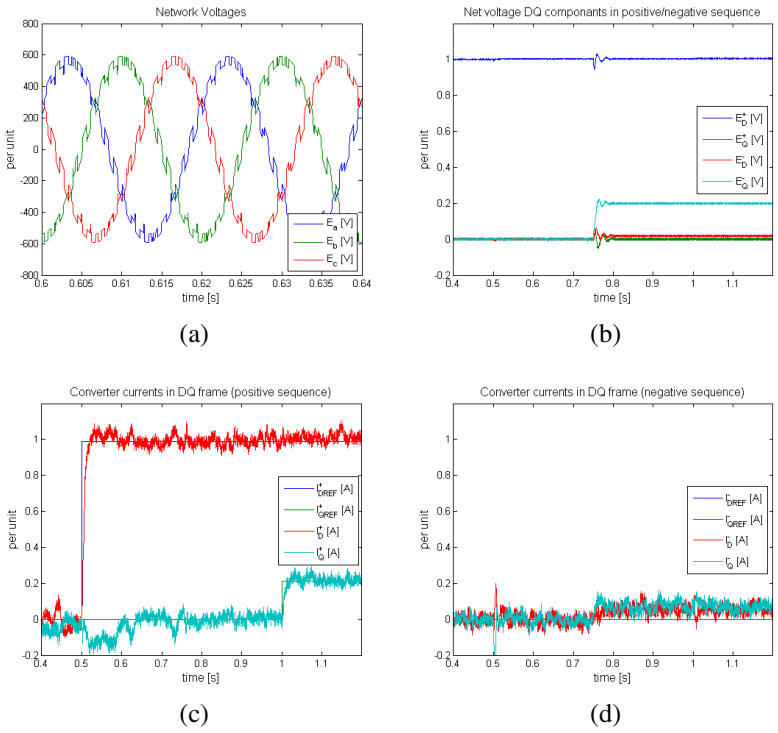


Fig. 12: Operation at 450 Hz switching frequency: (a) phase voltages under balanced conditions, (b) decoupled voltage components, (c) currents and references in the positive sequence, and (d) the negative sequence.

4.3 Balance control of the three phase currents under asymmetric phase voltage conditions

In order to accurately control each of the four current components distributed in the two rotating reference frames, two current controllers are needed, one for each rotating frame, with a proper decoupling of the four components. The *double-decoupled synchronous-reference-frame multivariable PI current controller*, illustrated in Fig. 13, consists of two single-frame current controllers implemented in mirror form for both the positive and the negative sequence.

In the positive reference frame, the direct and quadrature current references I^+_{DREF} and I^+_{QREF} are applied to the two cross-coupled PI controllers regulating the network currents I^+_{D} and I^+_{Q} before the decoupled network voltages E^+_{D} and E^+_{Q} are applied as a feedforward signal. In the negative frame, the

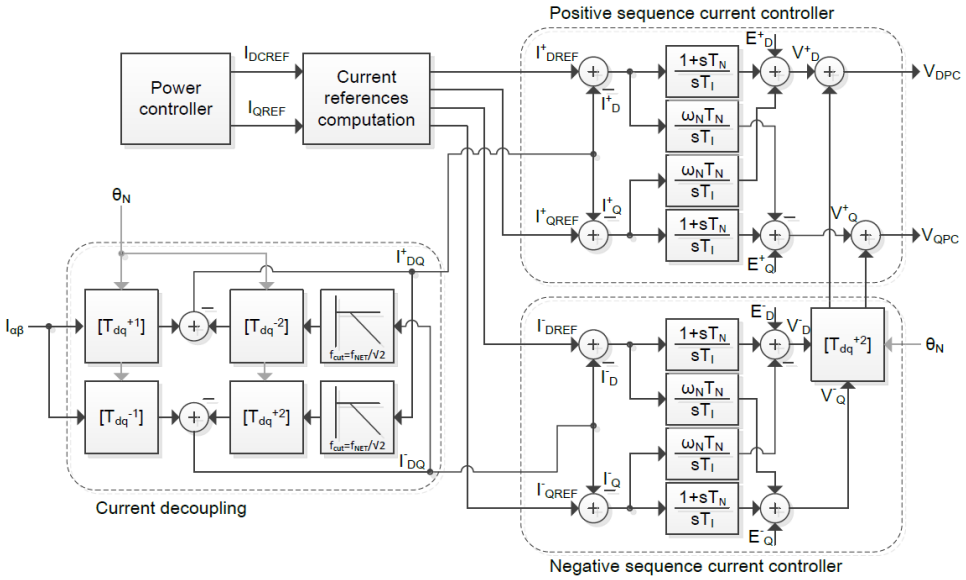


Fig. 13: Double-decoupled synchronous-reference-frame multivariable current controller

same scheme is applied in mirror image form, with inverted signs in the cross-coupling contributions. The output voltage reference signals V_{D}^{-} and V_{Q}^{-} are transformed to the positive sequence before being added to V_{D}^{+} and V_{Q}^{+} as a contribution for the unbalanced phase voltages before being applied by the modulator.

The current references I_{DREF}^{-} and I_{QREF}^{-} in the negative sequence can be set to zero to ensure current symmetry in the case of imbalance in the phase voltages. With values different from zero, the current references I_{DREF}^{-} and I_{QREF}^{-} can be used to control the negative-sequence currents in order to introduce imbalance into the phase currents.

The double-frame controller was tested under conditions of voltage imbalance with four current reference steps. Figure 14(b) shows that the currents in the positive sequence were well controlled and decoupled. In the negative sequence, as illustrated in Fig. 14(c), current symmetry could be ensured by control; at the same time, we could control the imbalance freely to obtain currents as in Fig. 14(d). After the decoupling between the direct and the quadrature components of the currents by the multivariable PI approach had been verified, Fig. 14(b) shows that a small transient appeared in the negative sequence when a current step was applied in the positive sequence. The reason comes from the necessary filtering applied to the feedback signals and the fact that the sudden phase imbalance appears as a step in time.

5 Power considerations

The previous section introduced a simple way to control the four components of the phase current, independently of the state of balance of the phase voltages. When imbalance occurs, the second harmonic appearing in the phase voltages affects the instantaneous power seen at the point of common coupling. If uncontrolled, the phase currents tend to have an imbalance in the same direction as the imbalance in the phase voltages. This strongly affects the instantaneous power as seen at the point of common coupling and also on the DC link side, as pointed out in Ref. [21]. When a phase voltage imbalance occurs and the controller maintains symmetry in the phase currents, the second harmonic in the instantaneous power is considerably reduced, and the ripple in the DC link voltage is reduced at the same time. Another way is to act on the current references so as to impose an imbalance in the phase currents to counter the phase voltage imbalance. For this compensation to be implemented, the instantaneous power must be computed as a function of the four current and four voltage components to assess the current references as a function of the voltage imbalance.

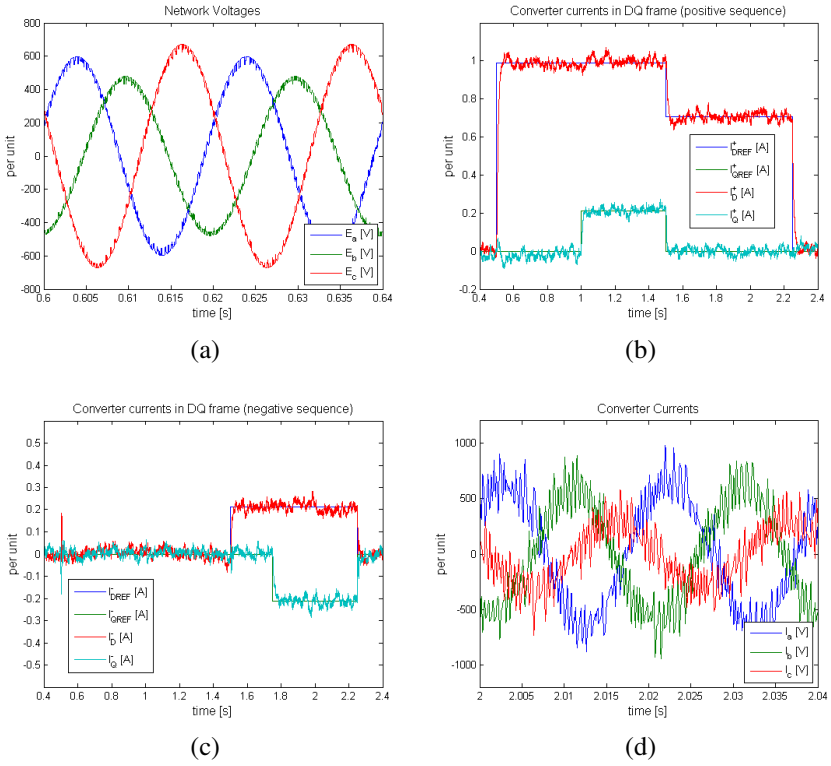


Fig. 14: Double-frame current control: (a) phase voltage imbalance, (b) current control in the positive sequence, (c) current control in the negative sequence, and (d) resulting phase currents.

5.1 Power oscillations during network imbalance

When an asymmetric perturbation occurs in the phase voltages, as in Fig. 15(a), and if symmetric current operation is maintained as in Fig. 15(c), a second harmonic appears in the computation of the active and reactive instantaneous power as in Fig. 15(d). This power oscillation is even stronger if the negative sequence of the current is not controlled, since the current imbalance tends to be in the same direction as the voltage imbalance (as in Figs. 12(b) and 12(d)). A simple relationship established in Ref. [22] links the power ripple to the DC link ripple, as shown in Eq. (12):

$$V_{\mathrm{DCripple}} = \frac{P_{\mathrm{ripple}}}{2C_{\mathrm{DC}}\omega V_{\mathrm{DC}}}. \tag{12}$$

There is an evident relationship between the voltage ripple and the value of the DC link capacitance, which in industrial applications tends to be as low as possible. Therefore, to maintain the DC voltage ripple at its minimum, one must act on the power ripple either by operating with symmetric currents or by compensating the phase voltage imbalance with an opposite phase current imbalance.

5.2 Elements of instantaneous-power theory

One approach to defining the reactive instantaneous power was introduced in Japan in the 1980s and has been considered as a reference [23–25]. In contrast to the German approach known as the FBD method [26], this instantaneous-power theory has led to many further developments and attempts to find a unified theory. Some other approaches that have introduced different definitions of power components, such as Refs. [27, 28], have shown the state of uncertainty and lack of agreement in the scientific community [29–32]. In the Japanese approach, the apparent power is a combination of continuous parts P_{NET} and Q_{NET} and four redundant second-harmonic oscillating parts $P_{2\mathrm{C}}$, $P_{2\mathrm{S}}$, $Q_{2\mathrm{C}}$, and Q_{S}, as in Eq. (13). The

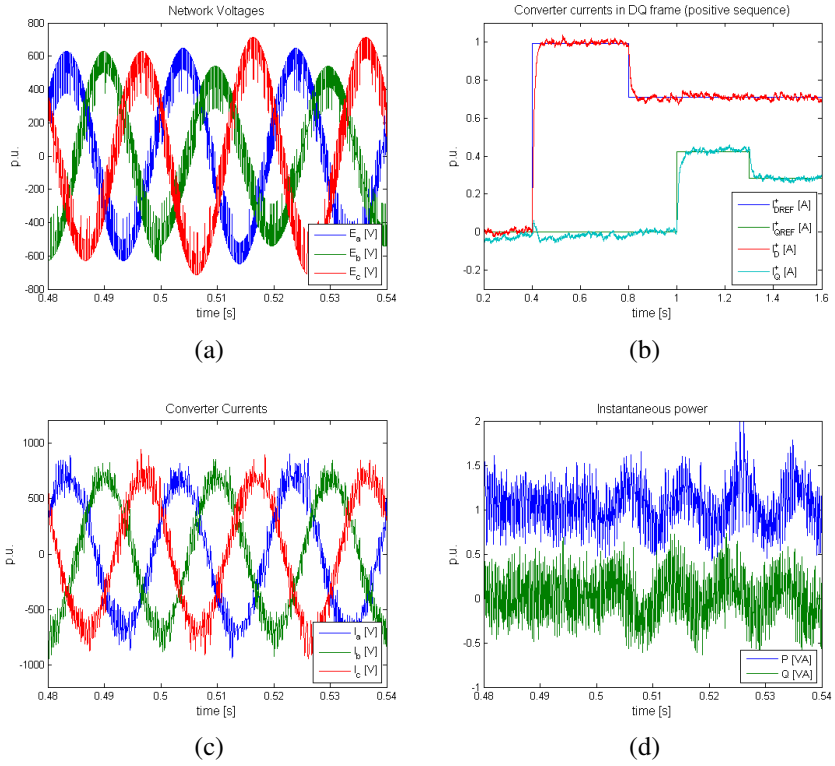


Fig. 15: Power considerations for unbalanced network: (a) phase voltages, (b) control of positive-sequence currents, (c) resulting phase currents, and (d) instantaneous active and reactive power.

active and reactive power are found by taking the real and imaginary parts, respectively, of the apparent complex power S_{NET}:

$$S_{\mathrm{NET}} = (P + P_{2\mathrm{C}}\cos(2\omega t) + P_{2\mathrm{S}}\sin(2\omega t)) + j(Q + Q_{2\mathrm{C}}\cos(2\omega t) + Q_{2\mathrm{S}}\sin(2\omega t)). \tag{13}$$

The concept of the quadrature complex power T_{NET} was introduced in Ref. [33]. The reactive power is calculated on the basis of the conjugate current vector I^{*}_{DQS} and a voltage vector E'_{DQS} lagging the pole voltage vector E_{DQS} by 90°. Following this approach, the active power P_{NET} is the real part of the apparent complex power S_{NET} and the reactive power Q_{NET} is the real part of the quadrature complex power T_{NET} as in Eq. (14):

$$\begin{cases} S_{\mathrm{NET}} = \frac{3}{2} E_{\mathrm{DQS}} I^{*}_{\mathrm{DQS}}, \\ T_{\mathrm{NET}} = \frac{2}{3} E'_{\mathrm{DQS}} I^{*}_{\mathrm{DQS}}, \end{cases} \quad \begin{cases} I^{*}_{\mathrm{DQS}} = e^{j\omega_{\mathrm{N}} t} I^{+}_{\mathrm{DQ}} - e^{-j\omega_{\mathrm{N}} t} I^{-}_{\mathrm{DQ}}, \\ E_{\mathrm{DQS}} = e^{j\omega_{\mathrm{N}} t} E^{+}_{\mathrm{DQ}} + e^{-j\omega_{\mathrm{N}} t} E^{-}_{\mathrm{DQ}}, \\ E'_{\mathrm{DQS}} = -j e^{j\omega_{N} t} E^{+}_{\mathrm{DQ}} + j e^{-j\omega_{\mathrm{N}} t} E^{-}_{\mathrm{DQ}}, \end{cases} \quad \begin{cases} P_{\mathrm{NET}} = \mathrm{Re}\left\{S_{\mathrm{NET}}\right\}, \\ Q_{\mathrm{NET}} = \mathrm{Re}\left\{T_{\mathrm{NET}}\right\}. \end{cases} \tag{14}$$

In any case, the instantaneous power components can be computed as in Eq. (15) and can serve as a basis for the computation of the compensation, in a way similar to that proposed in Ref. [34]:

$$\begin{bmatrix} P \\ Q \\ P_{2\mathrm{C}} \\ P_{2\mathrm{S}} \end{bmatrix} = \frac{3}{2} \begin{bmatrix} E^{+}_{\mathrm{D}} & E^{+}_{\mathrm{Q}} & E^{-}_{\mathrm{D}} & E^{-}_{\mathrm{Q}} \\ E^{+}_{\mathrm{Q}} & -E^{+}_{\mathrm{D}} & -E^{-}_{\mathrm{Q}} & E^{-}_{\mathrm{D}} \\ E^{-}_{\mathrm{D}} & E^{-}_{\mathrm{Q}} & E^{+}_{\mathrm{D}} & E^{+}_{\mathrm{Q}} \\ E^{-}_{\mathrm{Q}} & -E^{-}_{\mathrm{D}} & -E^{+}_{\mathrm{Q}} & E^{+}_{\mathrm{D}} \end{bmatrix} \begin{bmatrix} I^{+}_{\mathrm{D}} \\ I^{+}_{\mathrm{Q}} \\ I^{-}_{\mathrm{D}} \\ I^{-}_{\mathrm{Q}} \end{bmatrix}. \tag{15}$$

5.3 Compensation methods

The relation presented in Eq. (15) is the starting point for establishing current references for reducing the second-harmonic content of the active power. By setting the oscillatory parts P_{2C} and P_{2S} of the complex power to zero, one can perform a simple matrix computation of the voltages to find the corresponding current references. This approach was introduced in Ref. [35]. Another method was introduced in Ref. [36], which considered the voltage drop across the filter impedance; in this reference, the original approach was criticized for containing a singularity. As demonstrated in Ref. [11], however, the second approach contained the same singularity. Finally, a third similar approach was introduced in Ref. [37], in which the strength of the network was considered. But, from the point of view of current control, none of those three methods can be distinguished from the others. Therefore, only the original method, described by Eq. (16), is presented here, for simplicity:

$$\begin{bmatrix} I_{\mathrm{D}}^{+} \\ I_{\mathrm{Q}}^{+} \\ I_{\mathrm{D}}^{-} \\ I_{\mathrm{Q}}^{-} \end{bmatrix} \approx \begin{bmatrix} E_{\mathrm{D}}^{+} & E_{\mathrm{Q}}^{+} & E_{\mathrm{D}}^{-} & E_{\mathrm{Q}}^{-} \\ E_{\mathrm{Q}}^{+} & -E_{\mathrm{D}}^{+} & -E_{\mathrm{Q}}^{-} & E_{\mathrm{D}}^{-} \\ E_{\mathrm{D}}^{-} & E_{\mathrm{Q}}^{-} & E_{\mathrm{D}}^{+} & E_{\mathrm{Q}}^{+} \\ E_{\mathrm{Q}}^{-} & -E_{\mathrm{D}}^{-} & -E_{\mathrm{Q}}^{+} & E_{\mathrm{D}}^{+} \end{bmatrix}^{-1} \begin{bmatrix} P \\ Q \\ 0 \\ 0 \end{bmatrix}. \tag{16}$$

The original method consists in solving the equations given in Eq. (16), where the current references are computed from the four components of the phase voltages as seen at the point of common coupling. The determinant Det of the condition matrix is calculated as in Eq. (17). A singularity appears when D reaches zero, and therefore this method is limited and cannot compensate for a full phase loss.

$$\begin{bmatrix} I_{\mathrm{DREF}}^{+} \\ I_{\mathrm{QREF}}^{+} \\ I_{\mathrm{DREF}}^{-} \\ I_{\mathrm{QREF}}^{-} \end{bmatrix} \approx \frac{P}{D} \begin{bmatrix} E_{\mathrm{D}}^{+} \\ E_{\mathrm{Q}}^{+} \\ -E_{\mathrm{D}}^{-} \\ -E_{\mathrm{Q}}^{-} \end{bmatrix} + \frac{Q}{D} \begin{bmatrix} E_{\mathrm{Q}}^{+} \\ -E_{\mathrm{D}}^{+} \\ E_{\mathrm{Q}}^{-} \\ -E_{\mathrm{D}}^{-} \end{bmatrix} \begin{cases} \mathrm{Det} = -D^2, \\ D = \left[(E_{\mathrm{D}}^{+})^2 + (E_{\mathrm{Q}}^{+})^2 \right] - \left[(E_{\mathrm{D}}^{-})^2 + (E_{\mathrm{Q}}^{-})^2 \right]. \end{cases} \tag{17}$$

A simulation of the power converter was run with the previously presented double-frame controller under several conditions of phase voltage balance and imbalance. The power compensation approach was implemented as a function of the four components of the phase voltages to compute the four current references. The system was run with several steps in the active and reactive currents, and the four current references were computed as a function of the four voltage components.

From the point of view of current control, all three compensation methods showed exactly the same results as for compensation of the active power at the point of common coupling, regardless of the strength of the network, the switching frequency, or the value of the line impedance on the power converter side. The compensation of the active-power oscillations could therefore be done by the method suggested in Ref. [35], which requires the lowest computation effort. When voltage imbalance appeared, the current references were all adjusted as in Figs. 16(a) and 16(b). As predicted, the resulting phase currents, illustrated in Fig. 16(c), allowed us to compensate the active-power oscillations as in Fig. 16(d) by increasing the reactive-power oscillations.

As long as the phase voltage dip is within some established limits, given by the condition that the positive-sequence components of the voltage remain higher than the negative-sequence components, one can increase the corresponding phase current to maintain the instantaneous active-power balance on the network side. Such operation is obviously limited by converter limits such as the maximum semiconductor device current, and the maximum phase voltage dip that can be handled by such a control method is dependent on the operating point of the whole power converter at the moment of the phase voltage dip.

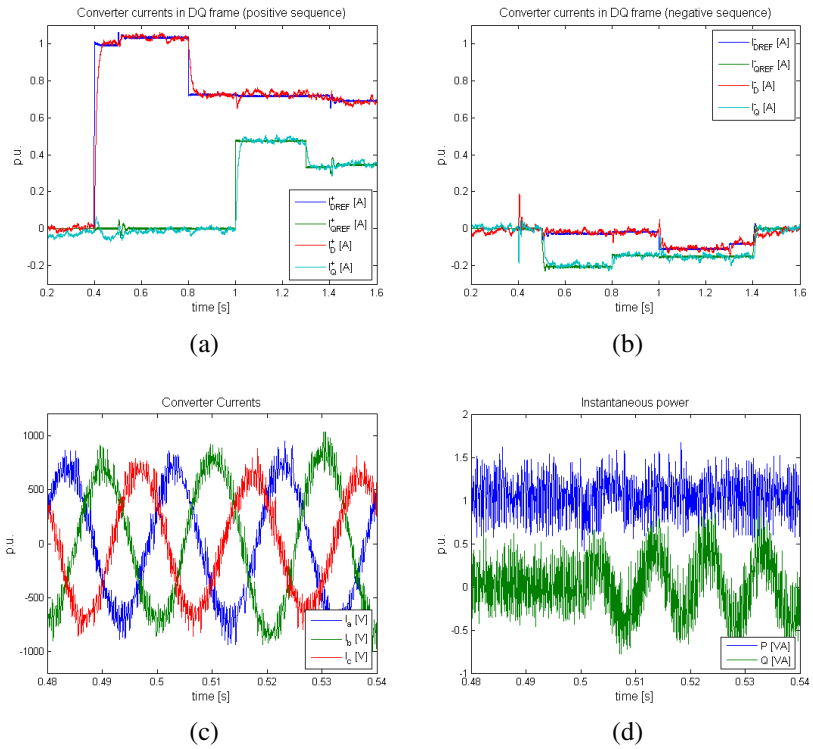


Fig. 16: (a) Active-power-oscillation compensation with current references in the positive sequence, (b) computed current references in the negative sequence, (c) resulting phase currents, and (d) instantaneous active and reactive power.

6 Conclusions

When a voltage source inverter is operated with any type of grid, the synchronization must be robust enough to be able to reject all harmonics coming from the grid, as well as from the power converter itself. With respect to rejecting the second-harmonic component due to phase voltage imbalance and ensuring good PLL dynamics at the same time, the use of a decoupling method for the positive and negative sequences proved to be sufficiently accurate and allowed the current controller to work with four decoupled voltage components to handle asymmetries.

The current controller, when optimally tuned, showed its limitations in terms of bandwidth, especially at low switching frequencies. For the proper handling of currents under conditions of voltage asymmetry, feeding the decoupled values of the voltage forward is already a step forward. However, to ensure current symmetry, a second frame controller must be implemented to ensure zero values in the negative sequence of the currents.

One can control the current imbalance in such a way that the active-power oscillations due to voltage imbalance are reduced. A current reference computation method based on instantaneous-power theories has been presented and implemented. For phase dips down to a certain level, this compensation proved to work accurately, as long as the semiconductors allowed an increase in the current in some of the phases.

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One-Quadrant Switched-Mode Power Converters

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Abstract
This article presents the main topics related to one-quadrant power converters. The basic topologies are analysed and a simple methodology to obtain the steady-state output–input voltage ratio is set out. A short discussion of different methods to control one-quadrant power converters is presented. Some of the reported derived topologies of one-quadrant power converters are also considered. Some topics related to one-quadrant power converters such as synchronous rectification, hard and soft commutation, and interleaved converters are discussed. Finally, a brief introduction to resonant converters is given.

Keywords
One-quadrant; converter; topology; switch-mode; magnet; energy.

1 Introduction

Switched-mode power converters are a very efficient way to transfer energy from a source to a load. A switched-mode power converter is formed from switches, inductors, and capacitors. If these components are ideal, they do not dissipate energy, and the efficiency of the power converter is 100%. A further advantage of switched-mode power converters is the increase in power density that has occurred in recent years. The power density is defined as the ratio between the nominal power of the converter and its volume. This power density has been constantly increasing owing to an increasing switching frequency.

As this is a broad topic, there are several different ways to classify switched-mode power converters. The one-quadrant power converters are those with the capability to provide an output in only one quadrant of a plot of output voltage versus output current. These converters have the capability to transfer energy in only one direction. Most one-quadrant converters can also be classified as DC–DC converters. The main application of these converters is in voltage regulation. In this application, a non-regulated voltage, which is usually provided by a diode rectifier stage, is converted to a regulated output voltage which is not affected by the grid or variations in the load.

This article gives an introduction to one-quadrant power converters. It presents the basic, or direct, DC–DC converter topologies, showing typical waveforms and the basic design equations. The basic concepts of regulation and control of DC–DC converters are also discussed. Section 4 presents some of the most typical derived converter topologies reported in the literature. Some topics related to one-quadrant power converters, such as synchronous rectification, interleaving, and soft commutation, are presented in Section 5. Finally, resonant converters are briefly mentioned.

1.1 One-quadrant switched-mode power converters in particle accelerators

The main application of one-quadrant power converters is in storage ring particle accelerators. These accelerators are the key components of synchrotron radiation light source facilities. A storage ring is a particle accelerator where the particles circulate around a ring for several hours while their energy is maintained constant. As the energy of the particles is constant, the magnetic fields used for bending and focusing the particle beam are also constant. These magnetic fields are generated by currents provided by high-precision, stable power supplies. The precision and stability of these converters are of the order of several parts per million.

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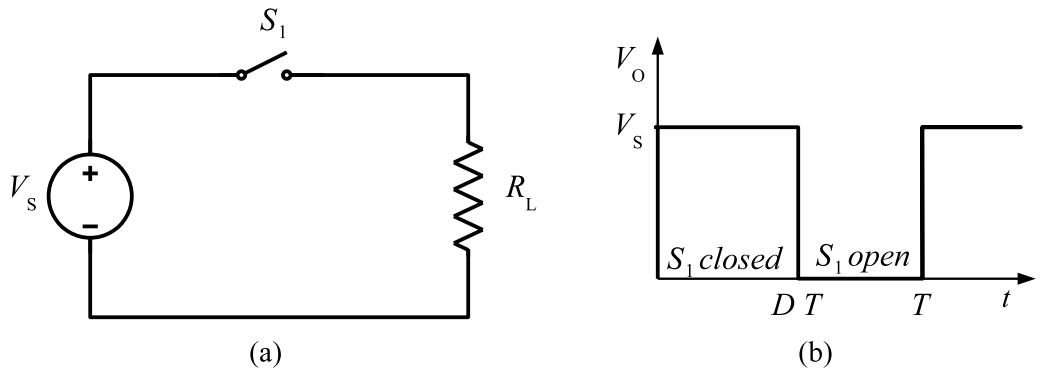

Fig. 1: Simple DC chopper: (a) circuit diagram; (b) output voltage waveform

2 Basic one-quadrant power converter topologies

This section provides a short introduction to the basic topologies of one-quadrant power converters. These basic topologies are also known as direct DC–DC converters. One characteristic of these topologies is that they are built using only one commutation cell. A brief description, a methodology for the analysis of these topologies, and key design equations are presented. First, the DC chopper converter is discussed as an introduction and to show how the average output voltage of a converter can be modified using 'on–off' switches. The basic topologies considered are the buck, boost, and buck–boost converters.

2.1 DC chopper

The simplest one-quadrant converter is the DC chopper, shown in Fig. 1. This consists of a DC input voltage source, a controllable switch, and a load resistor. When the switch is closed, the input voltage is applied to the resistor. This is defined as the 'on' state of the converter. When the switch is open, the current through the resistor is zero and the voltage is zero. This is called the 'off' state of the converter.

The switch can be operated with a duty ratio D, defined as the ratio of the on time of the switch to the sum of the on and off times. For constant-frequency operation,

$$D = \frac{t_{\rm on}}{t_{\rm on} + t_{\rm off}} \frac{t_{\rm on}}{T}, \tag{1}$$

where $T = 1/f$ is the period of the switching frequency f. The average value of the output voltage is

$$V_{\rm O} = DV_{\rm S}. \tag{2}$$

This average output voltage can be regulated by adjusting the duty cycle D.

The circuit shown in Fig. 1 is not a 'practical' circuit. The main reason for this is that it is not possible to build pure resistive elements. In practice, the connection of devices and circuit elements creates stray inductances that have to be taken into account. A circuit including the stray inductance of the load is shown in Fig. 2.

The inclusion of the inductance of the load leads to a need to provide a path for the current in the inductor. This is to comply with the 'rule' of power electronics that a current source that is like an inductor must not be open-circuited. Two circuits are defined according to the state of the switch; these circuits are shown in Fig. 3. The current paths are shown in red.

The load voltage and current are plotted in Fig. 4 under the assumptions that the load current never reaches zero and the time constant of the load $\tau = L_{\rm L}/R_{\rm L}$ is much greater than the period T. The average values of the output voltage and current can be adjusted by changing the duty ratio D. This is the principle of control of switched-mode power converters.

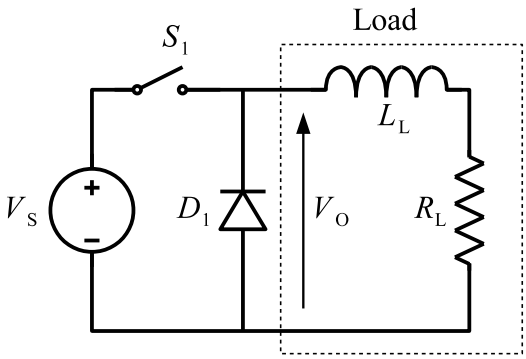

Fig. 2: DC chopper with inductive load

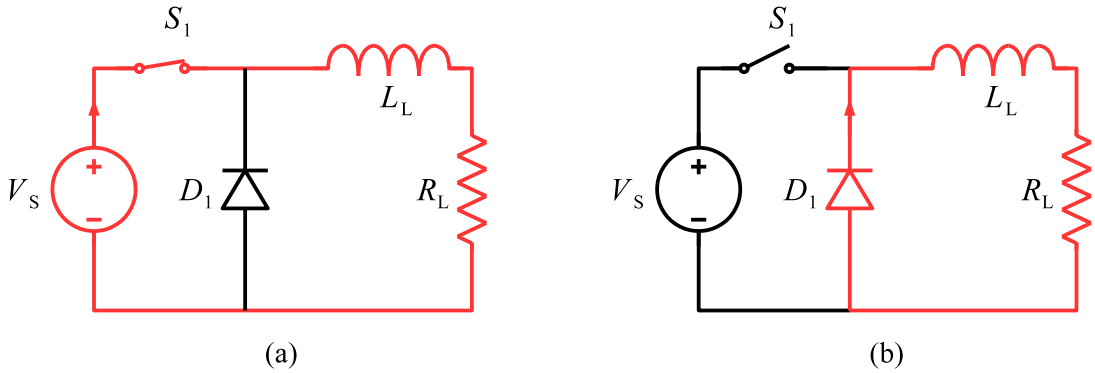

Fig. 3: DC chopper: (a) current path in on state; (b) current path in off state

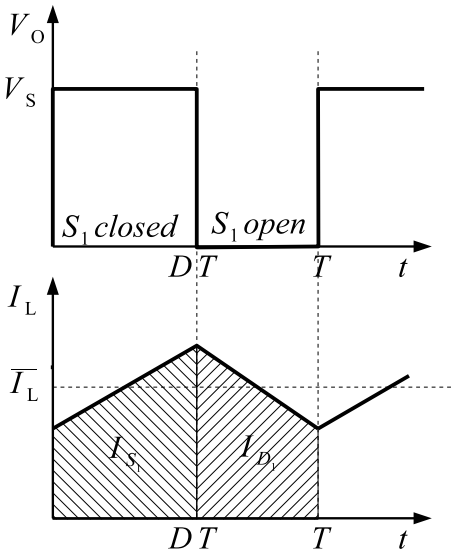

Fig. 4: DC chopper: output voltage and load current

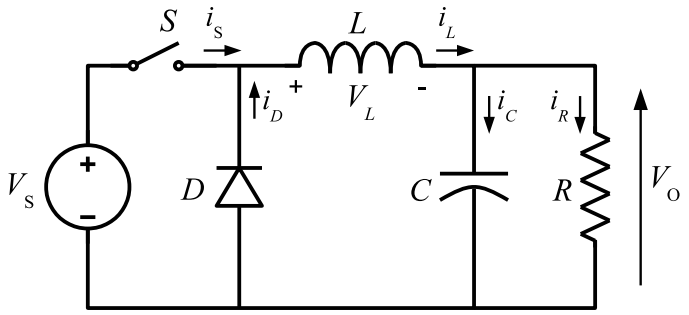

Fig. 5: Buck (step-down) converter

2.2 Buck converter

The addition of a capacitor to the circuit of Fig. 2 leads to the first topology of basic, or direct, DC–DC converters. These are step-down converters and are commonly known as buck converters. The basic circuit diagram of a buck converter is shown in Fig. 5. It consists of a DC input voltage source $V_{\rm S}$, a controlled switch S, a diode D, a filter inductor L, a filter capacitor C, and a load resistance R.

DC–DC converters can operate in two distinct modes with respect to the inductor current i_L. Figure 6 depicts the continuous conduction mode (CCM), in which the inductor current is always greater than zero. When the average value of the input current is low (high R) and/or the switching frequency f is low, the converter may enter the discontinuous conduction mode (DCM). In the DCM, the inductor current is zero during a portion of the switching period.

Typical waveforms of the converter in the CCM are shown in Fig. 6. It can be seen from the circuit that when the switch S is commanded to the on state, the diode D is reverse biased. When the switch S is off, the diode conducts so as to support an uninterrupted current in the inductor.

The relationships among the input voltage, the output voltage, and the switch duty ratio D can be derived from, for instance, the waveform of the inductor voltage V_L (Fig. 6). According to Faraday's law, the volt-second product for the inductor over a period of steady-state operation should be zero. For the buck converter,

$$(V_{\rm S} - V_{\rm O})DT = V_{\rm O}(1 - D)T. \tag{3}$$

From Eq. (3), the steady-state DC voltage transfer function, defined as the ratio of the output voltage to the input voltage, is

$$M_{\rm V} \equiv \frac{V_{\rm O}}{V_{\rm S}} = D. \tag{4}$$

It can be seen from Eq. (4) that the output voltage is always smaller than the input voltage.

The CCM is preferred over the DCM because it provides higher efficiency and makes better use of semiconductor switches and passive components. The DCM may be used in applications with special control requirements, since the dynamic order of the converter is reduced (the energy stored in the inductor is zero at the beginning and end of each switching period). It is uncommon to mix these two operating modes, because different control algorithms are needed. For the buck converter, the critical value of the inductance which is needed for CCM operation is

$$L_{\rm b} = \frac{(1 - D)R}{2f}. \tag{5}$$

The current i_L in the filter inductor in the CCM consists of a DC component $I_{\rm O}$ with a superimposed triangular AC component. Almost all of this AC component flows through the filter capacitor as a current i_C. The current i_C causes a small voltage ripple in the DC output voltage $V_{\rm O}$. To limit the

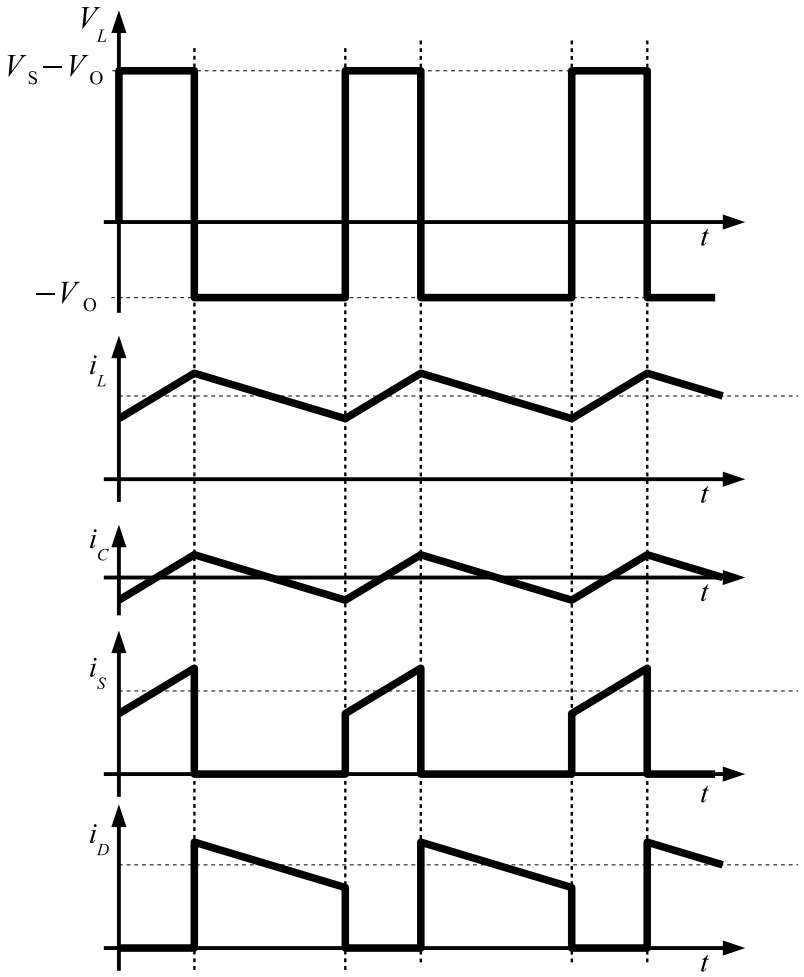

Fig. 6: Waveforms for buck converter

peak-to-peak value of the ripple voltage below a certain value V_r, the filter capacitance C must be greater than

$$C_{\text{MIN}} = \frac{(1-D)V_O}{8V_r L f^2}. \tag{6}$$

Equations (5) and (6) are the key design equations for the buck converter. The input and output DC voltages (and, hence, the duty ratio D) and the range of the load resistance R are usually determined by preliminary specifications. The designer needs to determine the values L and C of the passive components, and the switching frequency f. The value L of the filter inductor is calculated from the CCM/DCM condition using Eq. (5).

The value C of the filter capacitor is obtained from the voltage ripple condition (Eq. (6)). For compactness and low conduction losses in the converter, it is desirable to use small passive components. Equations (5) and (6) show that this can be accomplished by using a high switching frequency f. The switching frequency is limited, however, by the type of semiconductor switches used and by switching losses. It should also be noted that values of L and C may be altered by the effects of parasitic components in the converter, especially the equivalent series resistance of the capacitor.

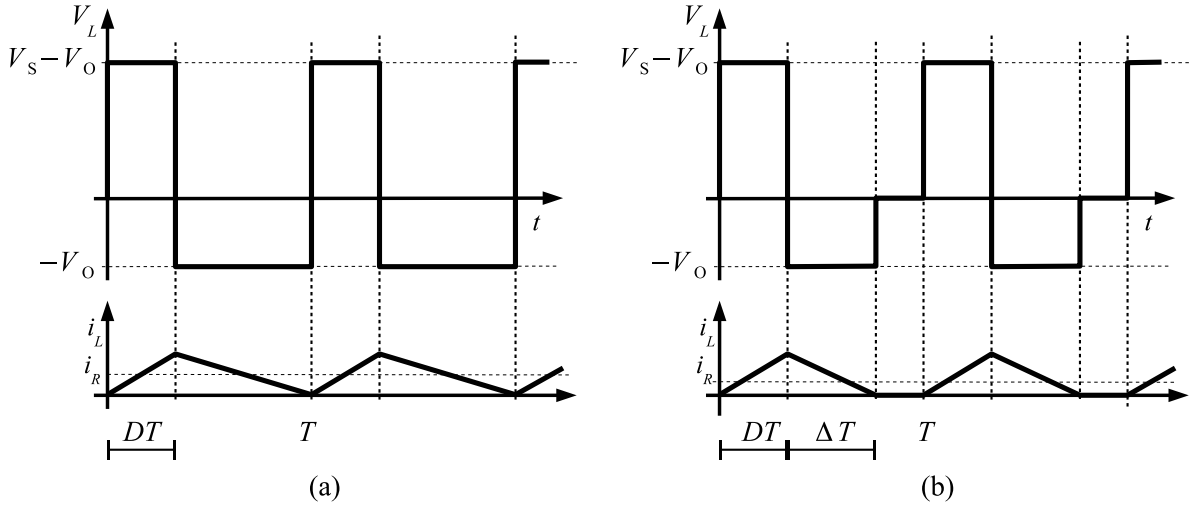

Fig. 7: CCM and DCM: (a) boundary condition waveforms; (b) DCM waveforms

2.2.1 Discontinuous current mode

Whether the converter operates in the CCM or the DCM depends on the load on the converter. If the value of the output resistance increases beyond the value used in Eq. (5), the converter starts to operate in the DCM. Figure 7(a) shows the waveforms of the inductor voltage v_L and inductor current i_L at the edge of the CCM. The value of the output current i_R is also shown in the plot. This value is the average of the inductor current over a period T.

The output current i_R for the condition at the boundary between the two modes is given by

$$i_{R\mathrm{B}} = \frac{DT}{2L}(V_\mathrm{S} - V_\mathrm{O}) = \frac{TV_\mathrm{S}}{2L}(D - D^2). \tag{7}$$

The output current required in the CCM is maximum for

$$I_{R\mathrm{B}_\mathrm{MAX}} = \frac{TV_\mathrm{S}}{8L}. \tag{8}$$

Figure 8 shows a plot of the minimum output current for CCM operation as a function of the duty cycle D.

The output–input voltage ratio under DCM conditions can be calculated using the waveforms in Fig. 7(b). The volt-second product over a period should be zero for a steady-state condition. Therefore

$$(V_\mathrm{S} - V_\mathrm{O})DT = V_\mathrm{O}\Delta T, \tag{9}$$

$$\frac{V_\mathrm{O}}{V_\mathrm{O}} = \frac{D}{D\Delta}. \tag{10}$$

The output current is the average of the inductor current I_L over the period T:

$$I_R = \frac{I_{L_\mathrm{peak}}(D + \Delta)T}{2T}. \tag{11}$$

Using Eqs. (8) and (11), Eq. (10) can be rewritten as

$$I_R = 4I_{R\mathrm{B}_\mathrm{MAX}} D\Delta. \tag{12}$$

From Eqs. (10) and (13),

$$\frac{V_\mathrm{O}}{V_\mathrm{S}} = \frac{D^2}{\left(D^2 + \frac{1}{4}\frac{I_R}{I_{R\mathrm{B}_\mathrm{MAX}}}\right)}. \tag{13}$$

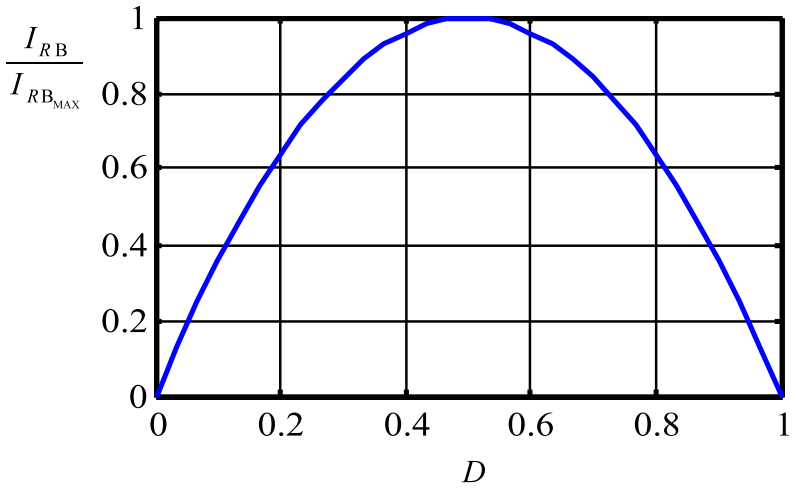

Fig. 8: Minimum output current for CCM versus duty cycle keeping V_S constant

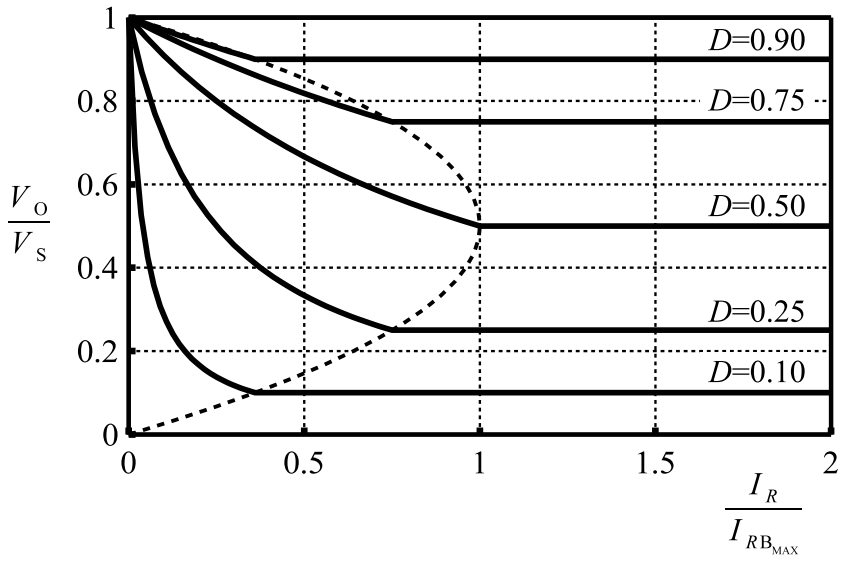

Fig. 9: Buck converter: output–input voltage ratio in DCM and CCM

Figure 9 shows the characteristics of the buck converter for both modes of operation. The voltage ratio is plotted versus the output current for several duty cycles. The boundary between the DCM and CCM is shown by the dashed curve.

2.3 Boost converter

The second topology to be analysed is the step-up, or boost, converter. It receives this name because the output voltage is always higher than the input voltage. Figure 10 depicts a simple circuit diagram of a boost converter. This comprises a DC input voltage source V_S, a boost inductor L, a controlled switch S, a diode D, a filter capacitor C, and a load resistance R. The converter waveforms in the CCM are presented in Fig. 11. When the switch S is in the 'on' state, the current in the boost inductor increases linearly. The diode D is off at this time. When the switch S is turned off, the energy stored in the inductor is released through the diode into the output RC circuit.

Using Faraday's law for the boost inductor,

$$V_S DT = (V_O - V_S)(1 - D)T, \tag{14}$$

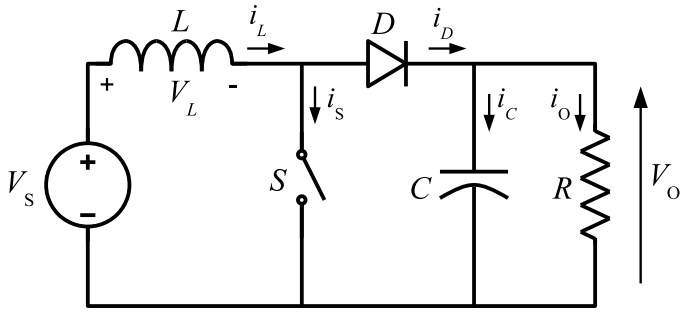

Fig. 10: Boost converter: circuit diagram

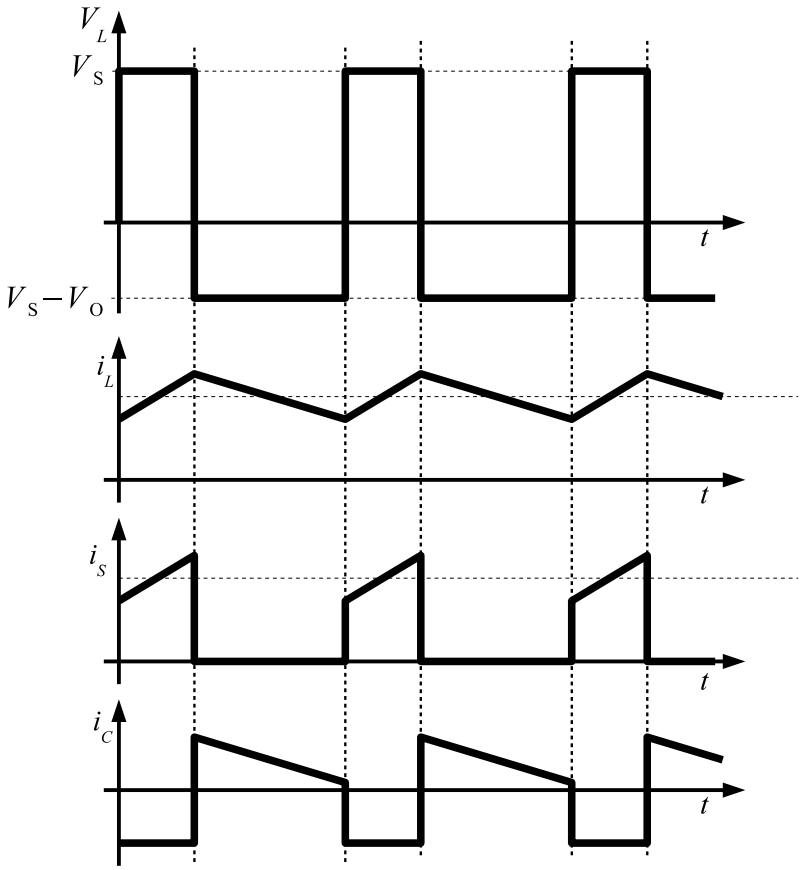

Fig. 11: Waveforms for boost converter

from which the DC voltage transfer function turns out to be

$$M_{\mathrm{V}} \equiv \frac{V_{\mathrm{O}}}{V_{\mathrm{S}}} = \frac{1}{(1-D)}. \tag{15}$$

The boost converter operates in the CCM for $L > L_{\mathrm{b}}$, where

$$L_{\mathrm{b}} = \frac{(1-D)^2 DR}{2f}. \tag{16}$$

The main waveforms of the boost converter are shown in Fig. 11. The current supplied to the RC output filter is discontinuous. Thus, a larger output filter capacitor is required than in the buck converter

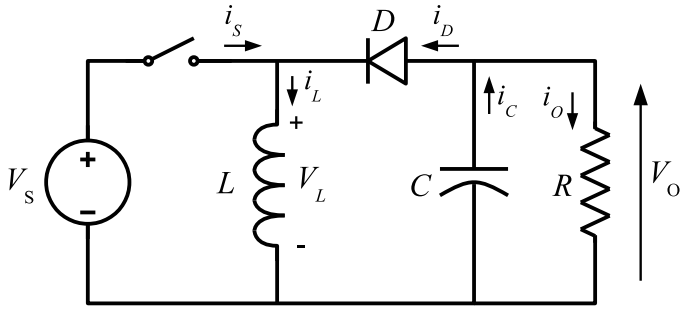

Fig. 12: Buck–boost converter: circuit diagram

in order to limit the output voltage ripple. The output filter capacitor must provide the DC current to the load when the diode D is off. The minimum value of the filter capacitance that results in a voltage ripple V_r is given by

$$C_\mathrm{min} = \frac{DV_\mathrm{O}}{V_\mathrm{r}Rf}. \tag{17}$$

2.4 Buck–boost converter

The last of the basic converter topologies is the buck–boost converter. A circuit diagram is shown in Fig. 12. This converter consists of a DC input voltage source V_S, a controlled switch S, an inductor L, a diode D, a filter capacitor C, and a load resistance R. While the switch S is 'on', the inductor current increases and the diode is maintained 'off'. When the switch is turned off, the diode provides a path for the inductor current. Note the polarity of the diode, which results in its current being drawn from the output. For this reason, the output voltage polarity is negative.

The waveforms for the buck–boost converter are depicted in Fig. 13. The condition for a zero volt-second product for the inductor in the steady state and the steady-state DC transfer function are given by the following equations:

$$V_\mathrm{S}TD = -V_\mathrm{O}(1-D)T, \tag{18}$$

$$M_\mathrm{V} \equiv \frac{V_\mathrm{O}}{V_\mathrm{S}} = \frac{D}{(1-D)}. \tag{19}$$

The critical value of the inductor that fixes the boundary between the CCM and DCM is given by

$$L_\mathrm{b} = \frac{(1-D)^2DR}{2f}. \tag{20}$$

The current that feeds the RC output filter is the same as that for the boost converter but in the reverse direction. Hence the value of the capacitor is given by Eq. (17).

3 Control of DC–DC converters

One of the common features of the power converters presented in the previous section is that the output voltage depends on the duty cycle D, which was defined as the ratio between t_on and the total period of switching T. Changes in the duty cycle produce variations in the output voltage of the converter. In other words, the output voltage can be controlled by changing the duty cycle.

The analysis of a converter from the point of view of control can be performed using the switching function. The switching function is a mathematical tool to represent the state of a power converter. For the basic power converters described above, the switching function has two values. When the switch is

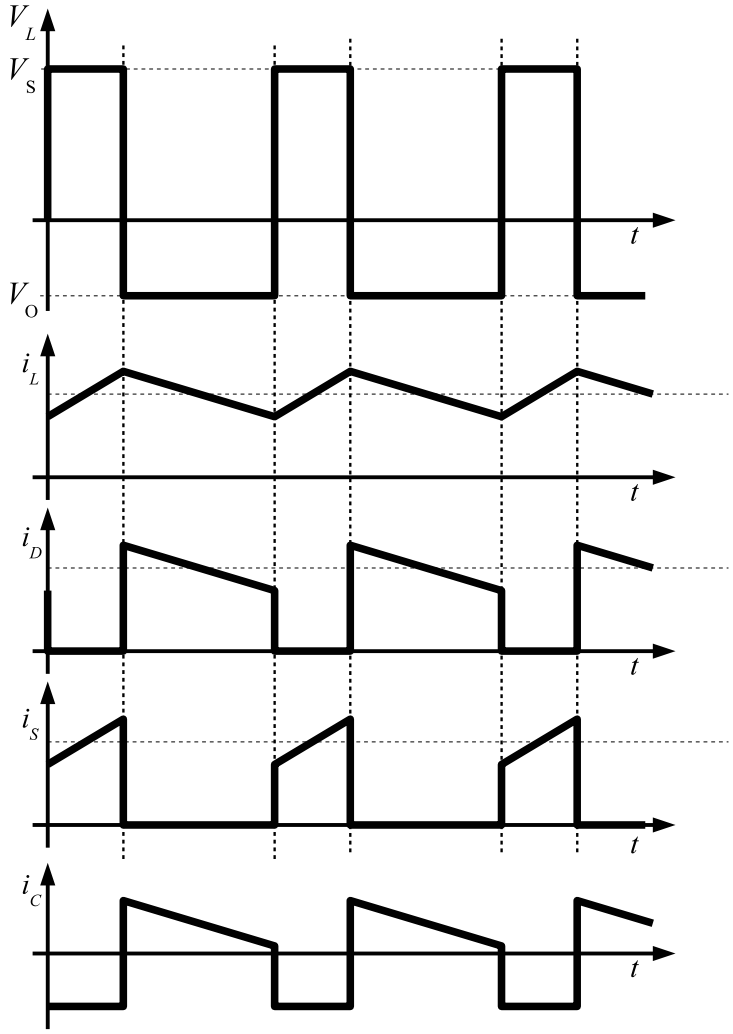

Fig. 13: Waveforms for buck–boost converter

on, the value of the switching function is unity, and when the switch is off, the value is zero:

$$s(t) = \begin{cases} 1 & \text{when the switch is on,} \\ 0 & \text{when the switch is off.} \end{cases} \tag{21}$$

A block diagram of the control of a power converter is shown in Fig. 14. The block labelled "Modulator" transforms an input signal v_D into the switching function $s(t)$, which controls the switch in the power converter. The modulator block can be built in several different ways. It can be implemented using a few analog components or using sophisticated digital circuits.

One of the most common applications of DC–DC converters is to provide a regulated output regardless of variations in the load and the input voltage. Another source of variation in the output voltage is changes in the components of the power converter; components can be affected by external factors such as temperature or ageing. The most common schemes used to regulate the output of power converters are presented in Fig. 15.

The feedback scheme (Fig. 15(a)) uses information from the output to provide the signal v_D to the modulator. The main advantage of this scheme is that a feedback controller receives information directly from the output voltage, which is the value intended to be regulated, and therefore it can compensate for all variations regardless of their source. A disadvantage is that feedback regulation can lead to instability

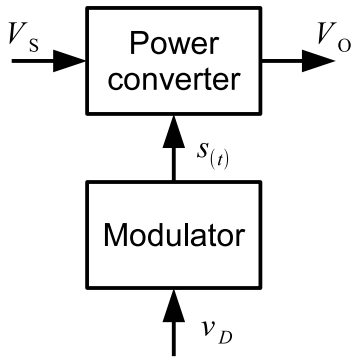

Fig. 14: Block diagram of power converter

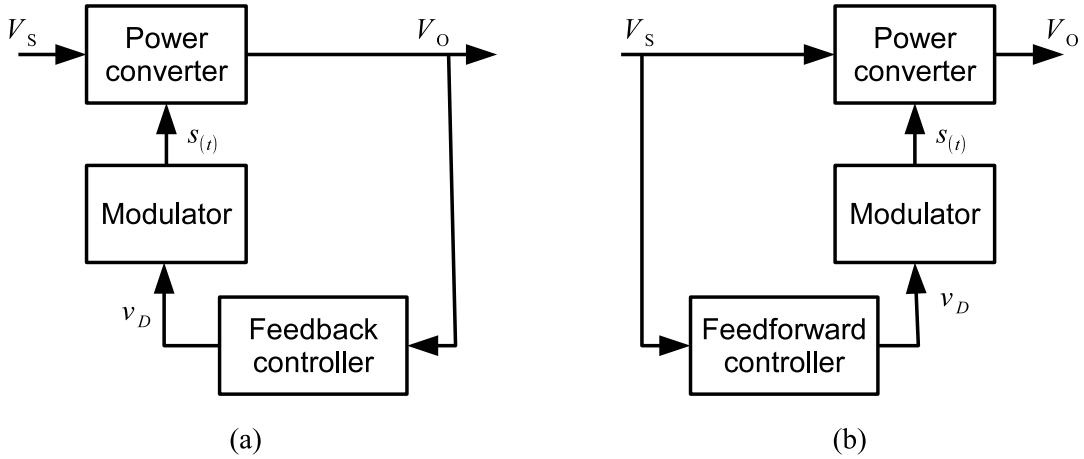

Fig. 15: Block diagrams of regulation schemes: (a) feedback regulation; (b) feedforward regulation

in the converter. Another disadvantage of the feedback scheme is that the output has to be affected in order to provide information to the feedback controller. In other words, the controller may not be fast enough to see a fluctuation and compensate for it. For example, a variation in the input voltage V_S such as 100 Hz ripple from the rectification stage could have an amplitude such that the feedback scheme cannot completely reject it. In such cases a feedforward scheme, as shown in Fig. 15(b), can be used. If it is known how the input voltage affects the output voltage (the DC transfer function), a feedforward controller can provide a signal v_D to the modulator that gives the correct value of the output voltage.

The various ways of obtaining the switching function to be applied to the power converter are referred as control, or modulation, methods. A list and brief discussion of the most common methods are given in the following sections.

3.1 Constant-frequency pulse width modulation (PWM)

This is the most popular method of controlling power converters. In this modulation method, the period of the switching signal T is constant and the information is contained in the width of the pulse, i.e., the period of time for which the switching signal is on, $t_{\rm on}$. This method is also known as carrier-based pulse width modulation. The switching function for constant-frequency PWM can be obtained by comparing the signal v_D with a carrier signal $c(t)$ as depicted in Fig. 16.

Figure 16 shows an analog implementation of a PWM modulator. In digital implementations, the carrier is replaced by a counter/timer block. In both types of implementation, a way to avoid multiple transitions within a carrier period needs to be added.

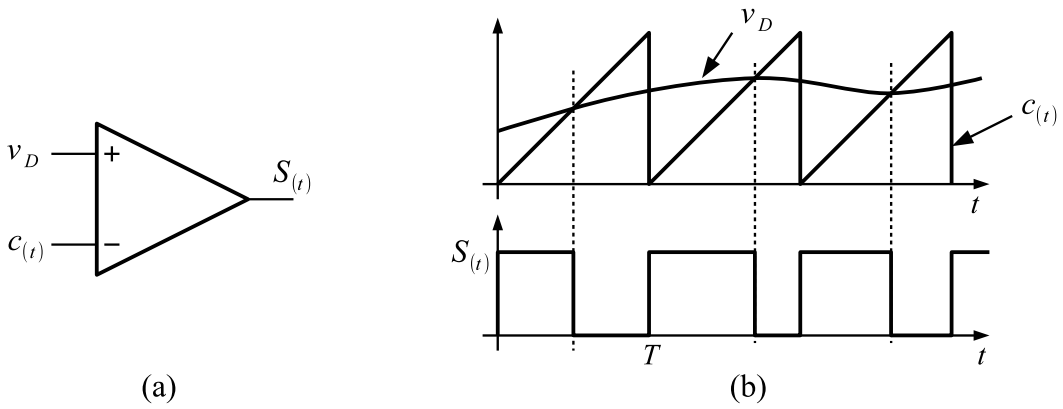

Fig. 16: PWM generation: (a) comparator; (b) waveforms

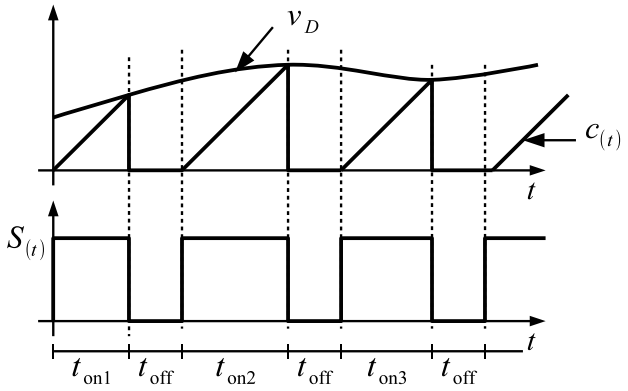

Fig. 17: PWM generation: constant-off-time/variable-on-time PWM

3.2 Variable-frequency PWM

Variable-frequency PWM, although not as popular as constant-frequency PWM, is also used in practice. The common variations of variable-frequency PWM are the constant-off-time/variable-on-time and constant-on-time/variable-off-time versions.

Figure 17 shows the waveform for constant-off-time/variable-on-time PWM using a sawtooth-like carrier signal. The switch is turned on after a fixed time; at this point, the sawtooth signal starts to rise at a constant rate. The switch is turned off again when the sawtooth signal intersects the signal v_D. After the turn-off of the switch, the carrier is reset to zero for a fixed period of time. The figure shows that the on time increases and the switching frequency decreases when the signal v_D is increased, resulting in variable-frequency operation. Constant-on-time/variable-off-time PWM can be implemented in a similar way.

Variable-frequency PWM is used in light-load operation of power converters in order to increase the efficiency of the converter under these conditions. The main disadvantage of this is the difficulty associated with the design of the input and output filters. The filter cut-off frequency has to be selected based on the lowest possible switching frequency in order to provide the required attenuation of ripple and electromagnetic interference (EMI) under all possible operation conditions. This usually leads to a conservative design with significant volume and cost penalties.

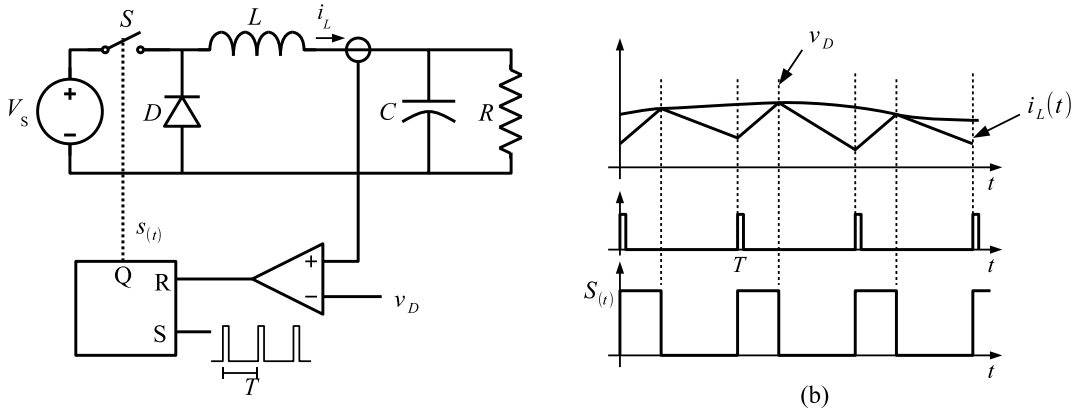

Fig. 18: Current mode: (a) circuit diagram; (b) waveforms

3.3 Current mode control

Current mode control uses direct measurement of the inductor current to generate the switching function. One way of generating the switching function is to replace the sawtooth carrier waveform used to generate the PWM by the inductor current, as shown in Fig. 18(b). The switching function is set to unity by a clock signal of period T. When the inductor current reaches the value of the signal v_D, the switching function is reset. Figure 18(a) shows a simple circuit for current mode PWM generation.

3.3.1 Slope compensation

The peak current mode method is inherently unstable at duty cycles higher than 0.5, resulting in subharmonic oscillations. A compensating ramp (with slope equal to the inductor current down-slope) is usually applied to the comparator input to eliminate this instability.

Note that in current mode control, the output voltage is not directly controlled. An addition loop is needed in order to obtain a regulated output voltage.

3.4 Variable-structure control

Variable-structure control offers an alternative way to implement a switching function, which exploits the inherently variable nature of the structure of DC–DC converters. In practice, the converter switches are driven as a function of the instantaneous values of the voltages and currents. The most important feature of variable-structure control is its ability to provide robust control. Although the study of variable-structure control is far beyond on the scope of this article, hysteresis control provides a very simple and intuitive example. Sliding-mode control is other variable-structure control method for power converters reported in the literature.

3.4.1 Hysteresis control

Hysteresis control is based on comparing the output voltage V_R with a reference voltage v_D using a hysteresis comparator. If the voltage is lower than the upper limit of the comparator, the switch is turned off until the output voltage reaches the lower limit of the hysteresis comparator. When the voltage reaches this limit, the switch is turned on. Figure 19 shows a simple circuit diagram for hysteresis control, and typical waveforms.

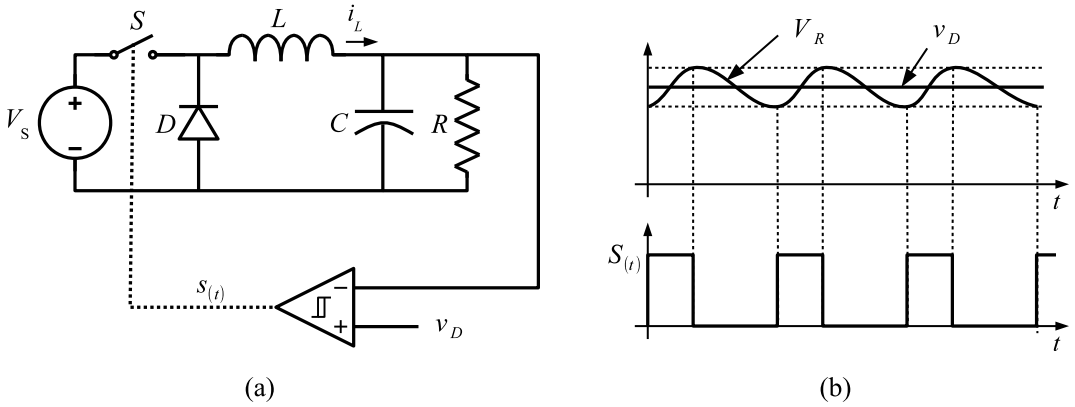

Fig. 19: Hysteresis control: (a) circuit diagram; (b) waveforms

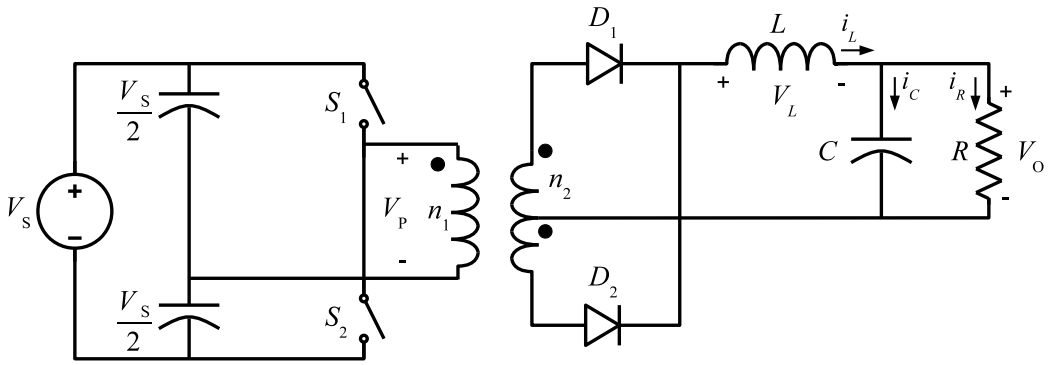

Fig. 20: Half-bridge converter: circuit diagram

4 Derived converter topologies

Several different topologies have been derived from the basic DC–DC converters. In this section, three different groups of converters will be presented. The first group of converter topologies are isolated versions of the basic converters. The use of a transformer provides galvanic isolation between the input and output voltages. An additional advantage of the use of a transformer is an increase in the output voltage range of the converter due to the turns ratio of the transformer. The second group is formed by the flyback converter. This converter has galvanic isolation provided by coupled inductors. The difference between a transformer and coupled inductors is that in the latter case there is no direct energy flow from the input to the output. This fact limits the use of these converters to low-power applications. Finally, a converter with continuous input and output currents is presented.

4.1 Half-bridge converter

The circuit diagram of a half-bridge converter is shown in Fig. 20. The output filter part of the circuit is the same as that in a buck converter. The square waveform of the transformer secondary is rectified and then filtered by the output stage. The voltage at the primary of the transformer is shown in Fig. 21. The voltage per second on the primary and secondary sides during the switching period has to be zero in order to avoid saturation of the transformer.

In this converter, two capacitors act as an input voltage divider, which is connected to one of the inputs of the transformer. A two-polarity voltage is obtained by connecting the other input to V_S or a reference voltage using the switches S_1 and S_2. The switches operate shifted in phase by $T/2$ with

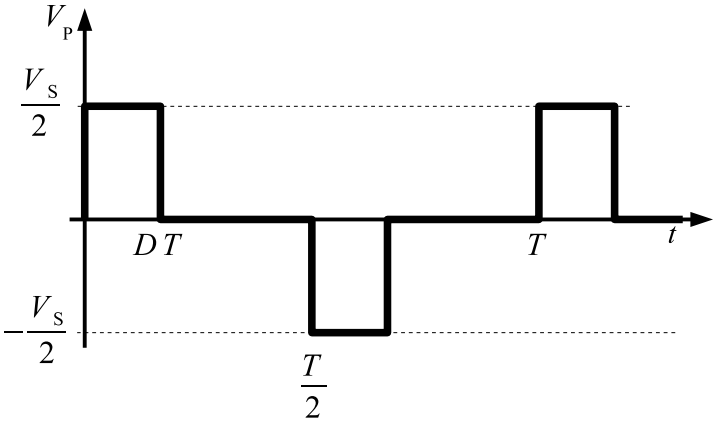

Fig. 21: Half-bridge converter: transformer primary voltage

the same duty ratio D. The duty ratio must be smaller than 0.5. When the switch S_1 is on, the diode D_1 conducts and the diode D_2 is off. The diode states are reversed when the switch S_2 is on. When both controllable switches are off, both diodes are on and share the filter inductor current equally. This short-circuits the transformer and forces the transformer input voltage to zero. The DC voltage transfer function of the half-bridge converter is given by the following equation:

$$M_{\mathrm{V}} \equiv \frac{V_{\mathrm{O}}}{V_{\mathrm{S}}} = 2D\frac{n_2}{n_1}. \tag{22}$$

4.2 Push–pull converter

Push–pull converters, like half-bridge converters, can be regarded as two single-switch buck converters running out of phase. A circuit diagram is shown in Fig. 22. The volts per second are balanced by alternating the operation of the switches S_1 and S_2. Similarly to the half-bridge converter, the output filter stage is the same as that in the buck converter. The main advantage of this topology is that both switches are connected to the reference voltage, which avoids the use of a floating driver for the switches. The main disadvantage is that differences in the period t_{on} of the switches could lead to saturation of the transformer.

The DC voltage transfer function of the push–pull converter is

$$M_{\mathrm{V}} \equiv \frac{V_{\mathrm{O}}}{V_{\mathrm{S}}} = 2D\frac{n_2}{n_1}. \tag{23}$$

4.3 Full-bridge converter

The circuit diagram of a full-bridge converter is shown in Fig. 23. In this topology, the controllable switches are operated in pairs. When S_2 and S_3 are on, a positive voltage V_{S} is applied to the primary side of the transformer. In this condition, the diode D_1 conducts the inductor current. With S_1 and S_4 on, the voltage applied to the transformer is $-V_{\mathrm{S}}$ and the the diode D_2 is on. If all the switches are off, both diodes conduct the output current and the secondary of the transformer is short-circuited.

The steady-state DC voltage transfer function is given by

$$M_{\mathrm{V}} \equiv \frac{V_{\mathrm{O}}}{V_{\mathrm{S}}} = 2D\frac{n_2}{n_1}. \tag{24}$$

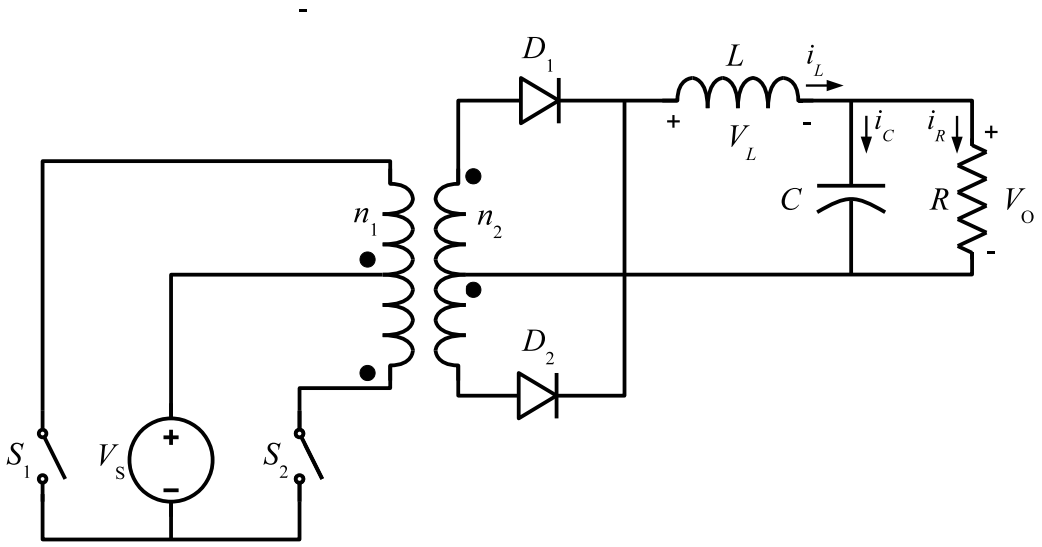

Fig. 22: Push–pull converter: circuit diagram

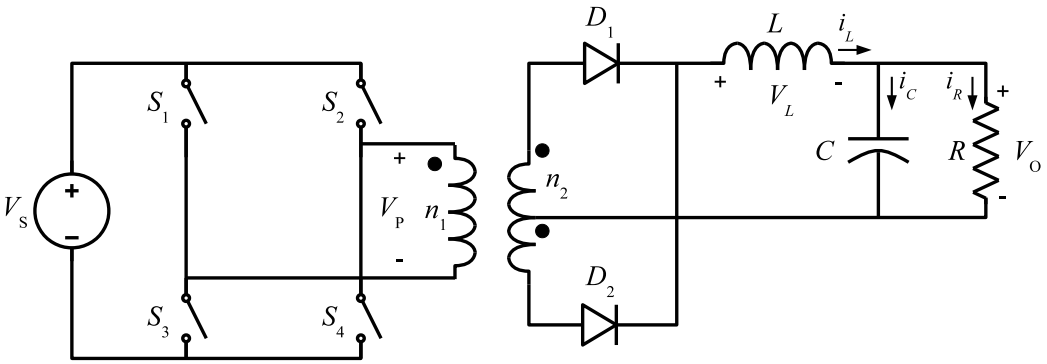

Fig. 23: Full-bridge converter: circuit diagram

4.4 Forward converter

The forward converter is another topology that uses a transformer in order to provide galvanic isolation. The voltage output can be lower or higher than the input voltage depending on the transformer ratio. A circuit diagram is shown in Fig. 24. As in the previous isolated topologies, the output filter stage is identical to that in the buck converter. When the switch S is closed, the diode D_1 conducts and transfers energy from the input to the output stage. During the period when the switch S is open, the diode D_2 carries the current in the inductor L and the diode D_3 connects the third transformer winding to the input voltage to decrease the magnetizing current to zero.

The steady-state DC voltage transfer function is given by

$$M_{\mathrm{V}} \equiv \frac{V_{\mathrm{O}}}{V_{\mathrm{S}}} = 2D\frac{n_2}{n_1}. \tag{25}$$

The condition to avoid saturation of the transformer is

$$n_1 D \leq n_3(1-D). \tag{26}$$

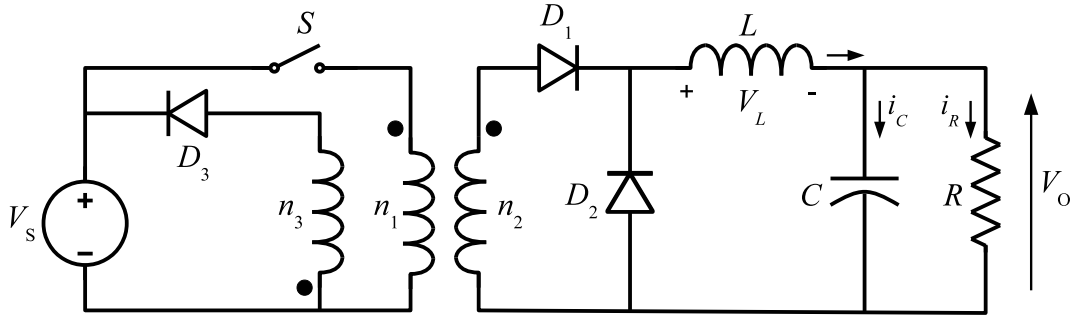

Fig. 24: Forward converter: circuit diagram

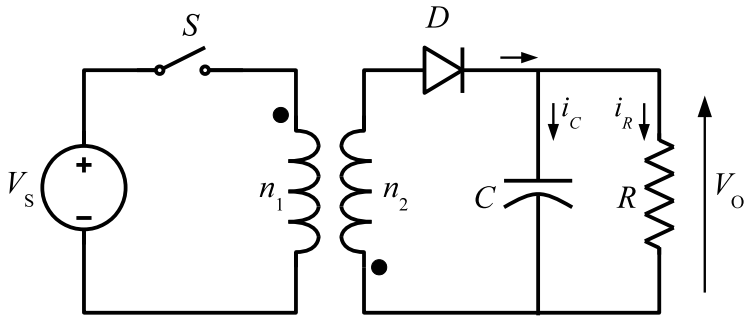

Fig. 25: Flyback converter: circuit diagram

4.5 Flyback converter

The flyback converter is derived from the buck–boost topology. The inductor is split into two coupled inductors. As a result of this, galvanic isolation is achieved and the DC voltage transfer function is multiplied by the turns ratio of the inductors. The basic circuit diagram is shown in Fig. 25.

The magnetic components of the flyback converter act more like two inductors sharing a common magnetic core than as a transformer. Energy is stored in the common magnetic core during the time t_{on} of the switch S and is then transferred to the output stage during the time t_{off}. There is no direct energy transfer between the primary and secondary windings, unlike the converters mentioned above. This limits the application of this converter to low-power applications.

4.6 Ćuk converter

The Ćuk (pronounced 'chook') converter was introduced by Slobodan Ćuk of the California Institute of Technology. The circuit diagram of this converter is shown in Fig. 26. The main advantage of this converter is the continuous currents at the input and output of the converter. The main disadvantage is the high current stress on the switch.

The DC voltage transfer function of the converter is obtained using the average current in the capacitor C_1, which should be zero during a switching period when there is power balance between the input and output of the converter:

$$I_{L_2} DT = I_{L_1}(1-D)T, \tag{27}$$

$$P_{\mathrm{IN}} = V_{\mathrm{S}} I_{L_1} = -V_{\mathrm{O}} I_{L_2} = P_{\mathrm{OUT}}. \tag{28}$$

Using these two equations,

$$M_{\mathrm{V}} \equiv \frac{V_{\mathrm{O}}}{V_{\mathrm{S}}} = \frac{D}{(1-D)}. \tag{29}$$

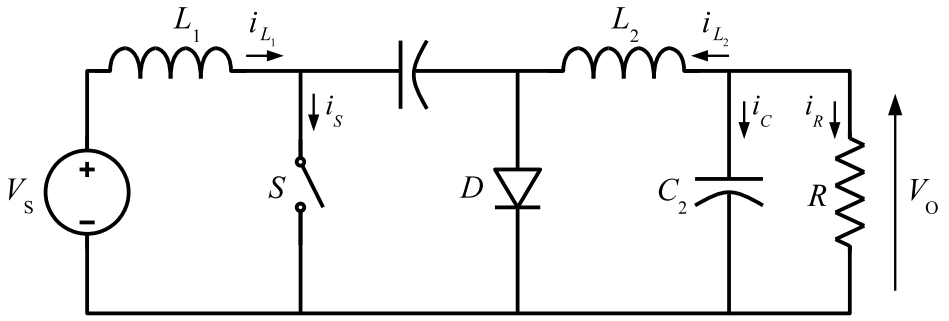

Fig. 26: Ćuk converter: circuit diagram

Isolated versions of the Ćuk converter can be found in the literature. There are also versions of this converter in which the two inductors L_1 and L_2 are integrated into one magnetic element in order to reduce the cost and volume of the converter.

The list of converters presented in this section is not intended to be exhaustive. The converter topologies presented are just a small sample of the many topologies that have been reported in the literature. The right topology for each application depends on many factors, which include the stress on the semiconductors and passive components, the level of power to be transferred, and the switching frequency, among others.

5 Additional topics

This section presents some additional topics related to one-quadrant power converters that are worth mentioning. Firstly, synchronous rectification is addressed as a method to reduce losses, especially in low-voltage power converters. Interleaved converters are discussed as a way to increase the power handled by converters while reducing the stress on the input and output filters. Finally, a brief introduction to hard switching, snubbers, and soft switching is given.

5.1 Synchronous rectification

One component of most one-quadrant converter topologies is a diode. This diode is used to provide a path for the current when the main switch is turned off, or for rectification and providing a DC output. The conduction losses of the diode make an important contribution to the overall power loss of a converter, especially for low-output-voltage, high-output-current power converters.

The conduction loss of a diode in a buck converter is given by the following equation:

$$P_{\mathrm{D}} = V_{\mathrm{F}} I_{\mathrm{O}} (1 - D). \tag{30}$$

The overall efficiency due to the diode conduction loss can be expressed as

$$\nu = \frac{V_{\mathrm{O}} I_{\mathrm{O}}}{V_{\mathrm{O}} I_{\mathrm{O}} + V_{\mathrm{F}} I_{\mathrm{O}} (1 - D)} = \frac{V_{\mathrm{O}}}{V_{\mathrm{O}} + V_{\mathrm{F}} (1 - D)}. \tag{31}$$

For low-voltage power converters, this equation shows that the overall efficiency of the converter can drop to unacceptable levels. One way to increase the overall efficiency under these conditions is to replace the diode by a MOSFET, as shown in Fig. 27. The MOSFET introduces an almost linear resistance with a lower voltage drop. Figure 28 shows the power loss in S_2 for a diode and for a MOSFET.

In addition to minimizing conduction losses, MOSFETs offer the additional benefit that they can easily be paralleled because their $R_{\mathrm{DS_{on}}}$ has a positive temperature coefficient.

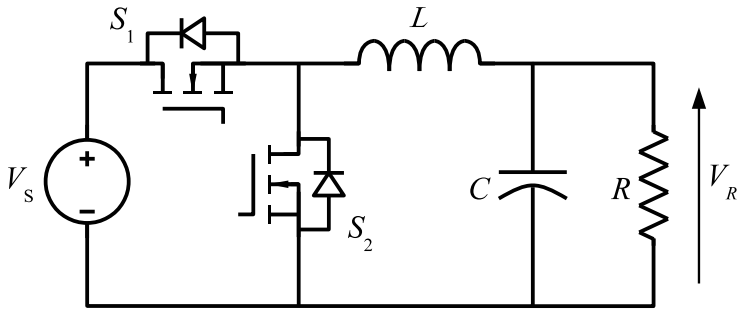

Fig. 27: Synchronous rectification: circuit diagram

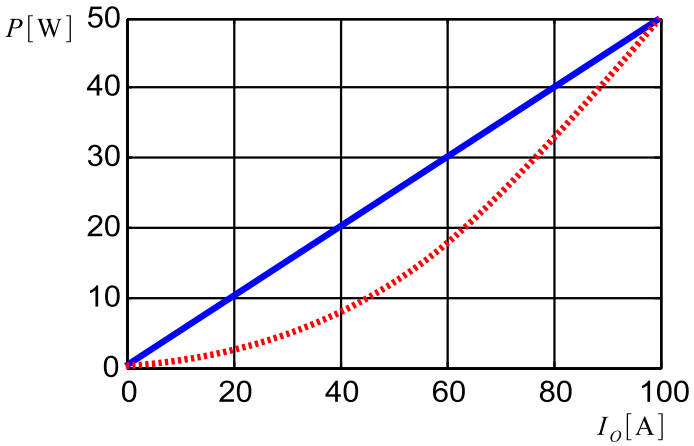

Fig. 28: Power loss in S_2: diode (solid line) and MOSFET (dashed line)

5.2 Interleaved converters

The concept of paralleling several DC–DC power converters in order to increase the output power is well known in power electronics. A further step is to group the components together and control the resulting converter as a unit. Interleaving is one of the techniques most often used, and provides several advantages such as an increase in the resulting switching frequency and a reduction in the component size. Figure 29 shows the circuit diagram of an interleaved buck converter. The switching functions for the switches $S_1, S_2, \ldots, S_N$ have the same switching frequency but there is a phase shift between them equal to $2\pi/N$, where N is the number of individual stages that form the converter.

The first plot in Fig. 30 shows the output currents of the individual stages and the overall output current formed by addition of the inductor currents for each phase. The ripple frequency of the overall output current is N times the frequency of the inductor phase currents. This multiplication of the ripple frequency reduces the requirements on the output filter. Figure 31 shows the normalized output ripple current. This shows how the ripple is reduced; for particular values of D, the ripple current is zero.

A similar effect is produced in the input current. The requirements on the input capacitor are also reduced by the interleaving of the converters. Figure 30(b) shows the input current for each branch and the total input current. An increase in the frequency and a reduction in the RMS value can be observed. Figure 32 shows the normalized input capacitor RMS current for different values of N.

5.3 Hard switching, snubbers, and soft switching

One of the big advantages of operating a power converter in switched mode is that voltages across and currents through the switches are not present simultaneously during the ‘on’ and ‘off’ states. This cannot

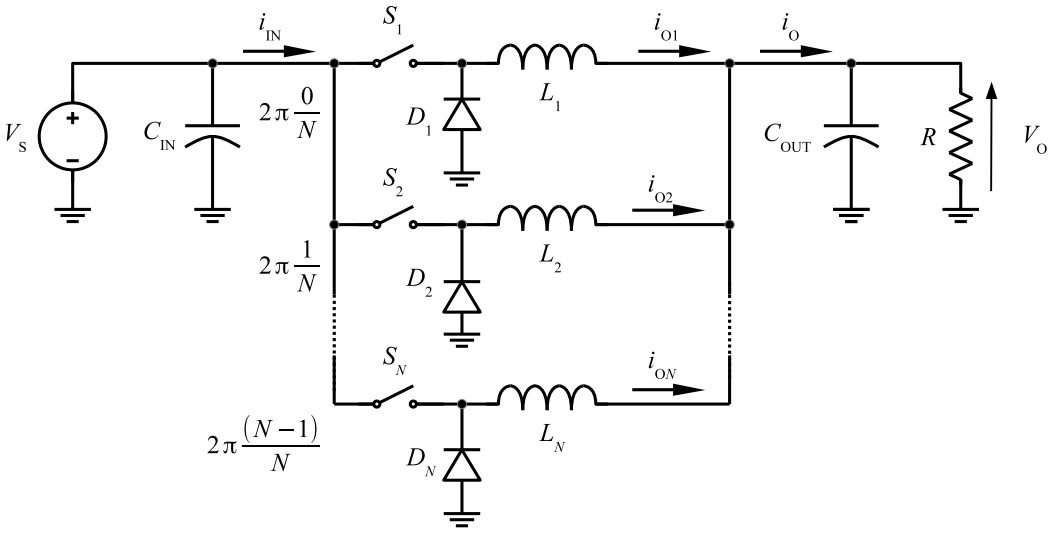

Fig. 29: Interleaved buck converter

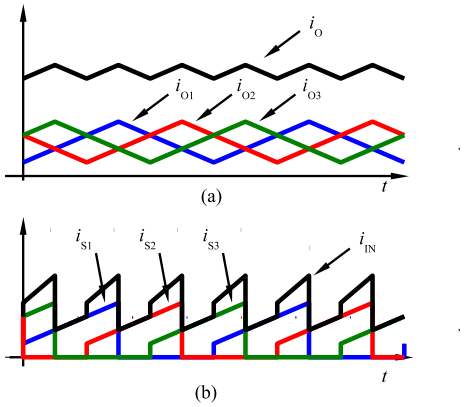

Fig. 30: Output and input currents for a three-stage interleaved buck converter

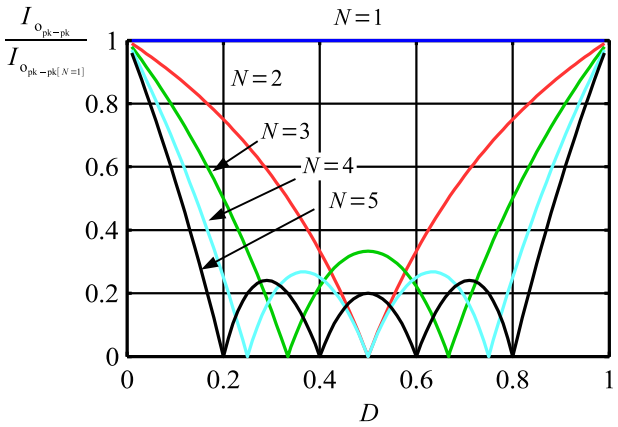

Fig. 31: Normalized output ripple current

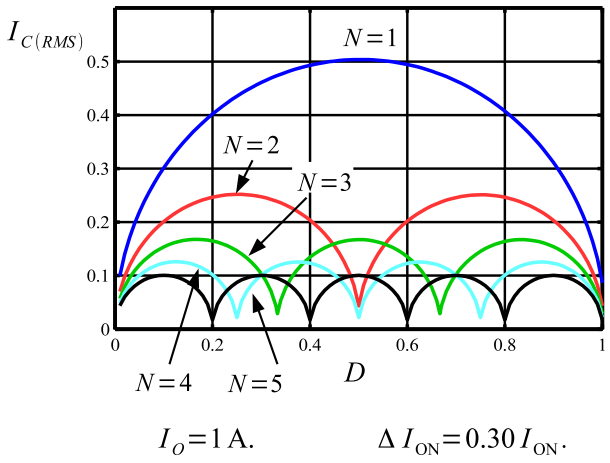

Fig. 32: Normalized input capacitor RMS current

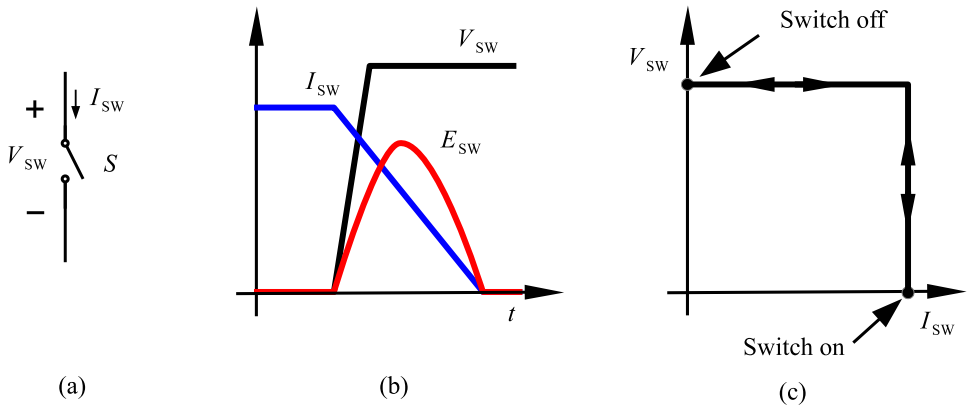

Fig. 33: Hard switching: (a) single switch without snubber; (b) switch voltage and current during transition; (c) transition diagram.

be true, however, during the transitions between the states of the converter. The trajectories during the transitions determine whether the switches operate in a hard or soft switching mode. The switching trajectory of a hard-switched power device is shown in Fig. 33. During the turn-on and turn-off processes, the power device has to withstand high voltages and currents simultaneously, resulting in high switching losses and stress.

The switching losses are proportional to the operating frequency of the converter and are usually the main factor that limits the operating frequency. Another disadvantage of hard-switching operation is an increase in high-frequency emissions, which produce EMI.

Dissipative passive snubbers are usually added to power circuits in order to reduce the $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ of the power devices, and the switching losses and stresses can be diverted to these passive snubber circuits. Figure 34 shows how the transition trajectory is modified by the presence of an RC snubber. The $\mathrm{d}v/\mathrm{d}t$ of the switch is reduced during the turn-off and part of the transition energy is transferred to the dissipative element of the snubber.

The snubber design has to be done carefully in order to correctly dimension the components and ensure proper operation. More complex snubber circuits have the ability to recover the transition energy and increase the overall efficiency of the converter.

A further step can be taken to reduce the commutation losses by operating the switches in a soft switching mode. The basic idea of soft switching can be explained using the plots in Fig. 35. The voltage

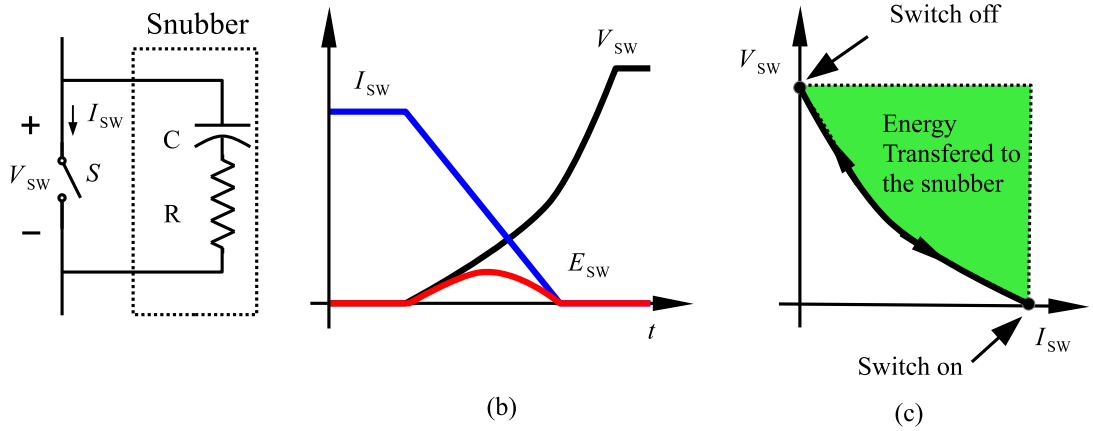

Fig. 34: Snubbers: (a) circuit diagram of RC snubber; (b) switch voltage and current during transition; (c) transition diagram.

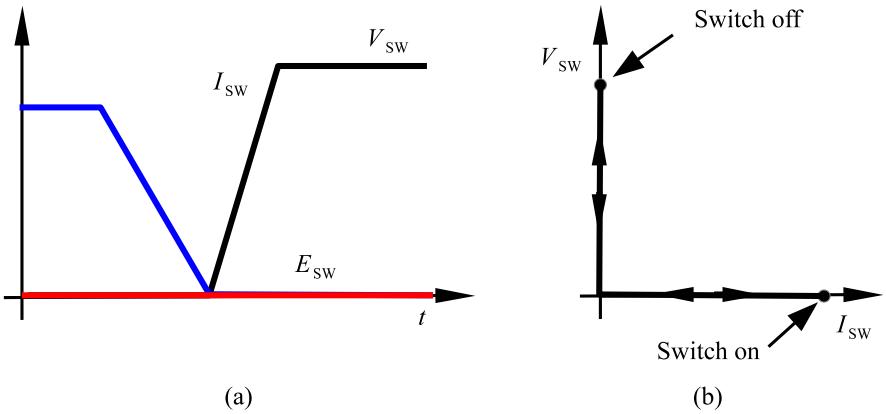

Fig. 35: Soft switching: (a) switch voltage and current during transition; (b) transition diagram

across the switch is forced to be zero while the current is dropping. When the current is zero, the switch voltage starts to rise until the switch reaches the turn-off state. The losses during the transition are zero.

A simple circuit operating in a soft switching mode is shown in Fig. 36. The switch M_1 opens with zero voltage across its terminals because this voltage is maintained by the capacitor C_1. The voltage v_{A} drops because the inductor current charges and discharges the capacitors C_1 and C_2. Once the voltage reaches zero, the diode D_2 starts to carry current and keeps the voltage close to zero. During the period of time that the diode is conducting, the switch M_2 is turned on. The positive transition of voltage v_{A} is produced in a similar way.

6 DC–DC resonant converters

The trend in power electronics is towards an increase in efficiency, power, and component density. For this reason, resonant converters have received special interest in recent years. These converters have the potential to operate at higher frequencies and with lower switching losses than hard-switching converters. The design of resonant converters and their control presents challenges different from those for other converters. In particular, the control of these converters is usually done by frequency modulation instead of pulse width modulation. Although a comprehensive analysis of DC resonant converters is far beyond the scope of this article, a brief description of their functional principles is given here.

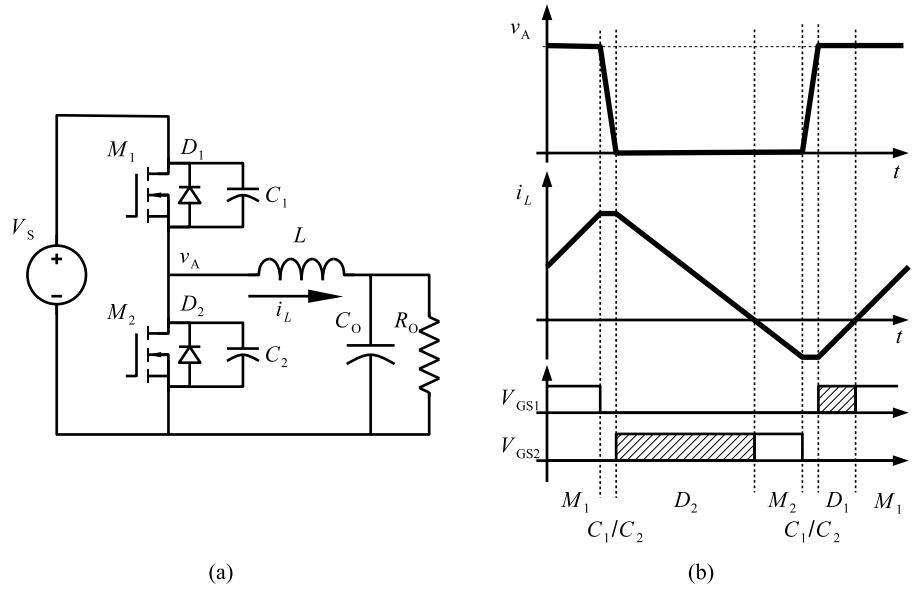

Fig. 36: Soft switching: (a) circuit diagram; (b) waveforms

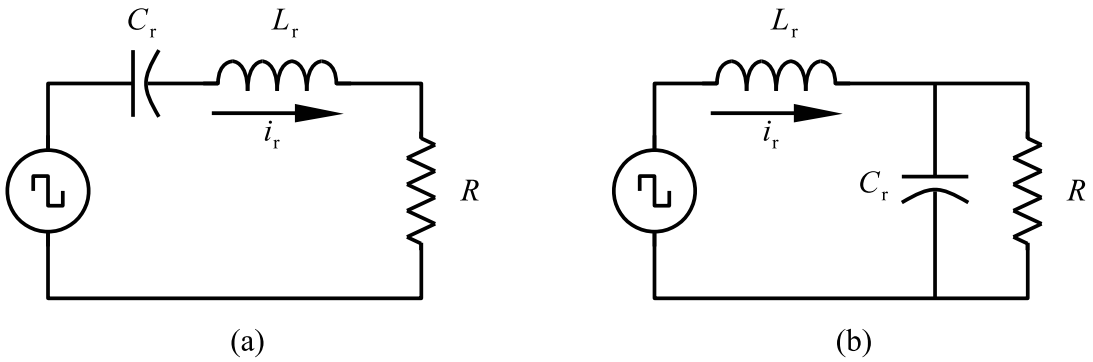

Fig. 37: (a) Series resonant converter; (b) parallel resonant converter

All of the resonant-converter topologies operate in essentially the same way. The power switches generate a square wave voltage or current, which is applied to a resonant circuit. Energy circulates in the resonant circuit, and part of this energy is transferred to the output.

The two basic types of resonant converter are the series resonant converter, shown in Fig. 37(a), and the parallel resonant converter, shown in Fig. 37(b). In both topologies, the energy transferred to the output is regulated by changing the frequency of the driving voltage. The resonant circuit forms a voltage divider with the resistor R. By changing the frequency, the impedance of the resonant circuit and therefore the output voltage can be varied.

The circuits shown in Fig. 37 have limitations. The series resonant converter cannot work under very light load conditions, because the operating frequency would have to be very high in order to regulate the output voltage. The parallel resonant converter requires large amounts of circulating current when operating under heavy load conditions.

6.1 LCC and LLC resonant converters

To overcome the limitations of the resonant converters shown in Fig. 37, converters combining series and parallel topologies have been proposed. Figure 38(a) shows a topology which includes two capacitors

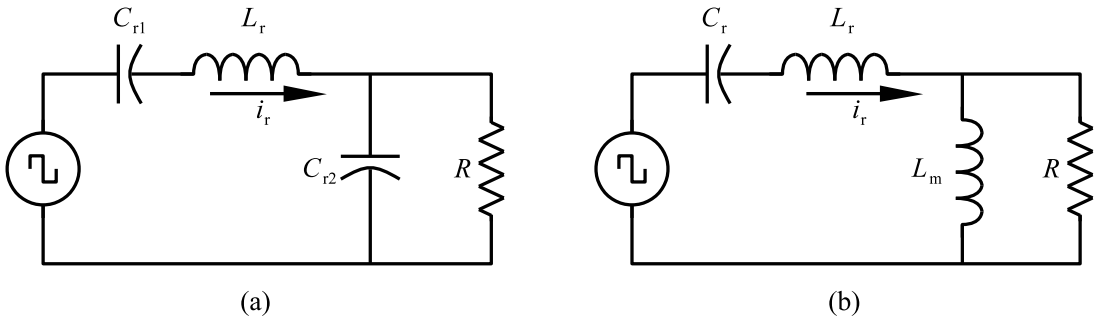

Fig. 38: (a) LCC resonant converter; (b) LLC resonant converter

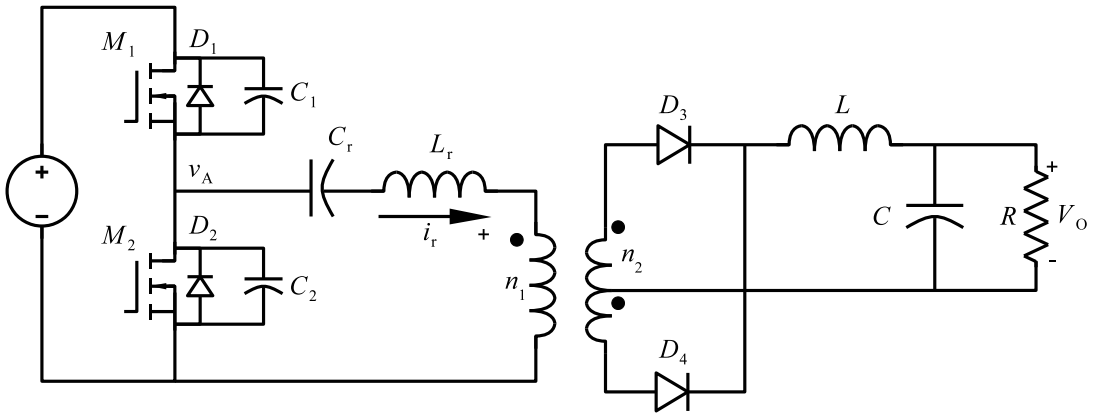

Fig. 39: LLC resonant converter: circuit diagram

and one inductor. This topology is named the LCC resonant converter.

The topology formed by two inductors and one capacitor (the LLC resonant converter) is shown in Fig. 38(b). This topology has several advantages over the LCC topology. For instance, the two inductors can be integrated into one physical magnetic component, and it also provides galvanic isolation.

A simplified circuit diagram of an LLC resonant converter is shown in Fig. 39. The two inductors are the magnetizing and leakage inductances of a transformer. The LLC topology has the additional advantage of being able to operate in a soft switching mode. This allows the switching frequency and power density of the converter to be increased.

The typical waveforms for an LLC resonant converter are shown in Fig. 40. Soft commutation is achieved in a similar way to that described in Fig. 36.

7 Conclusions

One-quadrant power converters play an important role in industrial and consumer electronics applications. Almost every electronic circuit is supplied with a DC voltage provided by some kind of power converter. If a regulated voltage is needed, this converter usually consists of a rectifier stage followed by a regulated DC–DC power converter. The field of power converters for particle accelerators is no exception to this trend. As was mentioned in the introduction, one-quadrant power converters are used to generate the high-precision, stable currents needed for storage ring accelerator magnets. The topologies used in this application depend on the power level required.

This article was intended to be an introduction to this broad subject. All the topics discussed here are covered in depth in books on power converters and in journal and conference papers. The references provided at the end of this article should be a good starting point for further studies.

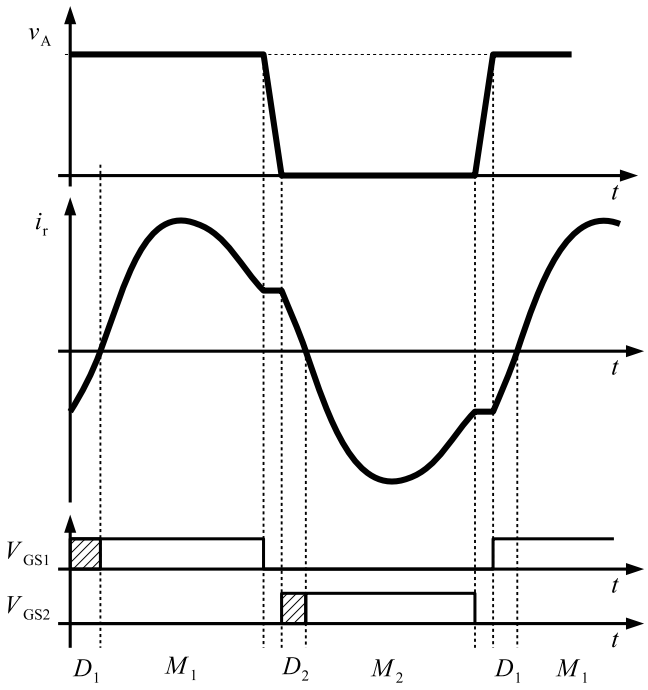

Fig. 40: Waveforms for LLC resonant converter

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Switched Mode Four-Quadrant Power Converters

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Abstract
This paper was originally presented at CAS-2004, and was slightly modified for CAS-2014. It presents a review of the key parameters that impact the design choices for a true four-quadrant power converter, in the range 1–10 kW, mainly based on switching mode converter topology. This paper will first describe the state-of-the-art for this power converter family, giving the drawbacks and advantages of different possible solutions. It will also present practical results obtained from the CERN-designed converter. It will finally give some important tips regarding critical phases like test one, when conducting a project dealing with this type of power converter.

Keywords
Four-quadrant; converter; topology; switch-mode; magnet, energy.

1 Introduction

The design of a four-quadrant power converter design is strongly dependent on its use, and several criteria are reviewed in the first part of this document. A review is then made of some commonly used topologies. The second part of this document gives the key points of the design for a specific four-quadrant power converter designed for powering superconductive magnets in the LHC machine.

In this paper the load will always be assumed to be a magnet, with resistance and inductance, which is a realistic four-quadrant power load. Since the system studied is highly non-linear and some topologies are quite complex to simulate (with up to three control loops working at the same time), the author gives a lot of illustrated key points instead of formulas. This approach is easier to follow as known problems are solved during the design phase. This paper mainly focuses on low or medium output voltages in the range −200 V to 200 V. For a high voltage converter, a different approach would normally be required, since the available components (semiconductor or passive) will have a big impact on the final design choice.

2 Definitions and description of different quadrant operation

The definition and the numeration of operating quadrants are shown in Fig. 1. The naming of each *generator* and *receptor* quadrant has been done according to the energy being managed by the converter placed between the energy source (mains) and the load. Energy can be taken from the mains and delivered to the load, the converter voltage and current being of the same sense, with the converter being seen to *generate* energy from the load's point of view. In the case where the voltage and current are opposite, energy comes back from the load, being 'received' by the converter managing it, in *receptor* mode.

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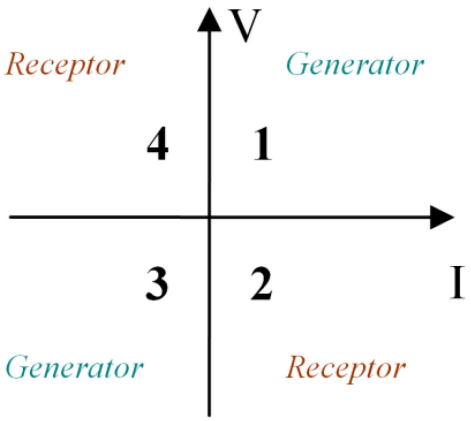


Fig. 1: Typical one-quadrant converter naming conventions

Some simplified graphs are presented to summarize the different type of power converter, applied to a typical four-quadrant power load, with a resistance in series with an inductance (R-L). Through this load example, the limitations of different topologies can be illustrated.

Figure 2 shows a possible curve for a one-quadrant converter, where the current can be controlled while it is increasing. The control of a decreasing current is still possible, but drastic conditions and limitations must be taken into consideration at the level of the power system definition; and also at the level of the current controller. If a negative ramp applied to the current is faster than the load's natural constant time, control will be lost. Also, a commercial one-quadrant converter can sometimes exhibit high output capacitance (for example in the case of a laboratory power supply), with a non-symmetrical rate of voltage change across the capacitor related to the load's operating conditions, i.e. mainly its level of current.

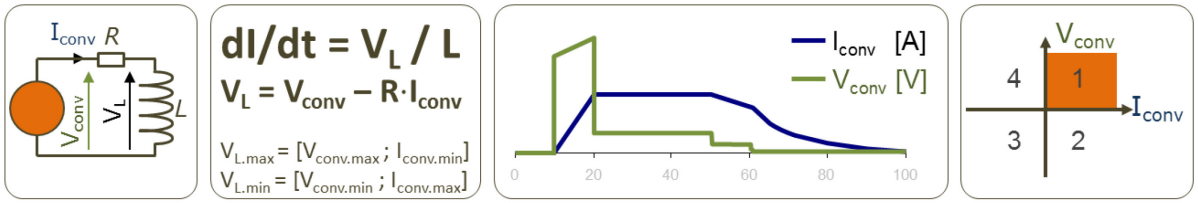


Fig. 2: One-quadrant converter typical curves

Figure 3 shows a possible curve for a two-quadrant converter, where the current can be controlled as long as it stays positive-only (or negative only). While the current decreases, and depending on its required ramp rate, the converter can be required to absorb energy from the load. In such a case, load energy will be 'removed' from it, being dissipated in cable resistance, but also 'managed' by the converter if its extraction is required to be faster than the rate allowed by the resistance. The converter can or dissipate, store, or send back the received energy to the original energy source (the mains). It should be understood that the converter must control the level of energy flowing from the energy source, through the converter, to the load inductance, or back from the inductance, in a fully controlled way.

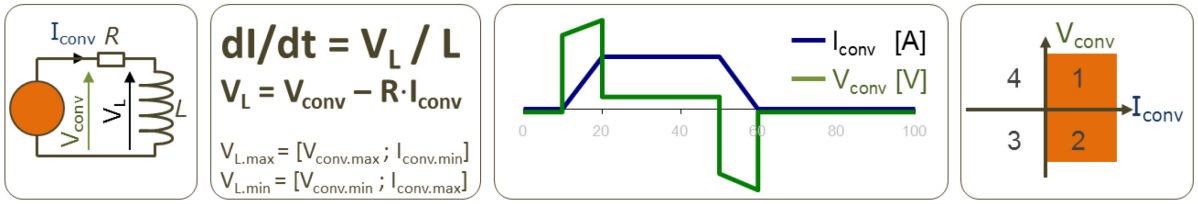


Fig. 3: Two-quadrant converter typical curves

There should be no confusion with some converters being operating in two diagonal quadrants, for example quadrants one and three, by the addition of a polarity switch (mechanical or electronic inverter); the converter, often a one-quadrant converter, will be able to deliver positive and negative current to the load, but will not be able to recover any energy from the load. Despite the load current being positive or negative, this kind of converter will suffer from exactly the same limitations as a one-quadrant converter, regarding the possible current ramp and controllability.

Figure 4 shows a possible curve for a four-quadrant converter, where the current can be controlled without any limitations, regarding to its sense, or evolution (positive or negative ramp). Like a two-quadrant-power converter, the converter can be required to absorb energy from the load. If some topologies are intrinsically providing full and true four-quadrant operation capability like an H-bridge, the management of energy and the directionality of the output current can often lead to relatively complex designs.

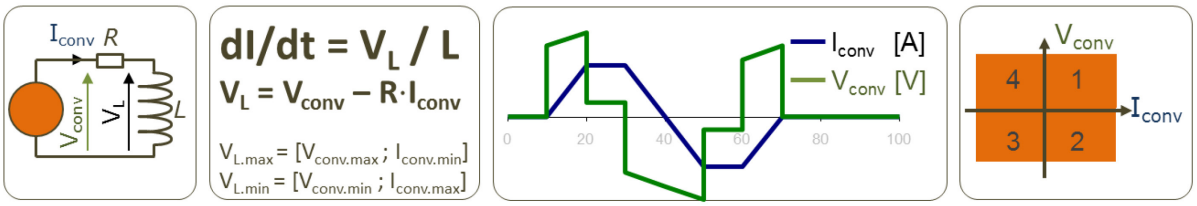


Fig. 4: Four-quadrant converter typical curves

2.1 Receptor mode solutions, a brief review

In the receiving quadrants (quadrants two and four), the converter has to extract energy from the load, either dissipating it, storing it, or sending it back to the mains. It should be remembered that a true four-quadrant power converter should regulate its output conditions while 'absorbing' energy, not being limited in its controllability and performance due to the quadrants in which it operates.

2.1.1 *Locally storing the load energy*

This function is often performed using capacitors, which are in charge of collecting load energy; these capacitors can be a naturally part of the topology chosen (full-bridge DC–DC topology), and dimensioned to take into account this secondary function (storage capacity). This storage capability can be dedicated either on the primary or secondary sides; this choice is made depending on the voltage used at the output, and also taking into consideration the complexity of the final design.

Even if some designs already include the local storage of energy, supercapacitors or superconducting inductors can present an attractive alternative in the case of demanding energy management, pushing this topology ahead. Of course, a variety of possible 'mechanical' storage solutions also exists, like kinetic energy storage, which relies on a rotating machine being coupled to the existing topology; these solutions, which are out of the scope of four-quadrant switching converters, are not treated in this paper.

2.1.2 *Sending the load energy back to the mains*

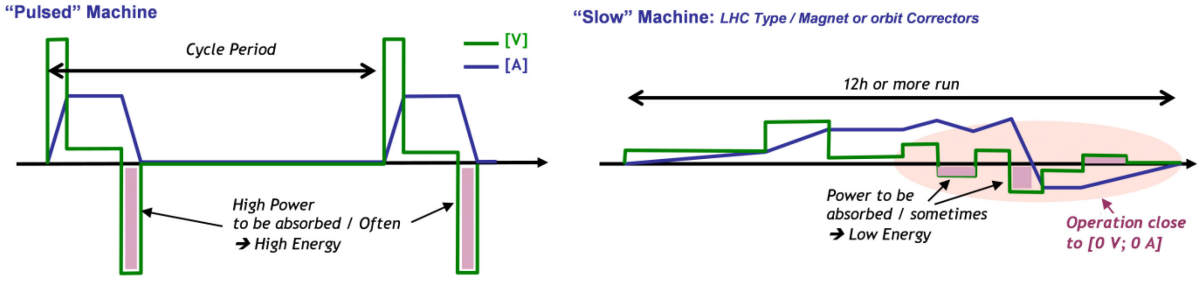
This field is dominated by thyristor-based topologies (two thyristor converters operating back-to-back), and is still extensively used when high power is required. Simplicity of design and robustness of this well-known topology are other big advantages. The price to be paid is certainly the limited bandwidth to be expected from network based on natural low frequency Also, some high frequency switching power converter designs have been presented as a valid alternative, with a working prototype validated at CERN, with relatively complex control requirements [2].

2.1.3 *Dissipating the load energy*

This is surely the least appealing solution, especially when semiconductors are used to dissipate energy as pure heat losses. Nevertheless, this alternative solution can be integrated into modern topologies, and still presents good performance in the fields of electromagnetic compatibility (EMC) and very high bandwidth performance. This approach can be justified when performance is judged to be the most important consideration, with the frequency of charge/discharge that the load will require determining viability at a power management level.

2.2 Influence of load cycle on converter topology

Different types of accelerators use different types of magnet for different purposes. It could be drastically summarized in two main different domains: pulsed or slow, as represented in Fig. 5. When a pulsed machine is designed the energy-saving aspects should be taken into account. With high frequency charge and discharge sequences, a true four-quadrant converter, giving back energy to the mains, or locally storing it for the next run, should be envisaged. In the other hand, a slow and ultra-high precision machine (like the LHC) will focus on different criteria like stable controllability versus operating point and the low-level conducted noise environment (EMC), which are both crucial criteria for high precision operation.



(a) (b)

Fig. 5: Machine type operation typical cycles. (a) Pulsed machine; (b) 'slow' machine

2.3 Load influence on design parameters

The LHC requires a very high magnetic field to control the beam; this field, being directly proportional to the current, can require up to 600 A load current in some four-quadrant converter families. The number of correctors, combined with these levels of current, made the superconductor magnet a valid choice for energy-saving considerations. These magnets are by definition lossless loads, since magnet is a pure inductance, up to some Henrys. To avoid adding extra losses in the tunnel, where converters are installed close to their loads, large cross-section copper cables were connected to these magnets, connecting the power converter to its load. All of these boundary conditions lead to a very high time constant circuit (large inductance value combined with very low resistance value), keeping in mind that:

$$\tau_{CIRCUIT} = \frac{L_{MAGNET}}{R_{CABLE}}, \tag{1}$$

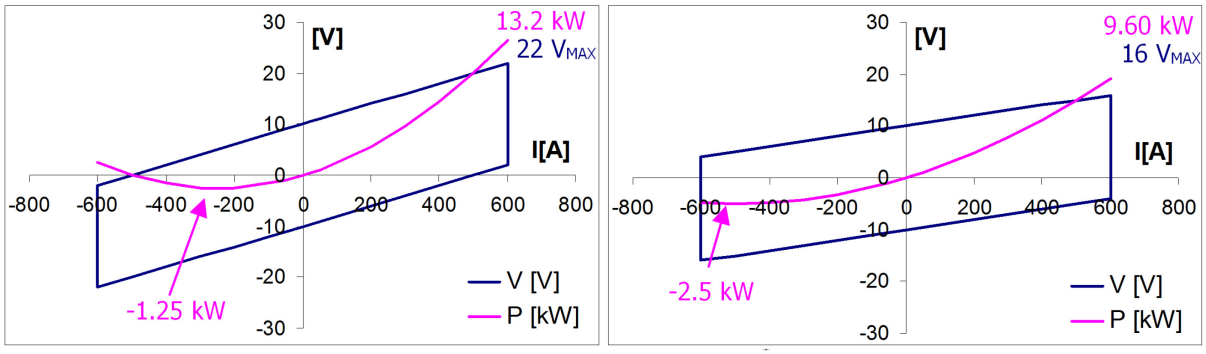
where L_{MAGNET} is the magnet inductance value [H] and R_{CABLE} is the cable resistance value [Ω].

The value of this time constant, inherent from the circuit type and physical characteristics, combined with the LHC's required characteristics giving the range of the current, determines the type of power converters to be used with specific operating areas,

$$P(I) = U(I) \cdot I = R_{\mathrm{CABLE}} \cdot I^2 + L_{\mathrm{MAGNET}} \cdot \frac{\mathrm{d}(I)}{\mathrm{d}t} \cdot I\,. \tag{2}$$

It can be stated that a trade-off could be found, given an operating range (I_{MAX} and dI/dt) for a dedicated magnet (L_{MAGNET} fixed) between generating peak power and regenerating absorbed peak power, modulating the cable resistance. Of course, if increasing cable resistance mechanically increases the losses, it will nevertheless decrease power absorbed by the power converter. Increasing regenerating power for a four-quadrant converter can be a lot more difficult than simply slightly increasing its generating power, saving a lot on the regenerating power level.

Figure 6 shows the typical case of a given superconducting magnet used with two different resistances given by the cable, 10 mΩ and, doubling the cable resistance, 20 mΩ.



(a) (b)

Fig. 6: Influence of circuit parameters on converter operation. (a) 20 mΩ; (b) 10 mΩ

In the 20 mΩ case described above (Fig. 6(a)), the power to be generated is 1.4 times higher when the level of power to be absorbed is up to two times lower, and at a lower operating current. Of course, cable losses are two times higher during all magnet operations. Nevertheless, this consideration could be really interesting in the case of a corrector magnet, which is not often used at full current (less heat losses), lowering the power converter design constraints.

3 Main topologies for the four-quadrant stage

A four-quadrant stage is the dedicated part of a power converter used to manage load voltage and current in the four-quadrant area. This function can be part of the converter topology (thyristor-based or H-bridge DC–DC topologies) or as a kind of extension to a standard one-quadrant power converter. This section deals with classical solutions, which are mainly used in the four-quadrant power converter domain.

3.1 Two thyristor bridges mounted in anti-parallel

This standard solution makes it possible to send back energy to the mains. It is based on two thyristor bridges, mounted in anti-parallel using the natural two-quadrant capability of each bridge. In this case, the four-quadrant stage is represented by the whole thyristor converter for half of the quadrant plane. This solution is very well known and can handle high power constraints. If noted here as a reminder, this topology will not be described in detail since it is not usually part of the switched mode converter family.

3.2 Linear dissipative stage

3.2.1 *Description*

A linear dissipative stage relies on a push–pull stage, with transistors used as ‘programmable resistors’ dissipating energy in their receiving modes. This stage is usually an additional stage for a standard generator power converter that is used to provide power at the input of the linear stage.

An alternative solution exists with polarity switches added to transform a single output to the required double outputs. This solution, see Fig. 7, is much easier considering the power converter to be designed, since it has a single output, but it leads to potential distortions that are seen when the polarity switches act. It also requires the control of additional transistors, while the standard double output voltage source can use simple additional rectifiers (an L-C filter can be shared between the two outputs, reducing the number of additional components and cost).

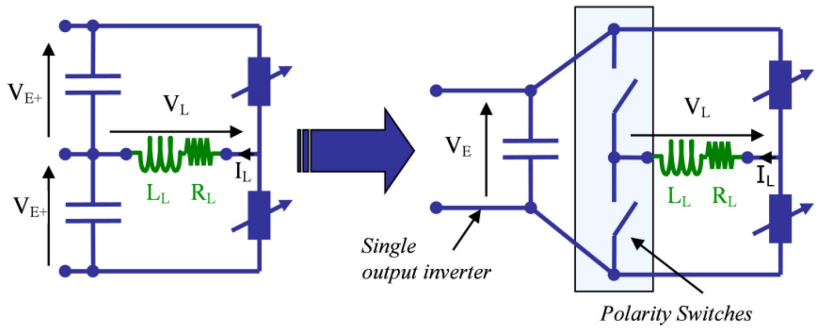


Fig. 7: Linear stage schematic

3.2.2 *Operation principle*

A dual output power source is used to power the linear stage, with the usual limitation of the two dual outputs being tied together. (Standard solutions are usually based on a dual output power converter using one inverter stage powering a dual output transformer.) Two different situations are possible, with a fixed value or variable dual output configuration.

3.2.3 *DC fixed dual output configuration*

Figure 8 shows voltage and current waveforms for a typical magnet application, highlighting the limitations and dissipation problems to be dealt with. In the particular example below, a [±10 V; ±120 A] converter is shown. Since losses in transistors are assumed to be 2 V at the highest level of current, a minimum dual voltage of 12 V is required to feed the output linear stage.

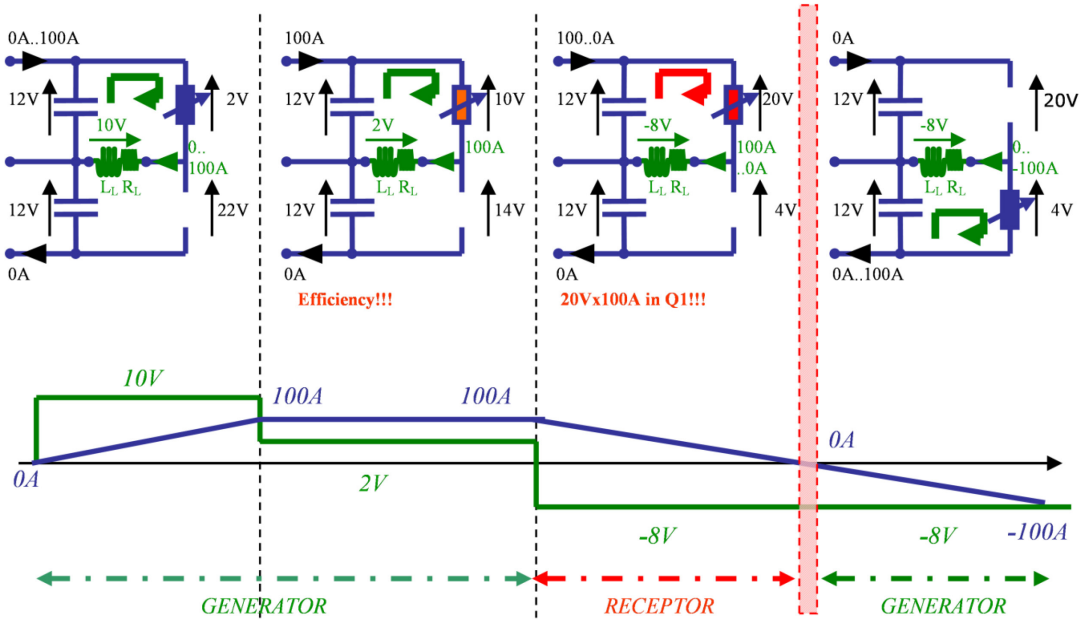


Fig. 8: Four-quadrant linear stage (fixed DC dual voltage)

A dual output 50 Hz transformer, with adequate rectifying and filtering series stage, can simply provide the two desired fixed DC sources, represented on the schematic by capacitor; modern design would potentially propose a switched-mode power supply for size reduction, for example. Both voltage sources have to provide a voltage capable of compensating the losses given by the voltage drop across the active switch at maximum current.

If this solution is very simple, an efficiency issue exists with loss management at the transistor level, especially in low voltage/high current conditions where the transistor has to dissipate a large proportion of the energy given by the power source. This is particularly true in superconducting magnet powering, since a high voltage is necessary to ramp the current to its maximum losses, when a steady state requires a very low voltage induced by the DC cable losses. A second source of losses is the regenerating phase, when an active transistor has to handle double the level of power that is normally required by the load.

An example of an old-fashioned system made of several transistors in parallel is shown in Fig. 9. If the system can be very fast (no topological power-side limitation except the transistor's inherent speed), dissipation is a hot issue, as well as the potential for a cascading failure, which can result from an initial failure leading to the destruction of several transistors at the same time.

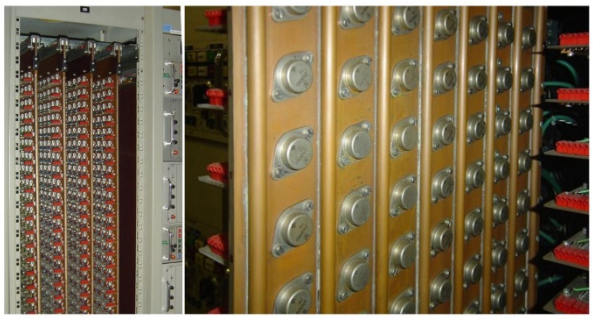


Fig. 9: Water-cooling linear stage of a CERN four-quadrant converter

3.2.4 *Variable DC dual output configuration*

The solution proposed in Fig. 10 is a lot better concerning the level of efficiency; generating power provided from the mains follows the requested load, in addition to the active transistor conduction losses.

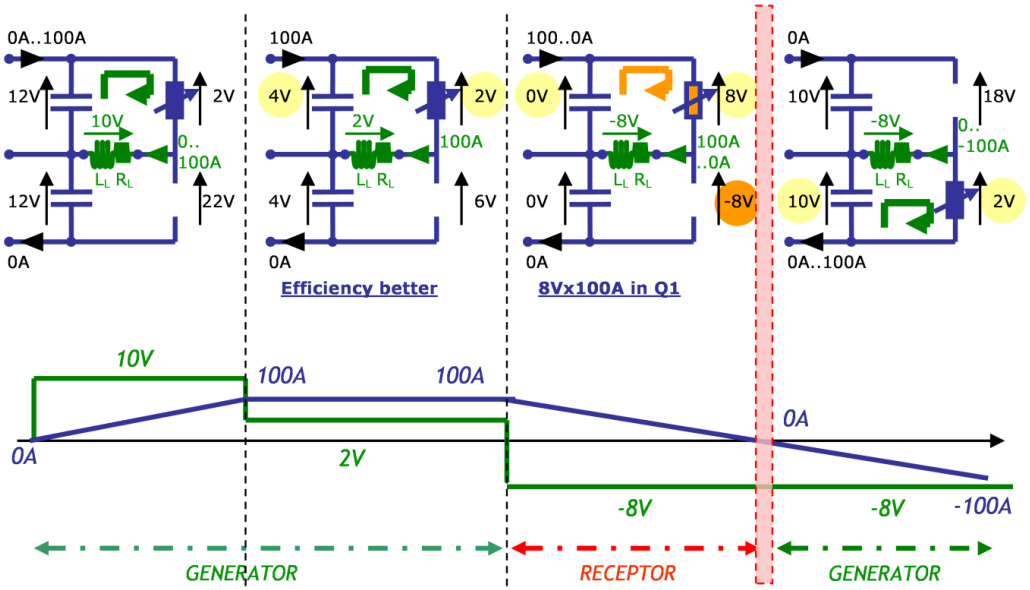


Fig. 10: Four-quadrant linear stage (variable DC dual voltage)

On the two schematics proposed, the 0 A zone is always considered to be a critical zone, since the linear stage always 'relies' on the current going through the relevant transistor following the voltage reference. This state is particularly critical when the 0 A point has to be crossed, while voltage has to be present on an inductive load. This is clearly impossible as shown in Fig. 10, and needs some artificial circuitry.

The voltage level across the transistor while the converter is operating in generator mode (2 V above) needs deep analysis. Indeed, it will be demonstrated below that it is possible to benefit from using an unsaturated linear stage, for giving extra rejection of mains perturbation. This option has obviously an efficiency cost since conducting active transistor losses will be higher.

3.3 Switching stage

3.3.1 *Description*

A conventional H-bridge stage (with an L-C filter in series to filter the switching ripple at the output level) can deal with energy sent to or received from the load. Energy has to be managed at the input of the H-bridge level, stored in the capacitor, or discharged by an additional brake chopper (switching transistors in series with a resistor, in charge of limiting the overvoltage condition across the input capacitor).

3.3.2 *Operation principle*

The H-bridge, see Fig. 11, is a natural four-quadrant power stage, which makes a good candidate for a four-quadrant power converter, combined with a single voltage power source, providing voltage adaption and insulation from the mains. This power source can be either a 50 Hz transformer or a modern switched-mode-based solution. This topology is very simple to control, since the duty cycle alone directly controls the output voltage, without any transition mode problem.

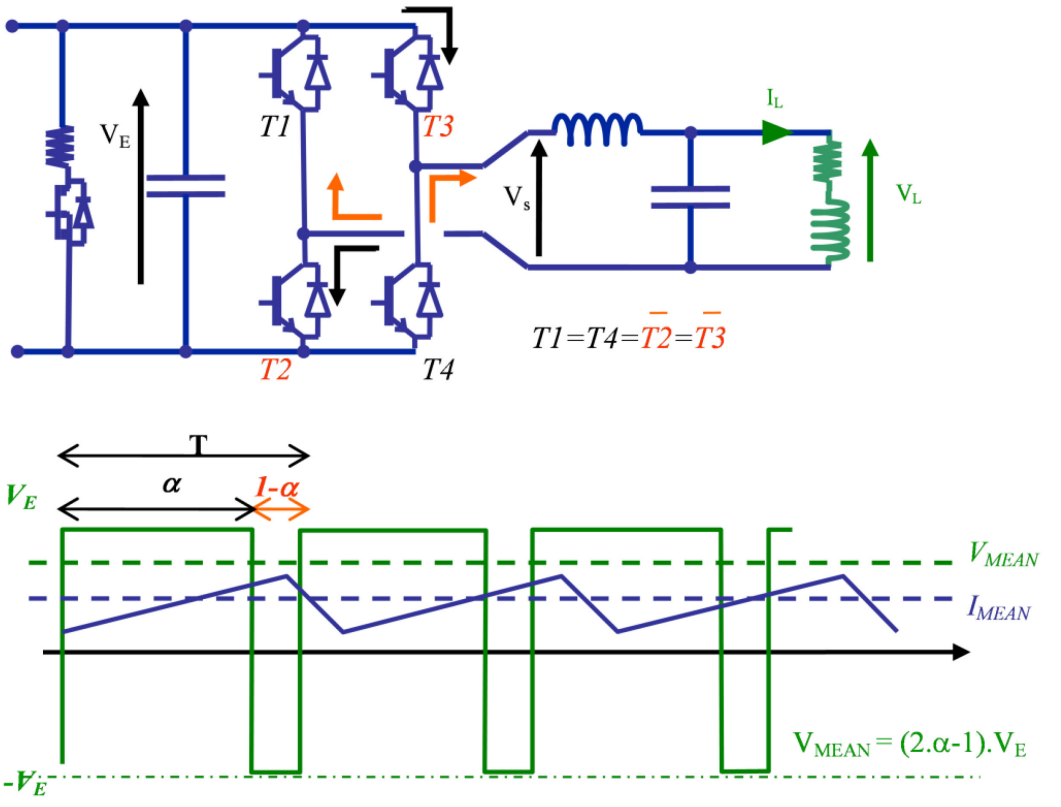


Fig. 11: Four-quadrant switching stage

This topology is often used, since it is highly flexible in terms of power, but it is also flexible in terms of voltage and current operating range. Concerns come from the losses due to the hard switching stage dealing directly with output current, and EMC at the output level resulting from the proximity with the switching cells. It must be taken into account that, once the load is grounded, the H-bridge capacitor, with the source it relies on, will be naturally excited at the switching frequency rate, with severe common mode noise issues to be solved at the output level.

In some advanced cases, converters can use a two-operation mode control, transforming the H-bridge into a classical buck converter, to reduce losses and current ripple (a leg is inactive when a switch is closed).

4 Review of different topologies

Figure 12 gives an overview of the possible combination of stages required to build a four-quadrant power converter. All 'rectifier bridge' paths indicate a topology where energy cannot be returned to the mains.

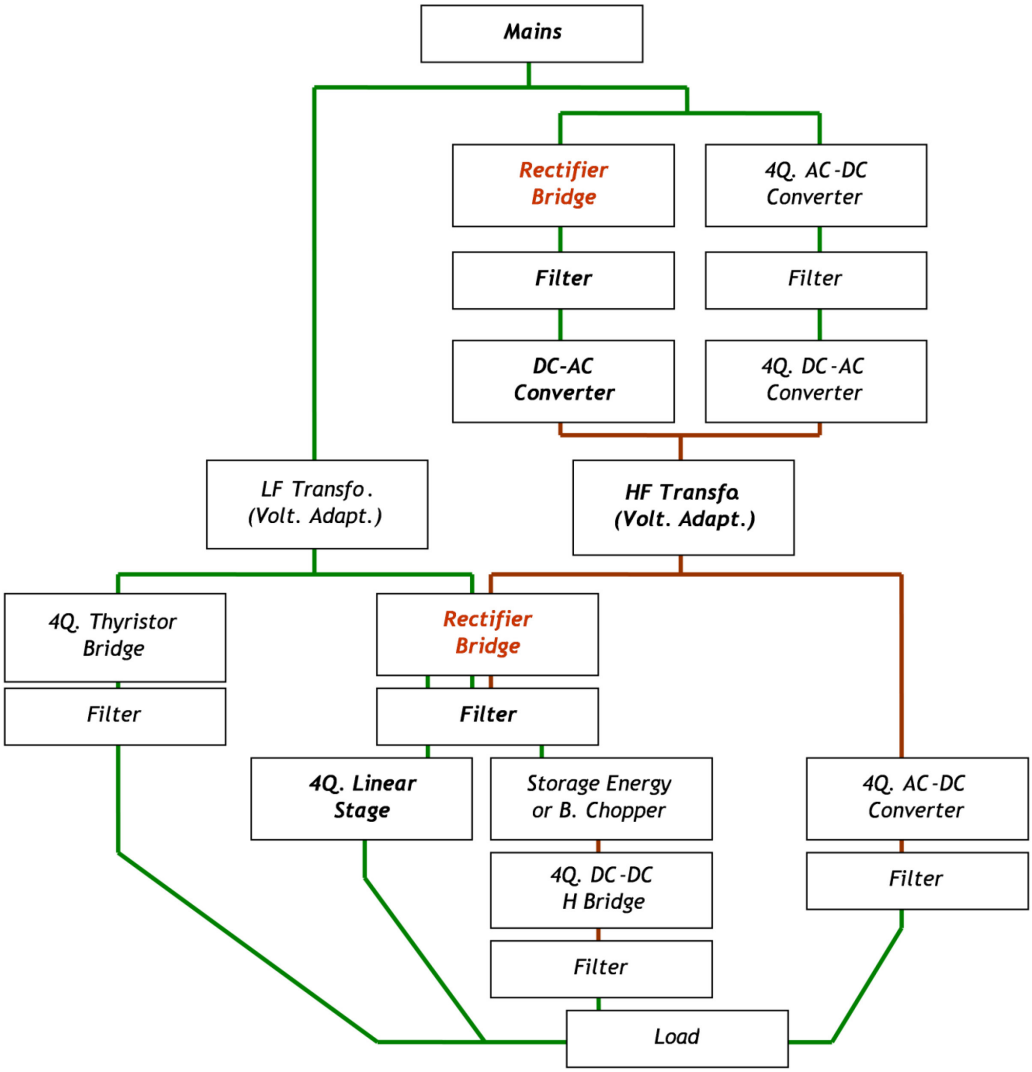


Fig. 12: Overview of possible combinations

The second part of this paper describes the design and realization of a power converter using a linear stage (indicated in bold in Fig. 12).

5 LHC120A-10V power converter design

This part describes the practical realization of a [±120 A; ±10 V] four-quadrant power converter, designed at CERN in 2003–2004 for LHC use.

5.1 Description

The converter was designed for being integrated into a high performance environment: its main use is to provide parts-per-million precision current to a superconducting magnet. A low level of EMC perturbations created by the power converter, on the input and output sides, and a high level of conformance toward the reference voltage to be followed (no distortion, high bandwidth) are strong requirements for the high precision electronics located in the power rack. Its integration in the existing tunnel is a natural constraint, which means that only switching base topologies are adequate: high efficiency minimizes the losses that must be evacuated from underground installations; and a small size and low weight are required for installation and repair interventions around the 27 km of the LHC tunnel. A long lifetime is also required from a system that will operate for more than 10–15 years.

5.2 Schematic overview

The converter is based on a high switching frequency phase-shifted standard topology, in series with a four-quadrant linear stage, and can be represented as shown in Fig. 13.

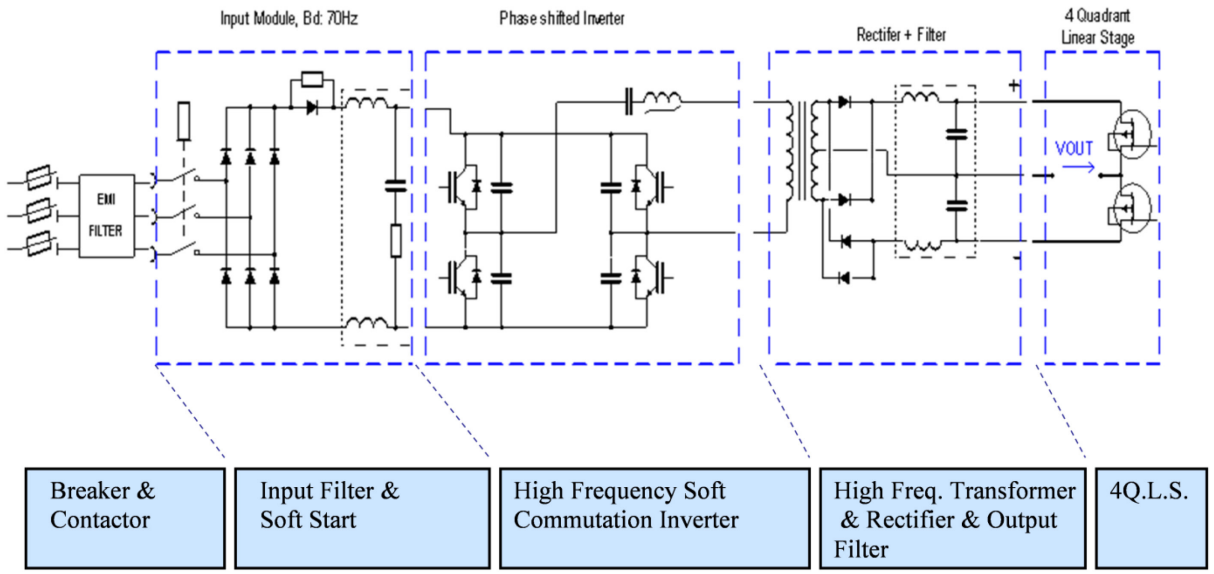


Fig. 13: LHC120A-10V schematic overview

Figure 13 shows that the power converter is in five parts.

- Protection and power control stage: a breaker is used for protection and safety reasons when an AC contactor is used to power the power converter or isolate it from the mains.
- AC–DC stage: a conventional rectifier bridge and input filter (70 Hz) with soft start capability provides DC voltage to the next stage.
- High frequency DC–AC inverter: a 70k Hz phase-shifted zero voltage switching (ZVS) inverter with insulated-gate bipolar transistors (IGBT) switches DC voltage into a high frequency voltage given to the power transformer in charge of adapting and isolating the output side.

– Isolation and rectifier stage: a high frequency power dual output transformer and low voltage Schottky power diodes output high frequency dual DC voltage to the four-quadrant linear stage.

– Four-quadrant linear stage: based on power MOSFET transistors (mounted in parallel on each side to boost the receiving energy capability), capable of absorbing and dissipating the entire load energy. This stage's performance is not dependent on a quadrant being in operation, and it has additional functions: minimum load of previous stage, active filter, and high rejection of the mains natural and expected 300 Hz ripple present at the AC–DC stage.

5.3 Four-quadrant linear stage

The main element of this power converter is the four-quadrant linear stage. In particular, the choice of power MOSFET for this stage leads to a specific design, to handle the inherent limitations of this kind of component (threshold, non-linear component).

5.3.1 *Principles*

Figure 14 shows a different working example, as a first approach to the system regulation laws.

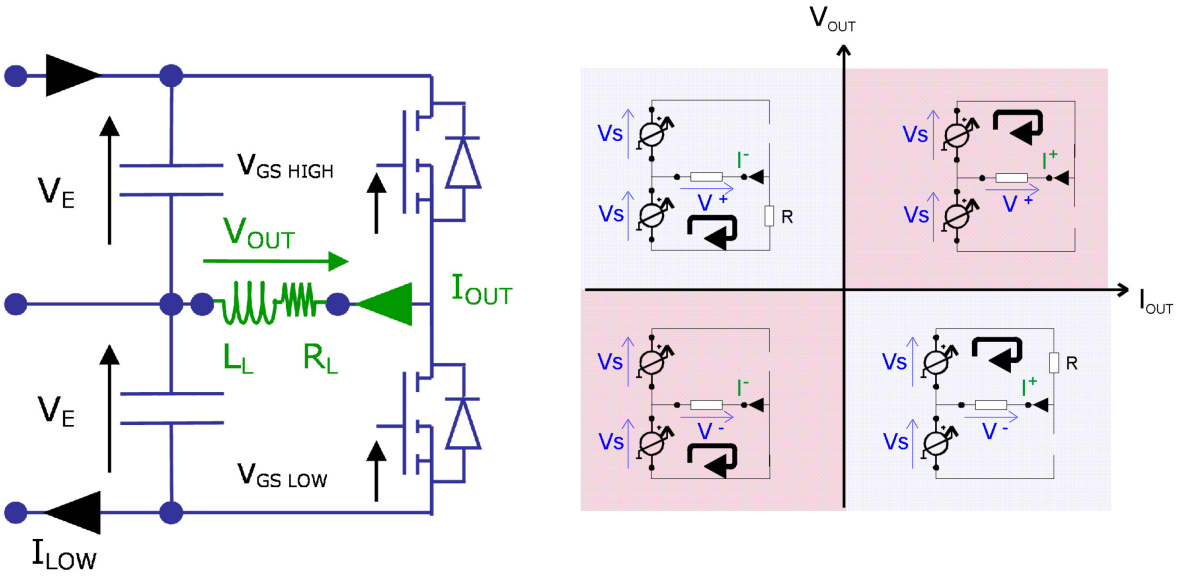


Fig. 14: Four-quadrant linear stage schematic (a) electrical schematics; (b) operational areas

The control principles can be simplified to two equations (Eqs. (3) and (4)), each of which are valid for two quadrants:

$$V_{OUT} = +\left(V_E - R_{HIGH} \cdot I_{HIGH}\right) \text{ Quadrants 1 and 2} \tag{3}$$

$$V_{OUT} = -\left(V_E - R_{LOW} \cdot I_{LOW}\right) \text{ Quadrants 3 and 4} \tag{4}$$

where R_{HIGH} and R_{LOW} are the equivalent power MOSFET resistances.

5.3.2 *Power MOSFET characteristics*

5.3.2.1 Power MOSFET, a natural current source

A power MOSFET is a natural current source, since the gate voltage determines the current flowing into it, independently from the voltage seen by it. This can be easily extracted from the manufacturer's data in Fig. 15, where a specific gate voltage leads to a constant current versus drain-to-source voltage V_{DS}. (Reference: FB180SA10, International Rectifier in this example below).

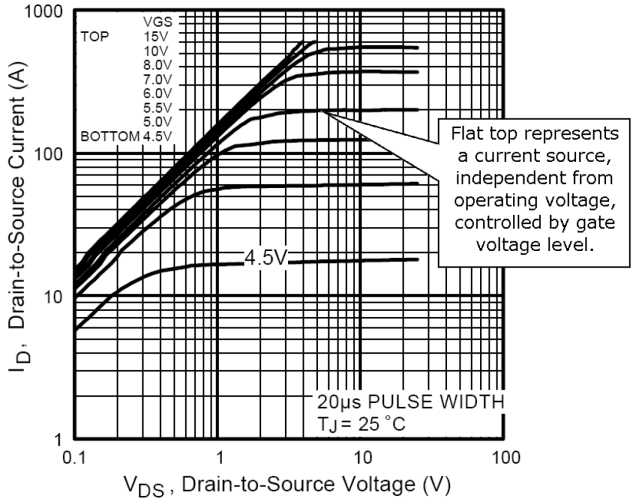


Fig. 15: Typical power MOSFET characteristics

The nature of the load involved, the superconducting magnet (current source per excellence), requires an output decoupling filter to be able to connect both the current source and the current load. Moreover, values of the load time constant involved in this practical realization were in a range that was so large that this option was not retained. A complete linear stage was nevertheless produced and successfully tested, using the intrinsic current source of a power MOSFET, being used in the flat part of its curve.

5.3.2.2 Power MOSFET transistor, a 'controlled resistance'

A power MOSFET transistor used as a 'controlled resistance' is a highly non-linear system. The following curves summarize the main phenomena that should be taken in account: influence of temperature, V_{DS} voltage, Miller capacitance, etc. Of course, the internal structure of a power MOSFET should be taken in account, especially with modern power MOSFETs, which are more able to switch than work in a linear mode.

5.3.2.2.1 Main parameters to be taken in account

Some key parameters are highlighted, always focusing on the gain G:

$$G = \frac{R_{DSON}}{V_{GS}}. \tag{5}$$

5.3.2.2.2 Gain variation over working range

A classical R_{DSON} versus V_{GS} curve shows that several orders of magnitude of static gain should be considered, where a linear model around an operating point is used. If a linear control system is chosen, the working range of the power MOSFET should be selected to minimize gain variations. Figure 16 shows a typical curve for a standard power MOSFET.

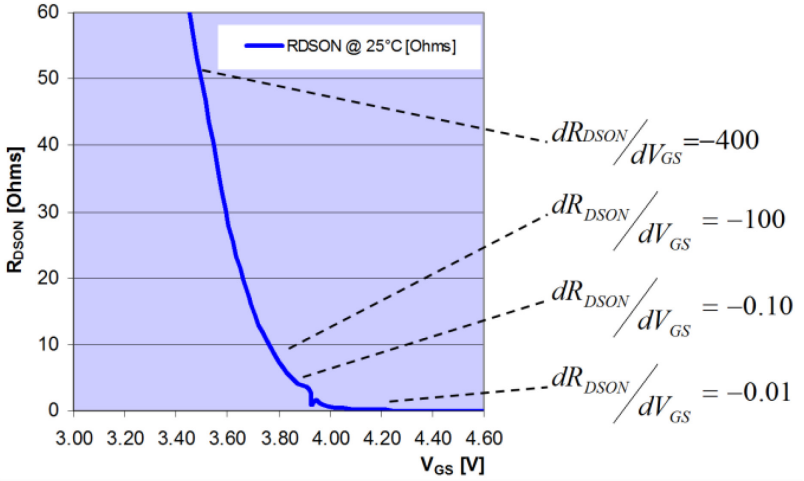


Fig. 16: MOSFET R_{DSON} overview

5.3.2.2.3 Threshold variations over a batch

The conduction threshold is a key parameter, since a transistor linear stage cannot expect a step voltage control signal that is driven by the linear control main loop to suddenly switch a power MOSFET into conductive mode without providing the correct V_{GS} threshold voltage. The knowledge of this threshold variation is mandatory when trying to cope with it. Manufacturers give a large range for this parameter since it can vary from 2–4 V. This means that a fixed threshold to approach the linear conductive mode is not a valid approach and cannot be considered for a safe and robust design.

5.3.2.2.4 Threshold variations and radiation

Variation of the threshold gate voltage versus radiation dose is a key factor for some converters used in particle accelerators. Figure 17 shows the results for a power MOSFET [1000 V; 15 A] threshold variation versus radiation dose; this power MOSFET is used in a test configuration to control a constant low current (50 mA).

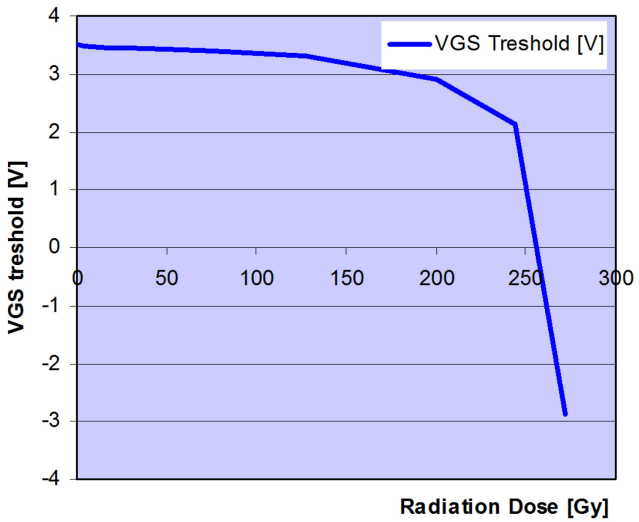


Fig. 17: Power MOSFET V_{GS} threshold variation versus radiation dose

Considering single-event sensitivity, the fact that a power MOSFET can stay in a continuous conductive state (even with a very low current being flowing through the transistor), with the voltage across it being lower than the maximum capability, makes this topology almost non-sensitive to single-event failures.

5.3.2.2.5 Temperature influence

The influence of temperature is well-known for power MOSFET transistors, with an R_{DSON} that increases with temperature. When controlling a power MOSFET transistor in linear mode, increasing the temperature introduces a negative threshold 'offset' as described in Fig. 18.

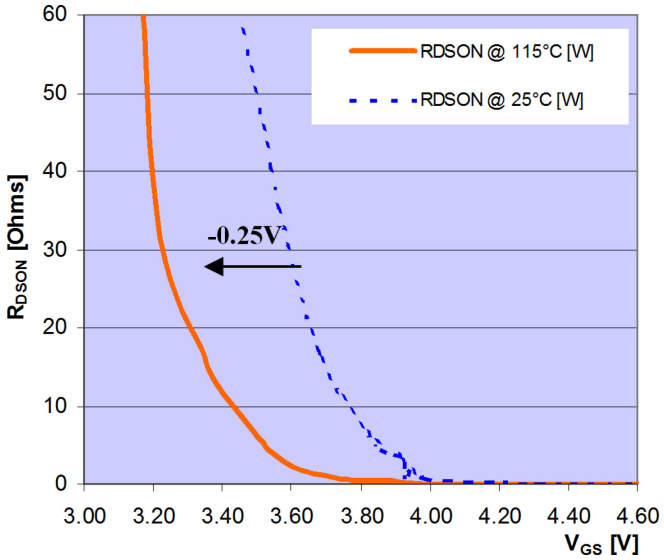


Fig. 18: MOSFET R_{DSON} versus temperature

This feature is important since, again, it prevents the use of a fixed threshold, *even* if trimmed per power MOSFET at 25 °C, for each power MOSFET threshold level.

5.3.2.2.6 V_{DS} influence

Gain is also influenced by the voltage across MOSFET V_{DS}. See the curves in Fig. 19. This curve has to be used to determine the minimum value of V_{DS} for operation. Indeed, in a classical linear stage, we will see that if maximum voltage is determined by the load operation area, the minimum value across a power MOSFET can be selected based on efficiency and control criteria. It can be observed that choosing a low operating voltage across the power MOSFET will lead to a square angle characteristic with a high rate of change that is difficult to control.

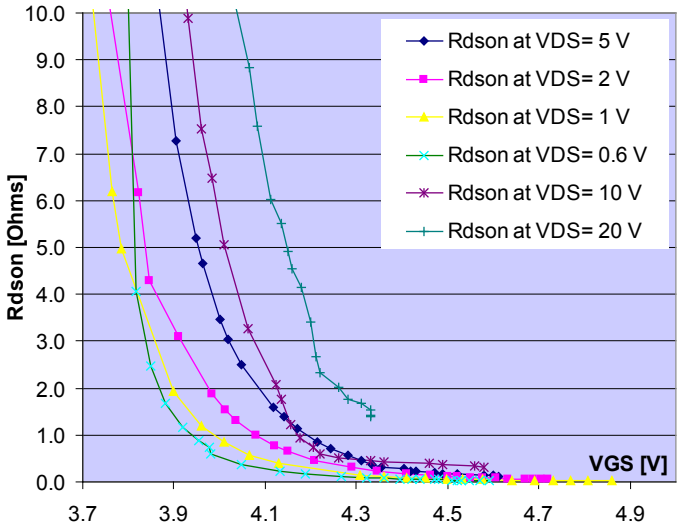


Fig. 19: Power MOSFET R_{DSON} versus V_{DS}

5.3.2.2.7 Miller capacitance effect

A signal applied to the gate voltage is loaded by a well-known capacitance that changes with the power MOSFET conduction status. This change could affect the bandwidth of the control signal if used with a high resistance in series with a power MOSFET gate. Total gate capacitance is a combination of the proper gate capacitance added to the output capacitance depending on the power MOSFET status: if a power MOSFET is conducting, and close to its minimum R_{DSON}, gate capacitance seen from the gate can be multiplied by a factor up to 2–3. In linear mode use, this capacitance can easily be derived from the manufacturer's data:

$$Q_g = C_{iss} \cdot \left(V_{GS\ Final} - 0\right) + C_{iss\ Miller\ add} \cdot \left(V_{GS\ Final} - V_{GS\ Threshold}\right) \tag{6}$$

where Q_g is the total gate charge, C_{iss} is the grid capacitance, $V_{GS\ Threshold}$ is the power MOSFET conduction threshold, and $C_{issMilleradd}$ is the Miller capacitance.

From this equation can be found the capacitance range:

$$V_{GS} \le V_{GS\ Threshold} \rightarrow C_{iss}\ , \tag{7}$$

$$V_{GS} \ge V_{GS\ Threshold} \rightarrow C_{iss} + C_{iss\ Miller\ add}\ . \tag{8}$$

5.3.2.3 Power MOSFET model conclusions

Controlling a power MOSFET like a 'variable resistance' presents two major problems when using a linear system: a conduction threshold on the gate applied voltage, and a high difference of 'static' gain depending on the resistance value to be obtained.

5.3.3 ***Power MOSFET push–pull control***

A linear loop is used to control the power MOSFET push–pull, based on an opposite signal from the control loop sent to the gate voltage of the power MOSFET transistor branches. In that configuration, the control loop has to provide a threshold voltage added to the small signal control signal once the power MOSFET reaches the linear zone. It can be noticed that when switching from the upper to the lower leg, the control signal has to provide a step of two times the gate voltage threshold.

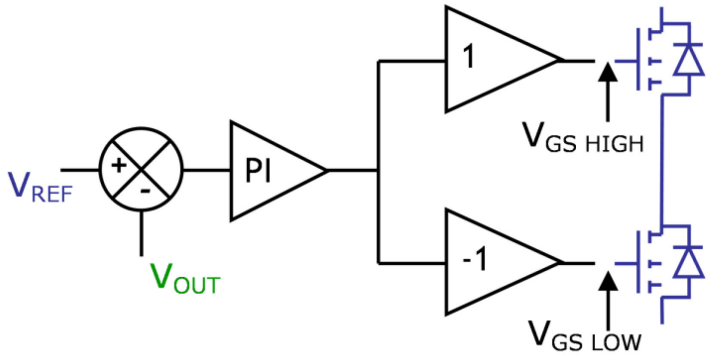


Fig. 20: Push–pull control principles

Even if this is highly non-linear due to the power MOSFET's R_{DSON} behaviour, this principle works quite well when taking in account the high level of R_{DSON} when used with a low current, while a high level of current requires a low value for R_{DSON}. Indeed, a small signal analysis would show that it is possible to choose a working voltage across the power MOSFET (design choice) so that each compensate themselves, giving an acceptable gain variation.

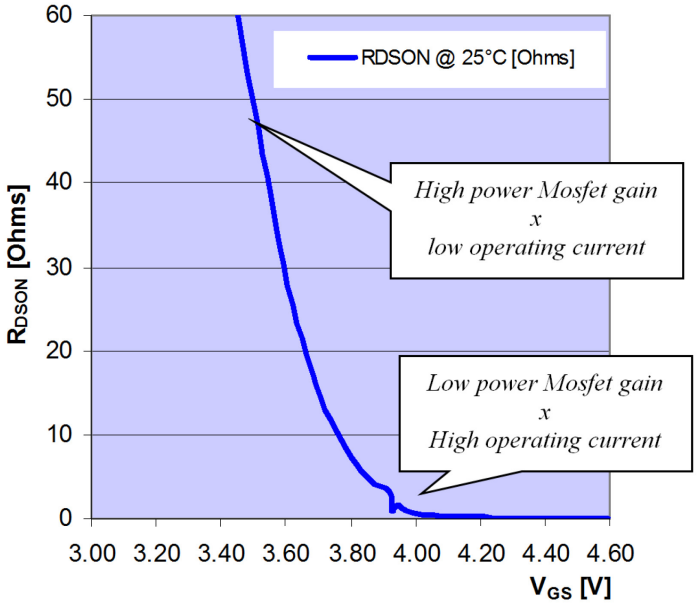
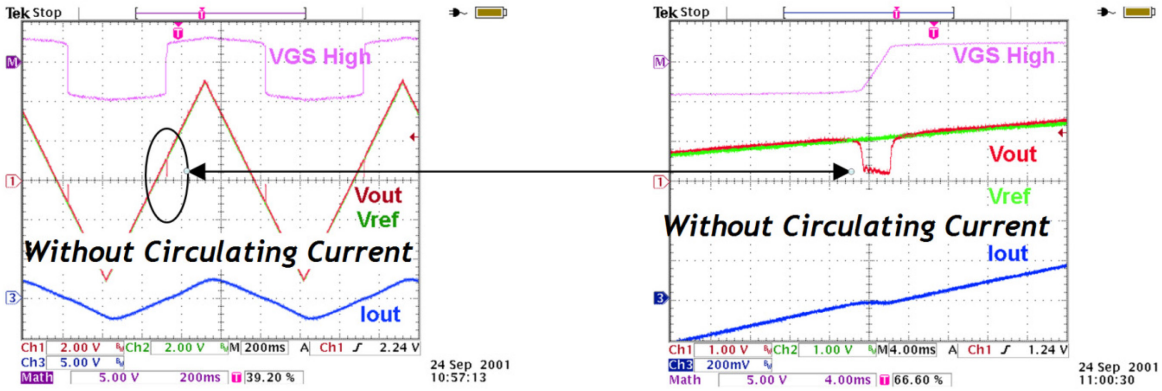


Fig. 21: Small signal analysis detail

5.3.4 *Inherent limitations of a push–pull stage*

Even if it is very simple, a basic push–pull system has an uncontrollable zone at null current, since voltage cannot be 'obtained' from the current in the load if it is null. This problem is enhanced with a superconducting load, where full voltage can be apply with null current. In the same order, the [0 V; 0 A] point is an unstable point. When applied to a power MOSFET stage, two severe limitations appear.

- Gate voltage threshold, which makes it difficult to use a simple linear system (a control signal given by the loop has to switch between $+V_{\text{GS threshold HIGH}}$ and $-V_{\text{GS threshold LOW}}$ as fast as possible to avoid the output becoming uncontrolled (blank area, where no power MOSFET conducts). Figure 22 shows the step voltage required from the voltage control loop; up to 8 V in this example (two times 4 V from each power MOSFET threshold level).
- Use of power MOSFET equivalent resistance area can be very wide, almost saturated to an almost open state, giving a four decade gain variation, which again is very difficult to control in a simple way, even with the self-compensating effect of the current being related to R_{DSON} values.



(a) (b)

Fig. 22: MOSFET-based push–pull stage limitations: (a) cycle overview; (b) zoom on 0 A crossing transition

5.3.5 *Circulating current*

A circulating current is a controlled current, internal to the converter – not seen by the load – that maintains a known state for both the DC–DC power converter and the four-quadrant linear stage. This feature was requested to obtain high level performance. It provides the following functions.

- Provides a minimum load for the DC–DC power converter and avoids a completely non-loaded output side of the dual output DC–DC power converter. The power DC–DC switched-mode converter is therefore easily controllable, without a problem of management of continuous and discontinuous mode, and there is a clamping voltage on the output capacitors on each side, whatever the output conditions.
- Pre-conditions the linear stage power MOSFET, close to the threshold gate voltage. The linear stage loop will be able to manage high-side and low-side transitions since none of the power MOSFETs requires a voltage step to change mode (conductive or not).
- Limits working zone of the power MOSFET used in linear mode. It is possible to redefine artificially the range of operation of power MOSFET of each leg in linear mode playing with the value of the circulating current combined with the operating voltage.
- Less important but very convenient is the capability of having a current circulating inside the power converter when trimming a power MOSFET, if a sharing procedure has to be used; this is when using power MOSFETs in parallel per side. A power converter can be trimmed without any external load, with an adjustable level of current being set to optimize this possible procedure.

Figure 23 shows a simple representation of the two loops involved in that mode. The addition of this loop – circulating current – provides real advantages, and gives possibility to – dynamically – trim the system very deeply (in this case the value of the circulating current is controlled depending on an adjustable limit on the output current). It is nevertheless an additional loop, which should not disturb the two loops already in place: power MOSFET push–pull and power DC–DC control. Great care of the bandwidth of this loop is mandatory, and high signal dynamic performance of the overall power converter are partly deduced from this loop's characteristics.

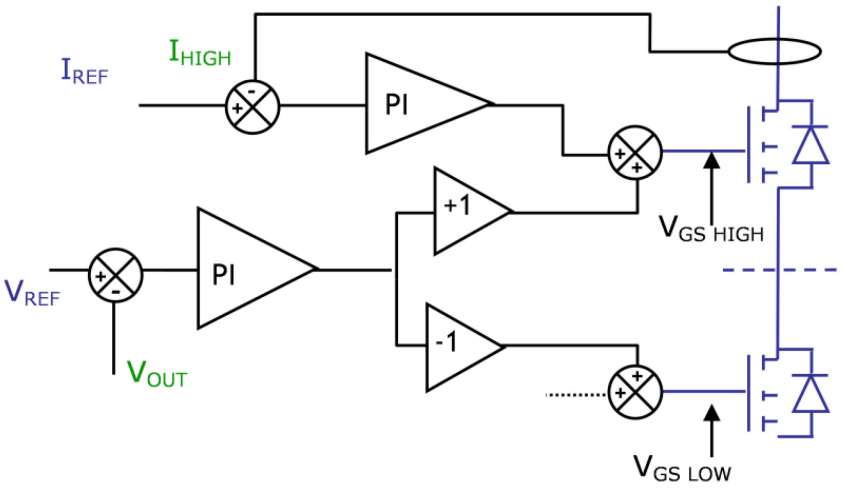


Fig. 23: Push–pull control principle with circulating current loop

5.3.5.1 Influence of circulating current on operational range

Circulating current can be used to limit drastically the highly non-linear zone to a more practicable one, limiting the high gain zone. This is particularly interesting since it doesn't cost too much in efficiency, reducing considerably the less controllable linear zone of the power MOSFET (high resistance, high

gain), which would lead to instability. Avoidance of this problem is especially critical with a superconducting load, where the power converter maximum output voltage can be applied in a receiving quadrant while current, even if slightly moving, is very low.

In the case where a linear stage provides full voltage at a current close to zero, a power MOSFET will be used with a high resistance value, inducing a very high gain, and becoming a critical zone for linear loop stability. The circulating current strategy ensures minimum current flows in each power MOSFET, which are then capable of producing the desired output voltage with medium values of R_{DSON}, while not just relying on output current. Figure 24 shows a drastic reduction of the range of R_{DSON}, using only 1 A of circulating current.

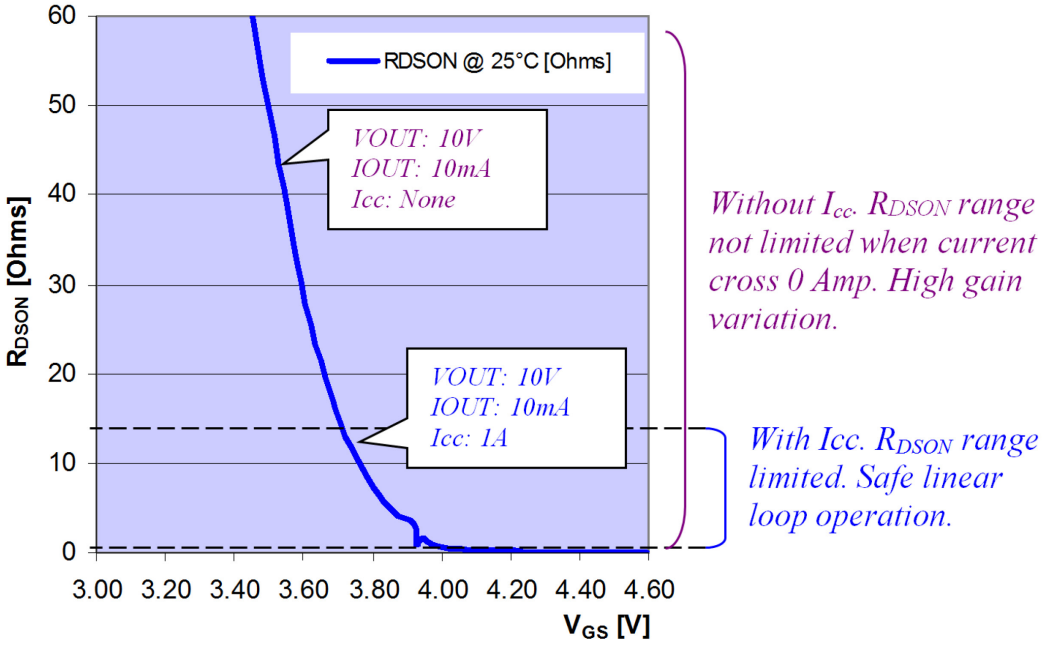


Fig. 24: Small signal analysis detail

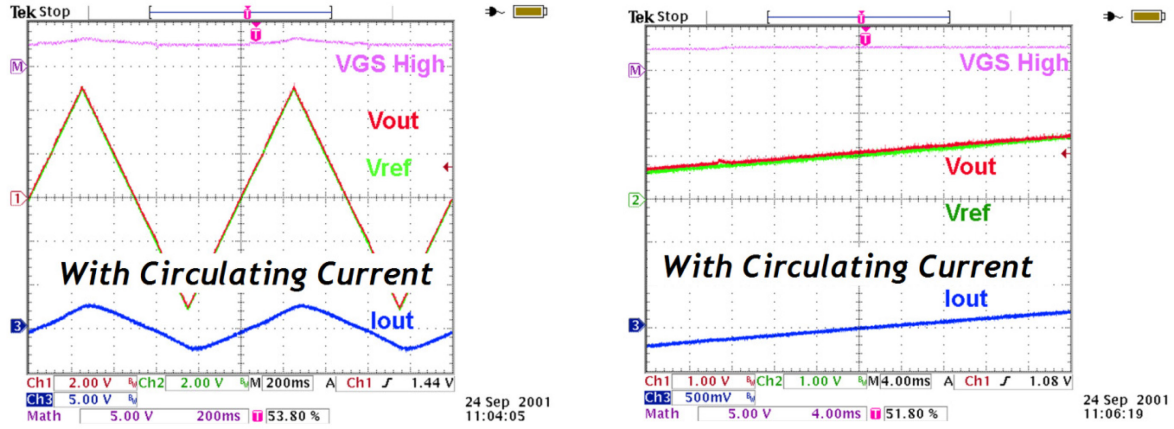
5.3.5.2 Circulating current implementation

Implementing this feature requires the addition of a current transducer per side. (Note that these two sensors can be used to deduct the output current of the load, which is often required for load protection.) In such a case, the following can be noted.

- Knowing the output current will make it possible to adjust the circulating current level to improve overall efficiency.
- Even if these sensors are of low precision (percentage level), they should be of a sufficiently high bandwidth that they do not interfere too much with the inner loop.
- It is possible to use shunts in series with each power MOSFET to provide a self-damping behaviour if the gate voltage is applied to a power MOSFET gate and measurement shunt.
- It is mandatory to use a higher reading range than the power converter produces, since each sensor will alternatively, and depending on the current polarity, see the output current added to the circulating current at a maximum output current if non-null (depending on the circulating current strategy). It is nevertheless possible to use a circulating current only around the 0 A area, making it possible to use a low-current sensor. This cost-effective solution will limit the potential benefit of the addition of a circulating current loop.

5.3.5.3 Circulating current results

Figure 25 shows the result of a circulating current on gate voltage, being constantly close to the threshold voltage of each power MOSFET.



(a) (b)

Fig. 25: Circulating current improvement effect: (a) cycle overview; (b) zoom on 0 A crossing transition

5.3.5.4 Circulating current possible operation

Circulation current leads to losses, especially when the output conditions are far from 0 A. The worst example is full output voltage, where circulating current causes the largest amount of energy to be lost in a power transistor. Considering that this circulating current is only useful close to 0 A output current, different strategies can exist, with I_{LIMIT} close to 0 A output current, to avoid extra losses.

A first possible strategy, with circulating current only present close to transitions, is given below:

- $I_{OUT} < I_{LIMIT}$ $I_{CC} \rightarrow$ $ON_{high\ value}$ Operating close to 0 A output current is possible;
- $I_{OUT} > I_{LIMIT}$ $I_{CC} \rightarrow$ OFF Circulating current removed above a threshold.

Another possible strategy, with circulating current always present, is given below:

- $I_{OUT} < I_{LIMIT}$ $I_{CC} \rightarrow$ $ON_{high\ value}$ Operating close to 0 A output current is possible;
- $I_{OUT} > I_{LIMIT}$ $I_{CC} \rightarrow$ $ON_{low\ value}$ Circulating current is always present, even if the value is reduced.

The I_{CC} low value is determined so that high frequency dual output voltage DC–DC is sufficiently loaded on the non-leading side to avoid overvoltage. It can be noticed that a very low level of I_{CC} is sufficient to polarize both power MOSFETs, and therefore avoid a too long delay before entering the safe 0 A crossing zone.

Figure 26 shows the positive effect of a non-null circulating current on the capability of dealing with a high current change rate. If the two operating cases seem almost equal for operating close to 0 A output current, the result is nevertheless different when taking into account the speed of the circulating current loop. Indeed, this additional loop will be lower than the main controlling loop and stabilization time can become critical if dI/dt is too fast. If this can occur, the second solution is a lot better. This is particularly interesting when the converter has to work on a pure resistive load, where dI/dt is not limited by the load.

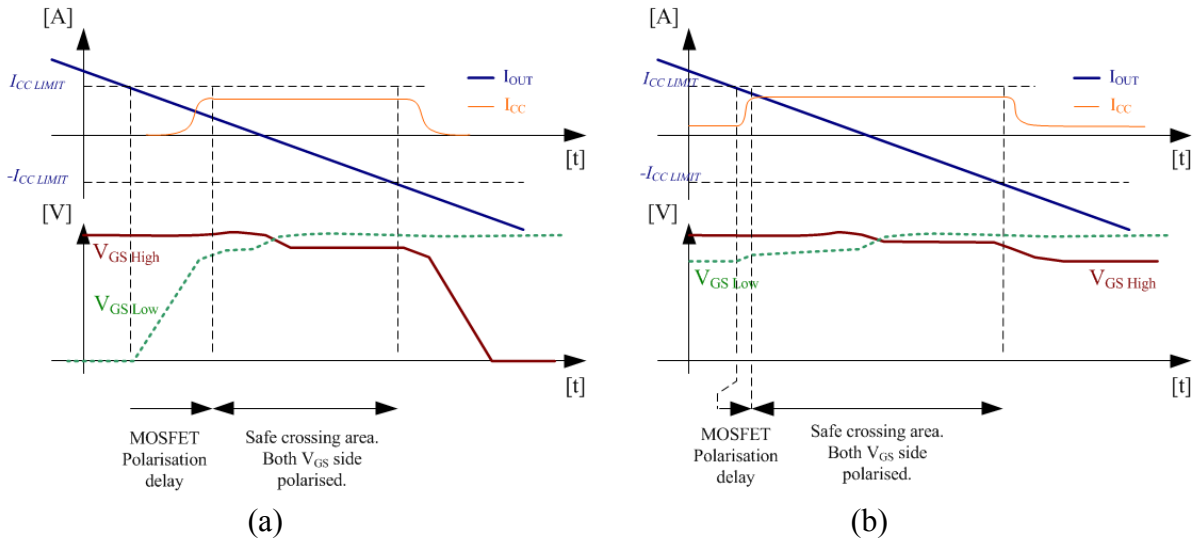


Fig. 26: Effect of circulating current on power MOSFET gate polarization: (a) circulating current set to null value case when not required; (b) circulating current being always non-null, with value changing according to the output current value.

5.3.5.5 Influence of the number of power MOSFETs on a linear loop

The minimum number of power MOSFETs to be used is determined by power or, better, by the energy to be absorbed by the linear stage. It is obviously possible to use a large number of power MOSFETs so that the V_{BIAS}, V_{DS} voltages across MOSFETs in generator mode can be decreased, while keeping a reasonable controllable area for the power MOSFETs when used at a high current in generator mode.

Reducing V_{BIAS} makes it possible to increase efficiency, at the price of additional power MOSFETs. Nevertheless, this improvement is balanced by the fact that MOSFETs will work in a higher gain area, due to the R_{DSON} characteristics curve, when absorbing energy from the load, leading to a potential instability. If this design feature can easily be taken in account, increasing the power of an existing converter does not just require an increase in the number of output power MOSFETs; control loops have to be reworked to ensure proper operation.

5.3.5.6 Medium and high frequency rejection results

As noted above, a power MOSFET is a natural current source, and it will offer a natural rejection of both medium and high frequency, from DC–DC dual output to four-quadrant linear stage (4QLS) output. If rejection is part of the control loops, the medium and high frequency rejection feature is clearly of benefit to the active power MOSFET characteristics.

Figure 27 shows voltage measurements from a real converter; V_{OUT} is the output voltage measurement, when V_{E+} is the voltage provided by the DC–DC power part. Measurements were performed at maximum power, to stress the input power filter regarding the 300 Hz expected content.

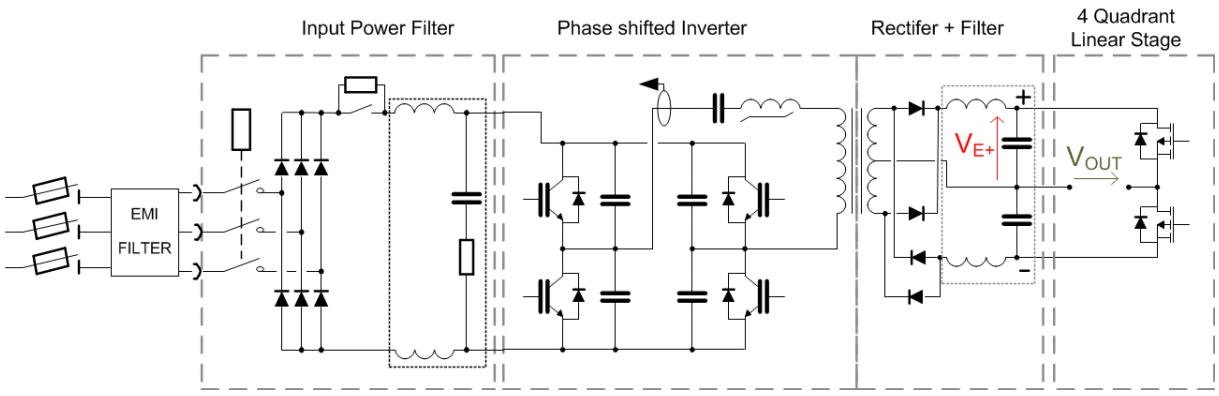
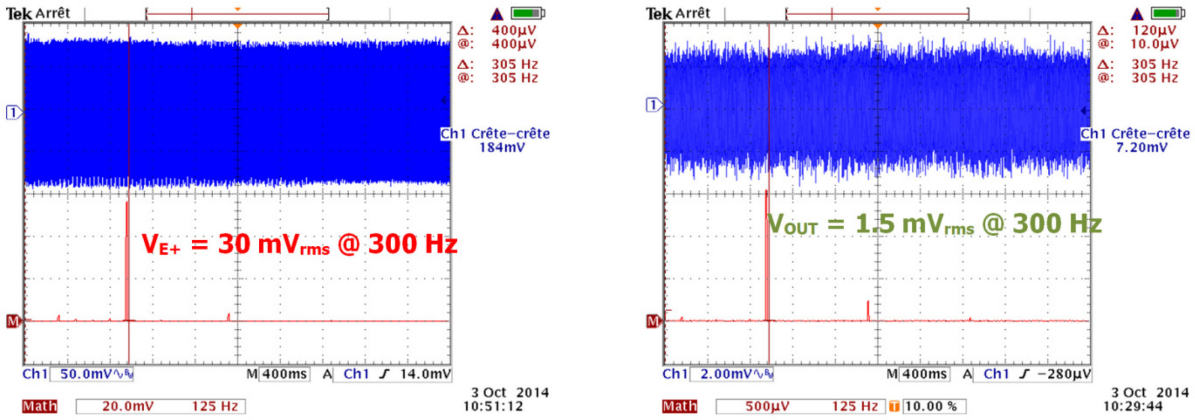


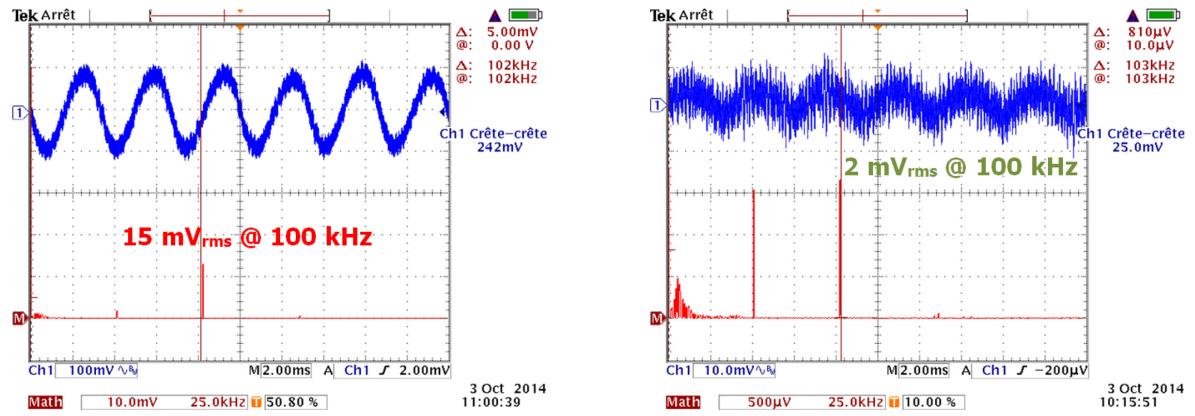
Fig. 27: Schematic with voltage measurements of interest

Figure 28 indicates that medium frequency rejection is very high; the performance comes from the voltage loop natural rejection, related to its bandwidth. The result is a dramatic reduction of the 300 Hz by a factor of 15. Decreasing V_{BIAS} will decrease the rejection of medium frequency since the gain of the power MOSFETs will be lower, being close to their saturation area (flat and low gain). A trade-off between the efficiency and the level of noise at 300 Hz is to be evaluated. Figure 29 shows the direct reduction effect of the power MOSFET current source behaviour in the high frequency range.



(a) (b)

Fig. 28: 4QLS medium frequency reduction measurements on a real converter: (a) 300 Hz level on DC intermediate Bus; (b) 300 Hz level on the output voltage.



(a) (b)

Fig. 29: 4QLS high frequency reduction measurements on a real converter: (a) high frequency level on DC intermediate Bus; (b) high frequency level on the output voltage.

5.4 Converter control loops

Since a four-quadrant linear stage is fed by the power DC–DC (inverter plus dual output filter), a control strategy for the power DC–DC, four-quadrant linear stage, and circulation current loops has to be decided upon. Since cascaded loops are involved, a factor of ten is considered between power DC–DC and four-quadrant linear stage loop speeds. The 4QLS is the fastest loop, since the generating and absorbing modes both using the 4QLS, but not the generating one. Indeed, 4QLS is fed by the load in quadrants two and four, and power DC–DC can be transparent in that mode.

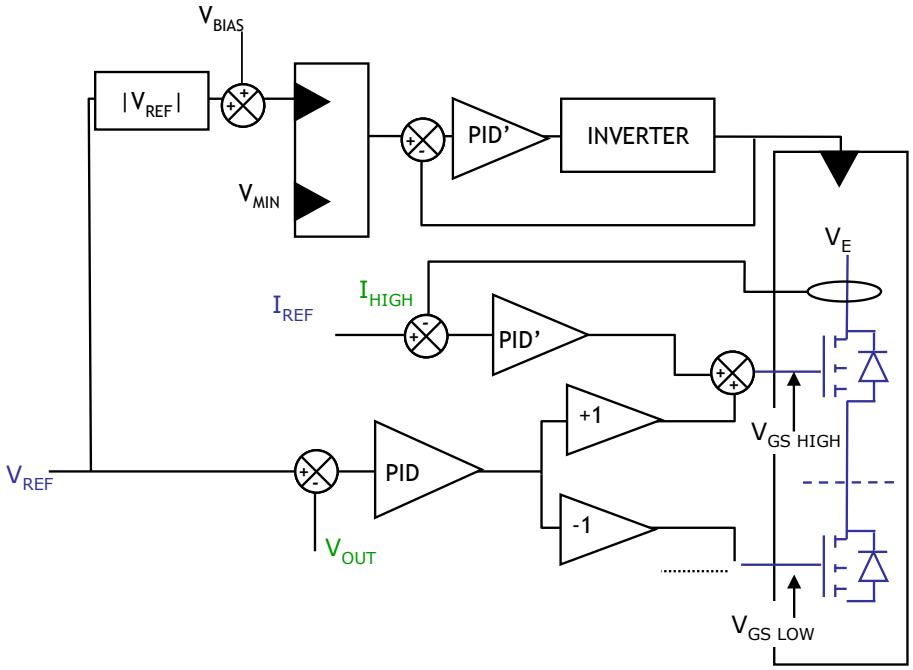


Fig. 30: Overall control strategy

Circulation current is always the slower loop, since polarization of the power MOSFET should be completely transparent from the other loops, and being assimilated to perturbations to be rejected by the other loops. The current rate can give a minimum speed for this loop to achieve non-distorted crossings.

5.4.1 *Power DC–DC loop*

This loop is at least ten times slower when compared to the four-quadrant linear stage. A voltage reference coming from the converter user was chosen to be the same bandwidth as the power DC–DC, to avoid the four-quadrant linear stage becoming faster than what the power DC–DC could provide, leading to conflicts. In this case two settings are used trim the power DC–DC reference: V_{BIAS} and V_{MIN}. The first is used so that the four-quadrant linear stage can work in a given operating range (not too saturated) as described in previous chapters. The second is used to ensure that power DC–DC is always at minimum loading by circulating current and a minimum given output voltage reference, leading to a minimum power. It also makes the loops more robust close to [0 A, 0 V], limiting the operating zone where all three loops are active at the same time. See Fig. 31.

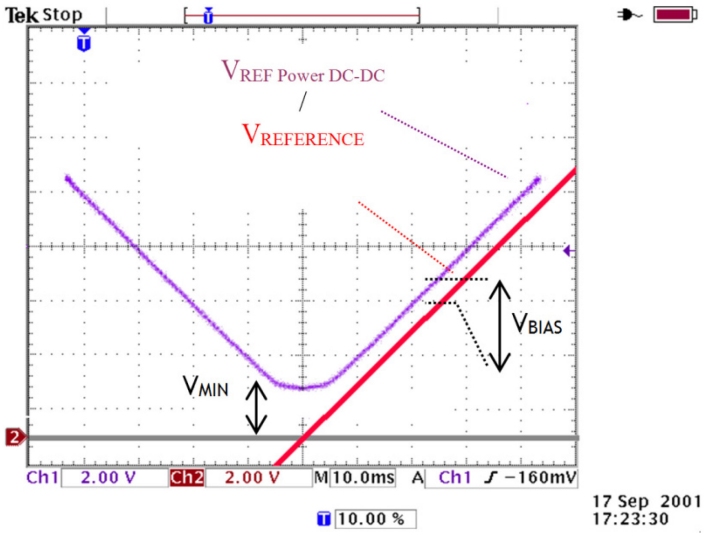


Fig. 31: Typical power DC–DC reference versus converter reference

6 Practical results

The converter was manufactured by the company Efacec, Moreira da Maia, Portugal, in 2004–2005, which was also in charge of the rack design and the industrialization of the proposed solutions, following the CERN design. The converter module is housed in a 5U 19″ 45 kg power module, as shown in Fig. 32. It includes control signal, interlocks, and signalling capabilities on the front of the module.

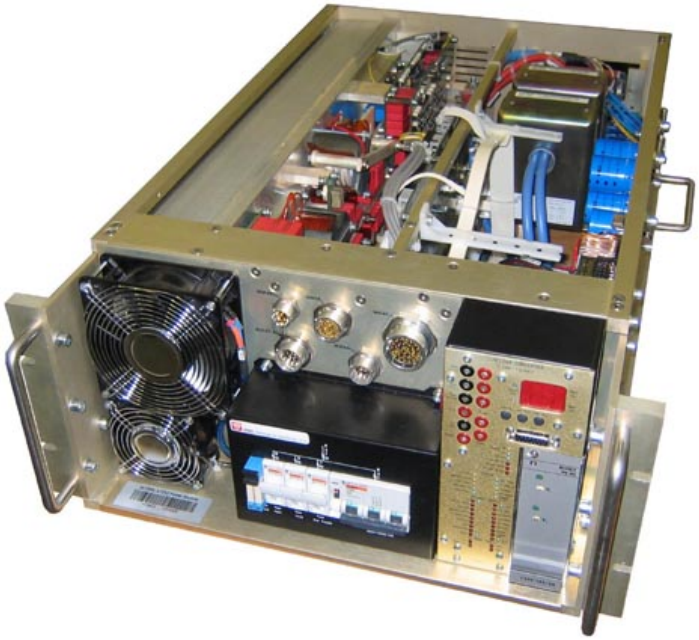
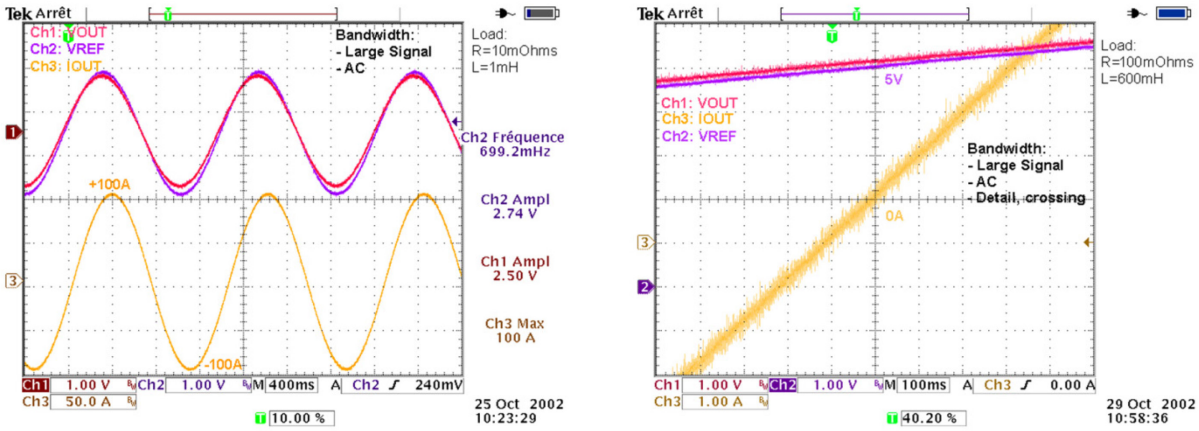


Fig. 32: LHC 120 A-10 V power module

Power converter characteristics during production confirmed the initial choice of the topology. The system is robust, with a bandwidth of 1 kHz, without any distortion of the voltage while crossing the 0 A point, and the EMC level was confirmed to be very low. The different trimming possibilities (V_{BIAS}, V_{MIN}, circulation current levels (low and high level), and its current limit when changing level) and the cascade type design made adjustments easy to achieve, since the system is not too interleaved. Efficiency was measured to be relatively low (72% at full power) due to linear stage losses.

Figure 33 shows a 0 A crossing plot, without any distortion, for different loads.



(a) (b)

Fig. 33: Crossing 0 A measurement for different magnet loads: (a) 0 A crossing performance on low time constant magnet; (b) detail of a 0 A crossing on large time constant magnet.

Moreover, the bandwidth of the system is constant whichever quadrant is used, ensuring safe operation on a superconducting magnet in regard to the very high precision level (some parts per million) of the current loop, which will not be affected by the load operating conditions. Figure 34 shows a typical plot of generator and receptor bandwidth. A voltage step is required, with a small signal added, so that the converter operates in generator mode, then receptor mode. The current doesn't change at this timescale, since the superconducting magnet keeps it unchanged (large time constant)

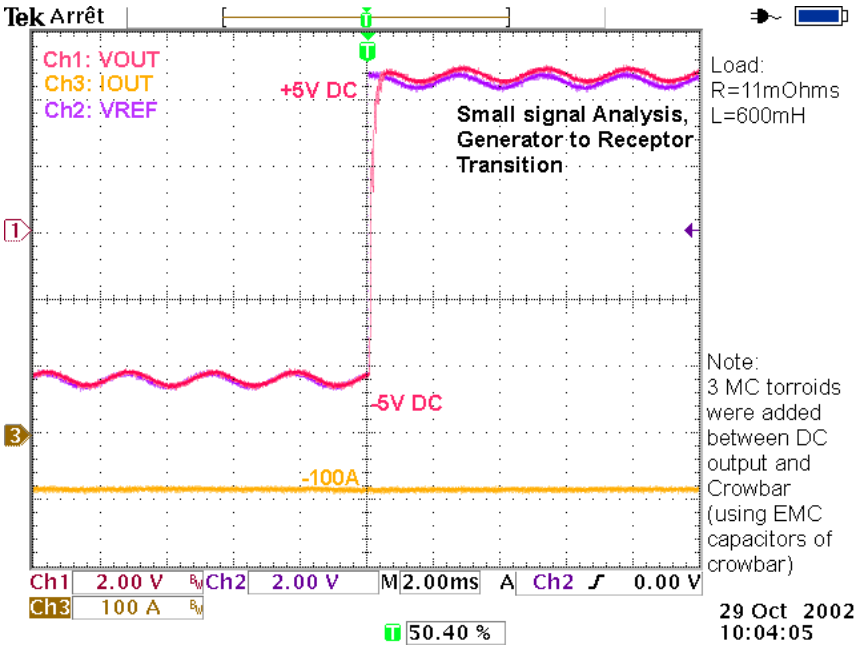


Fig. 34: Small signal analysis in receptor quadrant

EMC levels were measured on the AC side (input) and the DC side (user side, superconducting magnet in series over hundreds of metres). If the AC level is low, according to the IEC regulation standards, the DC side was found to be extremely low, especially in the high frequency range. This result is mainly due to the soft commutation inverter, added by the one switching stage alone topology. This choice was made possible to easily deal with parasitic components (limiting common and differential mode capacitors of transformers and secondary side rectifiers) using output filter as an

additional EMC component. The linear stage is obviously a quiet element that doesn't affect converter EMC, in opposition with a second switching stage. See Fig. 35 for a typical plot at maximum current and voltage.

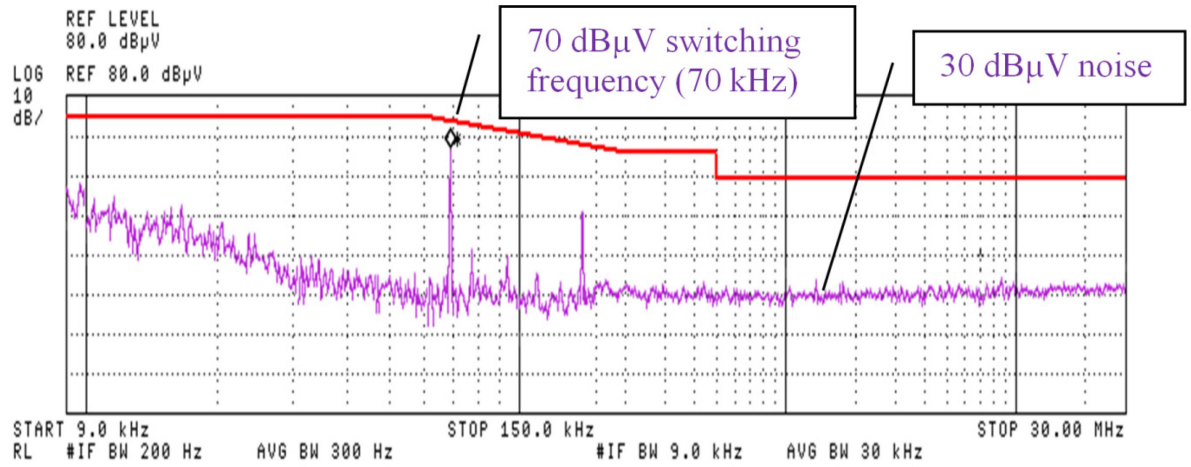


Fig. 35: DC output side EMC curve (1500 Ω probe)

7 Additional topics

This kind of converter type project is generally, and in CERN's case, put in place for providing several magnets for a given physics machine, with the additional complexity of load integrity and safety. Converters tests can then be put into perspective. The following chapters treat these topics to help the designers of converters not miss these important points. If taken into consideration at project start-up, it is possible to save a lot of time, with a real possibility of improving global project efficiency.

7.1 Load protection

Load protection is always a critical point, which cannot be neglected. Indeed, the high level of energy that can be stored in an inductor requires that a current path is always given to it, to avoid possible damage to the magnet (an inductive path, being opened, results in high voltage stress and dielectric damage).

CERN uses intensively the system called a crowbar, being a set of bidirectional controlled power switches in series with a resistor (though none in specific cases); this system is placed in parallel with the output of the converter, and has the function of protecting the load from a wrong condition, at the level of the power converter. A tentative opening of the load current path by the power converter would typically activate the crowbar system to avoid damaging the load. This system could be seen as replacing free-wheeling diodes in the case of a one-quadrant converter powering an inductive load. Thyristors are often chosen, since once set they are conductive (overvoltage detection across the crowbar system triggers the switches), and they will remain conductive as long as load current is present. Nevertheless, some systems use power MOSFETs as well, with the need to ensure that they are always safely controlled, letting them conduct the magnet's current. A simplified model is presented in Fig. 36.

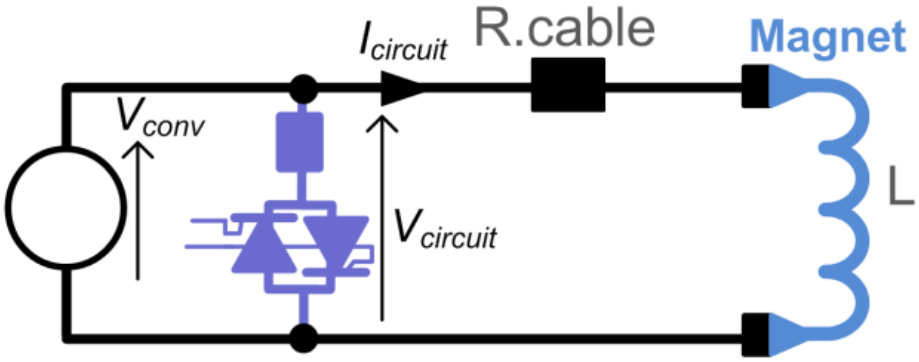


Fig. 36: Simplified overview of the crowbar

The design of such system, even if not complex, must ensure safe operation of the components being used. Very often, a capacitor will be placed in parallel with the crowbar system, limiting dV/dt across it so that the speed of closing the switch, in series with the crowbar resistor, is compatible with the voltage reached across the crowbar, the power module, and finally the circuit.

In the LHC machine, power converters are modular systems that can be removed from their slots, with the risk of disconnecting a power module for replacing it (case of its failure), while a lot of current is still flowing through it. Taking such a case into account, the crowbar system was designed not to rely on the output stage power capacitors of the converter, providing its own; on the other hand, crowbar systems are sometimes placed some metres from the power converter so that they do not create conditions for oscillations (self-inductance path through the crowbar capacitors in series), and then have to be limited in their value.

In addition, the capacitors placed on the crowbar side should not lead to too high dI/dt conditions for the thyristors when triggered, since collecting the capacitor peak current (sudden discharge) added to the long time constant's inductor current.

Figure 37 shows the capacitors (red blocks on the right-hand side) being placed away from the thyristors (left-hand side), to provide sufficient inductance in series in their path, to limit thyristor dI/dt when turning on.

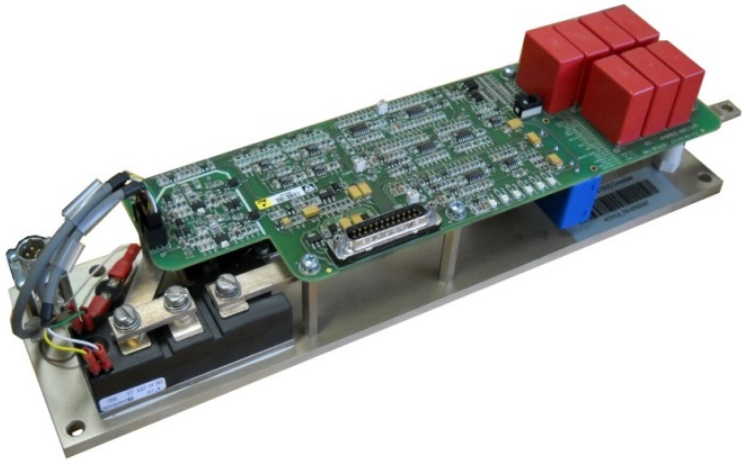


Fig. 37: Example of a CERN crowbar system

It can happen that power resistors can be requested to accelerate current discharge and the load energy removal process, taking into account their load energy capacity, rather than their power rating. Since the phenomena observed deal with energy versus time rather than power requirements, the function versus time of thermal management (resistor and semiconductor baseplate), and power losses

inside each component (the level decreasing with time as the current is reduced), they can be considered to be unusual by designers of switching power supplies, who are more used to 'permanent conditions' system. A safe design must deal with these considerations, to ensure a proper level of semiconductor junction or case temperatures during the full discharge of a superconducting magnet.

7.2 Reception, qualification and tests

For several projects being conducted at CERN for the LHC machine, four-quadrant converters designs were validated; and tests on the series were performed with very restricted access to the final superconducting loads. CERN used some tricks to test these four-quadrant units on standard loads.

7.2.1 *Back-to-back test*

A four-quadrant converter is able to deliver or receive energy from an inductive load, but also from another identical four-quadrant converter. It becomes then possible to test each unit versus another unit, and reach an unlimited time constant load, with the addition of an additional control loop for one of the module assimilated to the load, and controlled as such. This additional control loop ensures that the current and voltage developed across the module are following and simulating a high time constant load, copying a superconducting magnet (Fig. 38).

If this method is very elegant and very powerful for some heat tests, to determine whether the four-quadrant part (where energy is managed or dissipated) is correctly designed, the control of inherent converter and the one added for simulating the superconducting load must be very robust, since it is probable that any instability initiated by one of the power modules would be caught by the other one, which would be of identical design, with the same weaknesses, if any. It appears that a decoupling inductor is generally required (self-inductance of cables can be sufficient), its value being determined by the bandwidth of the additional simulating load controller.

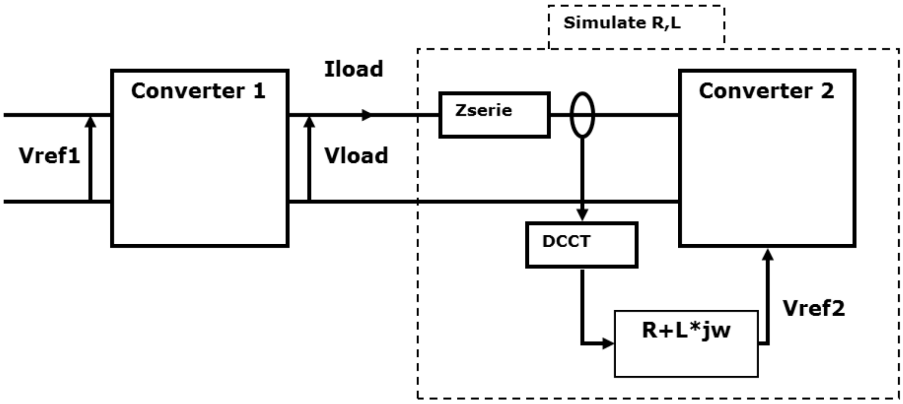


Fig. 38: Two converters operating back-to-back

7.2.2 *Four-quadrant converter bandwidth characterization*

If determining the voltage bandwidth of a converter is in general a relatively easy task, determining the behaviour of a four-quadrant converter becomes a more complex task; indeed, the converter should demonstrate that it regulates its output voltage in generator or receptor mode, leading to test facility constraints. Ideally, a converter should be operating in a receptor quadrant, in a steady state, while receiving input stimulus on its reference, to allow a Bode diagram to be plotted. This can lead to some potential issues regarding the fact that a power module is generally not designed to stay powered at a DC receptor point, the design being optimized based on the fact that load energy will decrease. That having been said, the total amount of energy that the converter can handle (except if sent back to the mains) is usually limited (by design), and in consequence, the time to measure the performance of the converter is also limited.

A simplified method consists of analysing a step-response to deduce the bandwidth of the converter alone. This simple test, even if not as rich as a frequency systematic Bode diagram type test, is often sufficient to obtain the stability margin and main performances (speed) of a system.

Taking this into account it is possible to reach the high dissipative area [V; I] of a four-quadrant converter on a standard inductive load (a few milliHenry plus a few milliOhms), with the condition of a large voltage step. A method has been put in place with two signal generators in series, providing a large step voltage (to select the receptive quadrant) superposed with a small signal square waveform (to study the step-response) (Fig. 39). The method allows the obtaining of any points for the receptive quadrant, with the combination of the current before the large step occurs, and the value of this step, in a very efficient way.

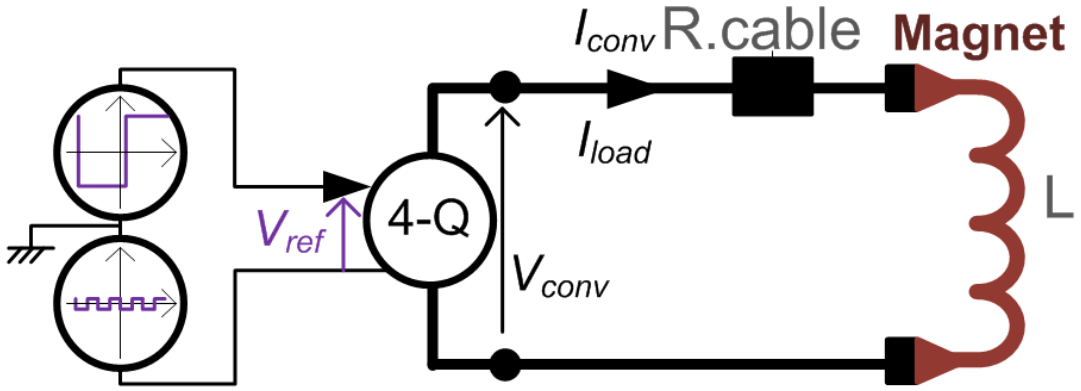
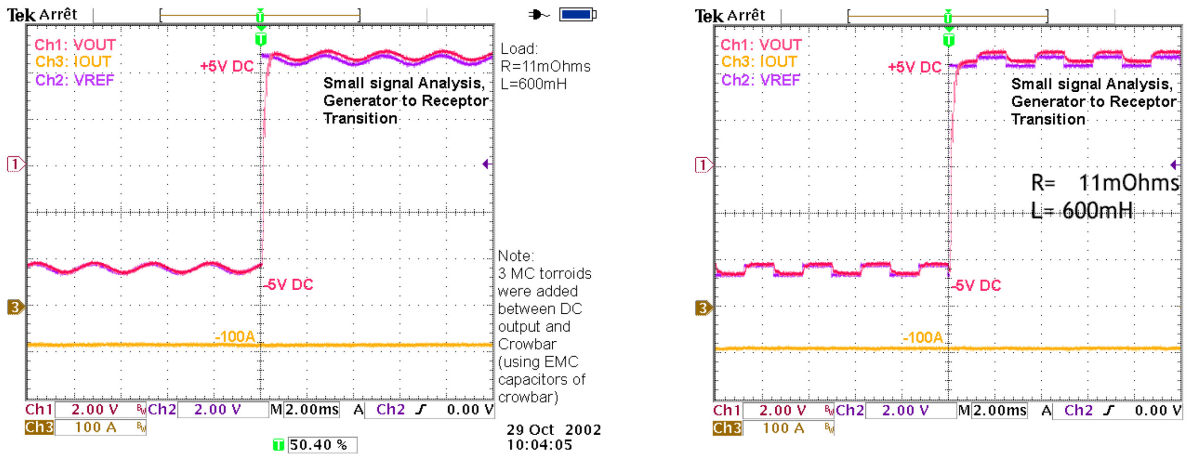


Fig. 39: Characterization of voltage loop using two signal generators

The result is the sinusoidal and square small signals, which are shown in Fig. 40. These were obtained from a superconducting magnet, but would have been equivalent to that obtained from a warm magnet of just 3 mH, which would be available in a standard test laboratory.



(a) (b)

Fig. 40: Example of step-response on a high time constant load, with the generator to receptor quadrant transition (a) on sinus type small signal; (b) on square type small signal.

8 Perspectives

CERN started a new project in 2013 for advanced four-quadrant power converters, using the same principles as those one described in this paper, but with an additional redundancy feature. It is intended that this will capitalize on the four-quadrant power stage using power MOSFETs and controlled as a

pure current source, which it is by nature, and no longer a programmable resistor. Achieving this will allow a current source to be naturally placed in parallel, with the capability of a redundant four-quadrant power converter.

9 Conclusions

This paper briefly described four-quadrant power converter topologies. Critical technical points from a CERN internal design were presented, with practical results obtained on a series of converters produced for the LHC accelerator. The requirement for not having any disturbances in the operating zone (especially around [0 A; 0 V]) was achieved, thanks mainly to the circulating current loop, in its function to avoid dead zones, and to optimize MOSFET control.

The design presented was one of the less noisy converters in the LHC, which was, after some years of operation, considered to be a wise approach. EMC compliance was found to be a very important point, for example while looking for explanations of beam instability, while tracking every system regarding its potential to disturb the beam at specific medium frequencies, in the range 1–50 kHz.

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Power Converters for Cycling Machines

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Abstract
Cycling accelerators require power converters that are capable of storing the energy that oscillates between lattice magnets and the converter during the acceleration process. This paper presents the basic requirements for such systems and reviews the various electrical circuits that have been used for a variety of differing applications. The designs currently used for fast-, medium- and slow-cycling accelerators are presented.

Keywords
Energy; power; acceleration; flicker; energy exchange; waveform.

1 Introduction

Some of the material presented in these proceedings is concerned with converters which supply direct current to the magnet loads. This is relevant to the storage ring, in which the particle momentum is fixed or where its variation with time is so slow that the energy increase in the magnets is smaller or of the same order as the resistive energy loss; in such circumstances, the converters can be regarded as variable-amplitude d.c. systems. However, in most true synchrotrons, which accelerate the charged particle beam, the magnetic fields in the bending and focusing elements (if these are part of a separated function lattice) are required to be raised in a relatively short time, from the low amplitude required at beam injection to a maximum value corresponding to peak beam energy; the fields then need to be reduced in as short a time as possible, so as to be ready to accept the next pulse of injected beam. Thus, these cycling accelerators require power converters that are capable of delivering the appropriate cycling waveform.

As the accelerator magnets cycle from the injection to peak field, energy is transferred from the power converter to the magnet gap; during the deceleration phase, this magnetic energy has to be removed from the magnet. In the case of a d.c. accelerator, this process occurs during switch-on and, far later, during the power-down of the converters. The stored energy is small compared to the resistive loss in the magnet during any extended period of d.c. operation, and hence this 'reactive power' is not considered in the power supply specification. However, in a cycling accelerator, the largest component of energy supplied from the converter to the magnets is usually the magnetic energy associated with the field amplitude. It is therefore significantly more efficient to recover that energy during the deceleration phase and store it for the next acceleration cycle. Hence, a suitable energy storage system is an essential part of a converter for a cycling accelerator, and this requirement is central to the design and specification of such equipment. The nature of suitable engineering schemes depends on the cycling frequency specified for the accelerator; these can vary from less than 1 Hz for the large synchrotrons associated with particle physics, to 50 Hz for small- to medium-sized accelerators. The details of the most suitable circuits are discussed in the following.

2 The choice of waveform

2.1 Accelerator requirements

The simplest waveform that could be envisaged for a cycling system is 'conventional' alternating current. However, consideration of the requirements for particle acceleration indicates that this is highly inappropriate. This is explained in Fig. 1. Injection occurs at low field and the particles are then

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accelerated to peak energy, at the maximum of the sine wave; the acceleration occurs only during the positive part of the cycle. The simple a.c. waveform shown in the figure produces major disadvantages:

- less than one-quarter of the cycle is used for acceleration,
- there is an unnecessarily large r.m.s. current, as the negative part of the wave is superfluous,
- therefore there are high resistive and a.c. losses,
- there is a high magnetic field variation with time at injection (see the following),
- The energy is exchanged 4 times per cycle as only two are required.

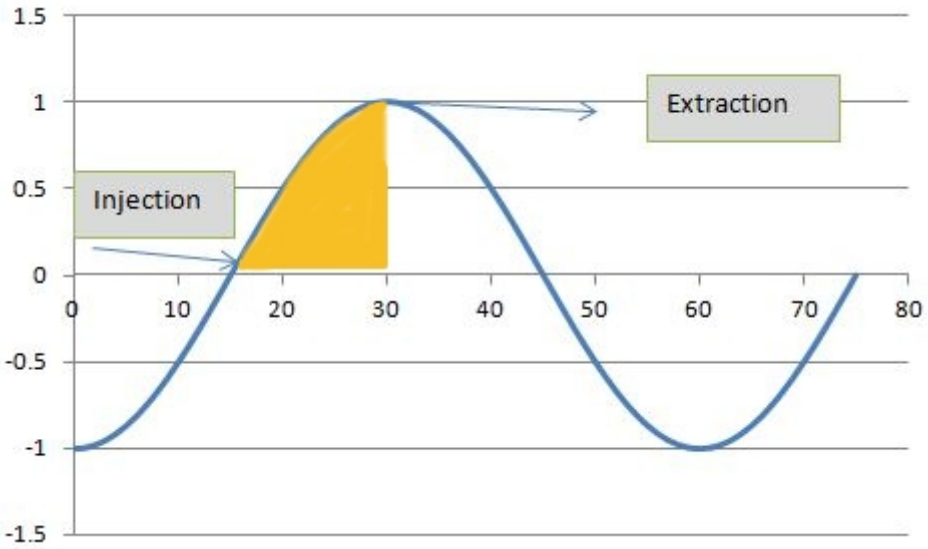

Fig. 1: Simple a.c. is an inappropriate waveform for a cycling accelerator. The simple alternating current wave is not used without biased current.

Before examining other possible waveforms in detail, it is worthwhile examining the detailed waveform requirements of the cyclic particle accelerator.

2.1.1 RF system

The radio frequency system provides the voltage necessary to accelerate the particles, or, where the particles are losing energy due to synchrotron radiation, to replace that loss and maintain the beam at the required momentum.

2.1.1.1 Acceleration

- Particle momentum (rigidity)

$$mv \propto B; \tag{1}$$

- RF accelerating voltage

$$V_{\mathrm{rf}} \propto \mathrm{d}B/\mathrm{d}t; \tag{2}$$

- RF power

$$P = k_1 V_{\mathrm{rf}} I_{\mathrm{beam}} + k_2 (V_{\mathrm{rf}})^2 \tag{3}$$

$$= (\text{power transferred to beam}) + (\text{loss into cavities});$$

where

- mv is the momentum of a particle mass m;
- B is the magnetic flux density in the bending magnets;

- I_{beam} is the beam current;
- k_1 and k_2 are constants fixed by the RF system and accelerator design.

Any discontinuity in dB/dt would call for a step change in RF voltage and power and could generate beam instabilities, leading to possible beam loss.

Additionally, the particle beam is held in a potential well, created by the RF voltage, in a mechanism known as 'phase stability'. The trapped particles move within that potential well, executing 'synchrotron oscillations'. The frequency of these oscillations (the 'synchrotron frequency') is one of the fundamental parameters of the accelerator and is proportional to dB/dt. Large values of this frequency can also cause resonant beam loss, and this places a further constraint on the field gradient, particularly at injection (see the following).

2.1.1.2 Synchrotron radiation

This radiation is emitted by ultrarelativistic particle beams (electrons at $E \sim 1$ GeV; protons at $E \sim 1$ TeV) when bent in a magnetic field:

- synchrotron radiation loss $\propto B^2E^2$, (4)
- for a constant radius accelerator $\propto B^4$, (5)
- V_{rf} to maintain energy $\propto B^4$, (6)

where E is the energy of the circulating beam.

The magnet waveform therefore needs to have no discontinuities in amplitude (effectively impossible with an inductive load) or gradient. To limit the maximum RF voltage that needs to be generated by the RF amplifier (and therefore to limit its power ratings), the maximum value of dB/dt should not greatly exceed the average required over the acceleration cycle.

2.1.2 Field gradient at injection

The variation of magnetic flux density with time generates eddy currents in any conducting material located within the field. In a cycling accelerator, eddy currents will occur predominantly in the walls of a metallic vacuum vessel, with smaller eddy currents present in the magnet poles themselves. These currents generate magnetic field disturbances:

- negative dipole field—reduces main field magnitude;
- negative sextupole field—generates negative chromaticity and could drive resonances.

The magnitude of these unwanted disturbances is inversely proportional to the beam momentum, which is, of course, determined by the dipole magnetic field, B. Hence the effect of eddy currents is proportional to

$$(1/B)(dB/dt), \text{ expressed as } \dot{B}/B \quad (7)$$

It should be noted that the synchrotron frequency is determined by the same ratio.

This parameter, the ratio of the field gradient to the field magnitude, is most critical at injection, when field and beam momentum are low and when the beam is being 'captured' into its correct synchronous phase. This situation is illustrated in Fig. 2.

It will be seen that the value of (1/B)(dB/dt) will be one of the determining factors on which the waveform suitability is judged.

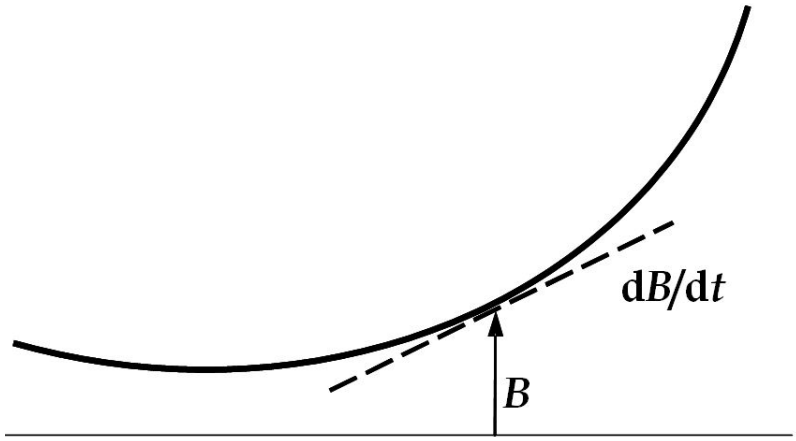

Fig. 2: Field gradient and magnitude at injection

2.1.3 Discontinuous operation

In some situations, the accelerator may only be required to undertake an acceleration cycle at time intervals that are much longer than the normal cycle time. For example, the circulating beam in a storage ring may decay very slowly with time. To maintain constant beam current, which is very valuable to experimenters, the booster synchrotron which feeds the main ring is needed to operate in 'top-up mode', in which the beam is only accelerated and injected once every '*n*' booster cycles, with the value of *n* varying according to the operational details of the storage ring. The booster could be operated continuously whatever time delay is required between injection pulses, but this results in unnecessary power consumption. Hence it is most efficient if the power converter can deliver an excitation waveform that allows discontinuous operation at intervals determined by the rate of loss of the stored beam, as illustrated in Fig. 3.

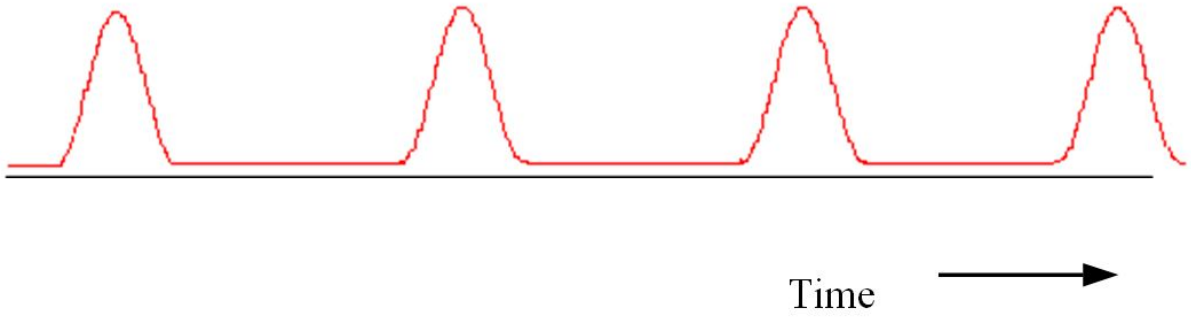

Fig. 3: Discontinuous acceleration cycles as used for 'top-up' injection; note that the delay between cycles is much in excess of the actual cycle time. Several strategies have been observed among top-up machines: at fixed interval (every *x* minutes or seconds) it is called d*t* (Diamond, APS); at fixed beam current decay (as soon as the *I* beam has decreased by *x*%) it is called d*I* (SLS, Elettra, Soleil, Bessy, Spring8, Petra).

2.2 Possible waveforms

Having established that a normal alternating current is not suitable for powering a cyclic accelerator and having examined the criteria against which waveforms should be judged, a number of more suitable waveforms can be considered.

2.2.1 Linear ramp

A linear field ramp and associated waveforms are shown in Fig. 4. It can be seen that the uniform gradient throughout the cycle results in a very high value of $(1/B)(dB/dt)$ at injection when the field magnitude is low, and some form of smooth transition into the ramp (the 'front porch') would be necessary.

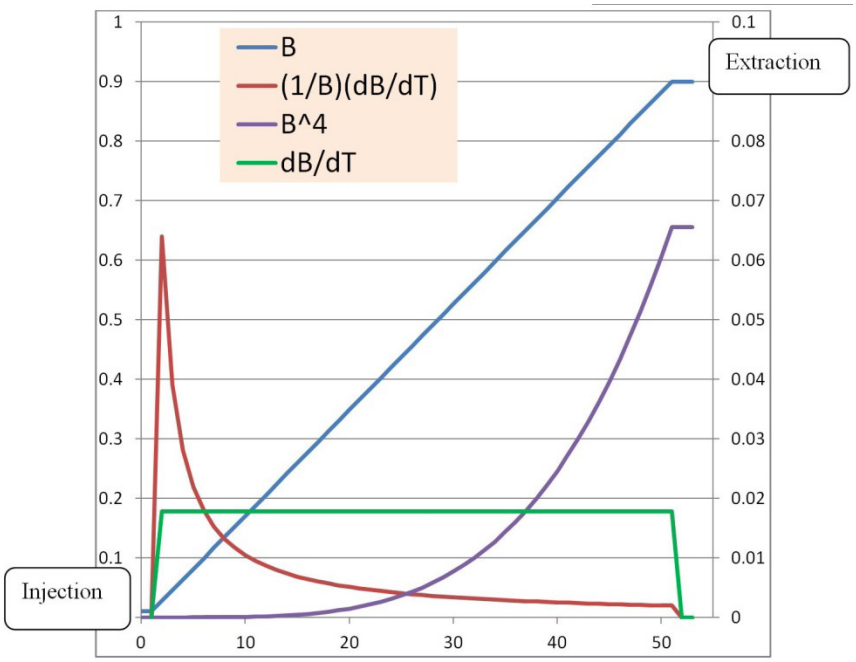

Fig. 4: A linear field ramp between injection and high energy (extraction) (B). Also shown is the gradient ($\mathrm{d}B/\mathrm{d}t$), B dot over B [$(1/B)(\mathrm{d}B/\mathrm{d}t)$], and the function determining synchrotron radiation loss (B^4).

2.2.2 Biased sine wave

This waveform, shown in Fig. 5, is based on the use of a half sine wave with a direct current bias of equal magnitude to the sine wave's peak value.

It can be seen that the biased sine wave provides a lower maximum value of $(1/B)(\mathrm{d}B/\mathrm{d}t)$ at injection compared to the linear ramp. However, the variation of gradient during the cycle has a higher maximum value than that produced by the linear variation and, hence, higher RF voltage would be required. Additionally, higher RF power would be needed if the beam was emitting synchrotron radiation, as the integrated value of the B^4 curve is higher.

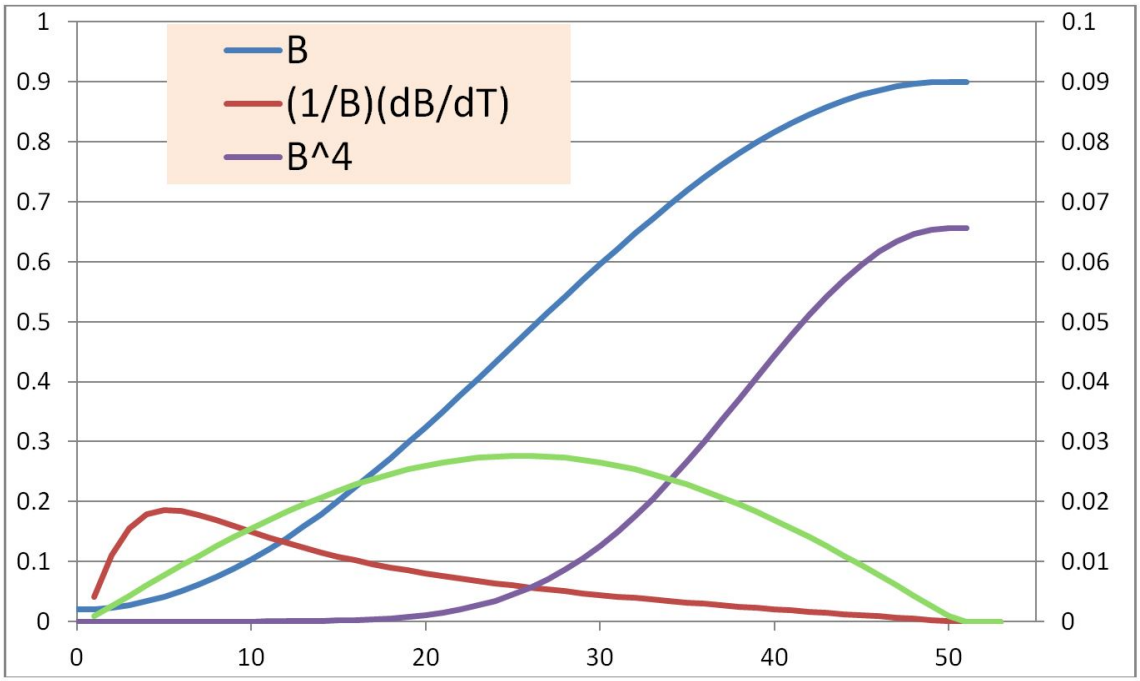

Fig. 5: A biased sine-wave field variation between injection and high energy (extraction) (B). Also shown is the gradient ($\mathrm{d}B/\mathrm{d}t$), B dot over B [$(1/B)(\mathrm{d}B/\mathrm{d}t)$] and the function determining synchrotron radiation loss (B^4).

2.2.3 *'Custom specified' waveform*

A better alternative to either of the two waveforms presented in Figs. 4 and 5 would be to have a variation with time that could be specified by the accelerator operator, i.e., a custom specified waveform. A possible example is shown in Fig. 6.

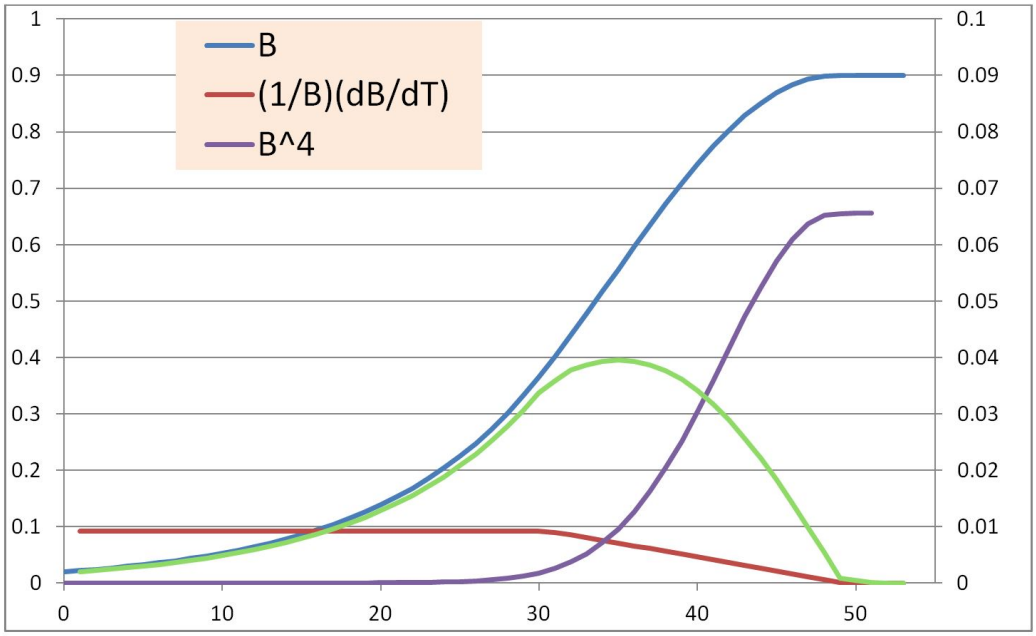

Fig. 6: A 'custom specified' field variation between injection and high energy (extraction) (B), designed to provide a low gradient during and just after injection. Shown is the gradient ($\mathrm{d}B/\mathrm{d}t$), B dot over B [$(1/B)(\mathrm{d}B/\mathrm{d}t)$] and the function determining synchrotron radiation loss (B^4).

The waveform is based on a constant value of $(1/B)(\mathrm{d}B/\mathrm{d}t)$ during and for a significant time after injection, which subsequently declines to zero at peak field. If the accelerated beam were to emit synchrotron radiation, the late increase in the B^4 term would result in a significant reduction in RF power, although the peak RF voltage is increased as the maximum in the $\mathrm{d}B/\mathrm{d}t$ term is higher.

2.2.4 *Waveform comparison*

A comparison of the three different waveforms presented in Figs. 4, 5, and 6 is given in Table 1.

Table 1: Comparison of suitability of three possible magnet waveforms

Waveform	**Suitability**
Linear ramp	Gradient constant during acceleration Limited voltage needs in the power supply $(\mathrm{d}B/\mathrm{d}t)/B$ very high at injection and low energy
Biased sine wave	$(\mathrm{d}B/\mathrm{d}t)/B$ maximum soon after injection but much lower than the linear ramp. Very limited control of the waveform during acceleration
Beam optimized waveform	Provides low $(\mathrm{d}B/\mathrm{d}t)/B$ at injection and up to half the wave. Presents engineering challenges such as much more voltage requested in the power supply and across the magnet terminals

It can be seen that the choice of waveform is usually a compromise between different criteria and is often predicated by the electrical engineering circuits that are available; this issue will be discussed later in the paper.

3 Power ratings in cycling systems

3.1 Electrical parameters

Figure 7 shows a typical bending magnet with its equivalent circuit.

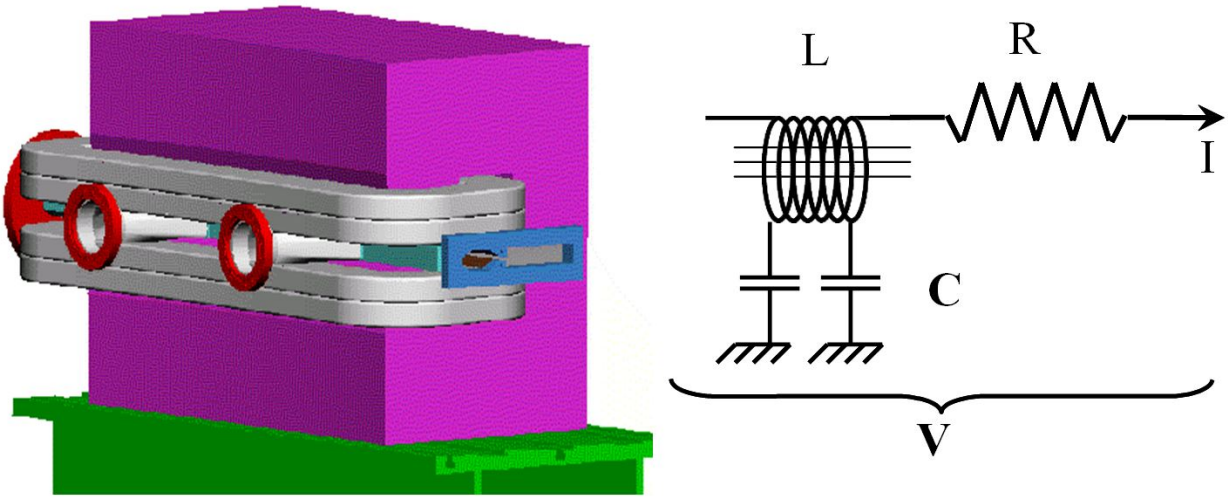

Fig. 7: A typical dipole bending magnet shown with its equivalent circuit

The symbols used in the equivalent circuit are defined below:

- magnet current, I;
- magnet voltage, V;
- series self-inductance, L;
- series resistance, R;
- distributed capacitance to earth, C.

Then:

- magnet voltage,
$$V = RI + L(\mathrm{d}I/\mathrm{d}t); \tag{8}$$
- instantaneous power,
$$VI = RI^2 + LI(\mathrm{d}I/\mathrm{d}t); \tag{9}$$
- stored energy,
$$E = \frac{1}{2}LI^2 \rightarrow \mathrm{dE}/\mathrm{d}t = LI(\mathrm{d}I/\mathrm{d}t); \tag{10}$$
- therefore power,
$$VI = RI^2 + \mathrm{d}E/\mathrm{d}t; \tag{11}$$

The first term in Eq. (11) will be recognized as the resistive loss in the magnet; the second is the rate of change of energy stored in the magnet as the field cycles between injection and peak field. This is referred to as ‘reactive power’, i.e., it represents a flow of energy which alternates between positive and negative values. The challenge of the cyclic power converter is to control this flow of energy and

provide the necessary storage system as significant quantities of energy circulate between the magnet and the power supply.

3.2 Categories of cycling systems

Before examining the various circuits and techniques which are used for power cycling accelerators, it is beneficial to consider the different regimes required for different accelerator applications.

Cycling systems can be categorized according to their repetition rates.

- Slow cycling: the term is usually applied to power systems with cycling time in the range
- 1 s to 10 s; a typical figure would be a cycle time of the order of 3 s. The supply systems for the largest proton accelerators generally fall into this category, as the energy stored in the long chain of electromagnets produces a large reactive power rating even at the low repetition rates.
- Medium cycling: with cycling time from 200 ms to 1 s, such systems have come to prominence more recently due to developments in power electronics which make this frequency range possible with full-waveform controlled circuits (as discussed in the following). They are typically used in separated-function electron accelerators where the lattice configuration eliminates the problem of beam anti-damping at high energy. The main added value is the possibility to use a single- or multi-shot strategy to optimize the stability of the main beam current.
- Fast cycling: corresponding to repetition rates of 10 to 50 Hz, these systems were used in the combined-function electron accelerators in the 1950s and 1960s where rapid acceleration times were needed to limit beam blow-up at high energy. They currently have applications in high-current medium-energy proton accelerators where the rapid cycling time provides intense fluxes of high-energy particles.

Three examples of these different types of accelerator requirements, with corresponding excitation and reactive power ratings, are now presented.

3.2.1 A slow-cycling system: the CERN Super Proton Synchrotron (SPS)

This 450 GeV, slow-cycling accelerator, used for high-energy particle physics, has undergone many modifications during its long life, and currently has a number of different operating modes. The presented data correspond to the 'fixed-target' mode, which demands the highest operational parameters. Details of the power system ratings are:

- peak proton energy 450 GeV;
- cycle time (fixed target) 8.94 s;
- peak current 5.75 kA;
- peak dI/dt 1.9 kA/s;
- magnet resistance 3.25 Ω;
- magnet inductance 6.6 H;
- magnet stored energy 109 MJ.

The waveforms corresponding to this mode of operation are shown in Figs. 8, 9 and 10.

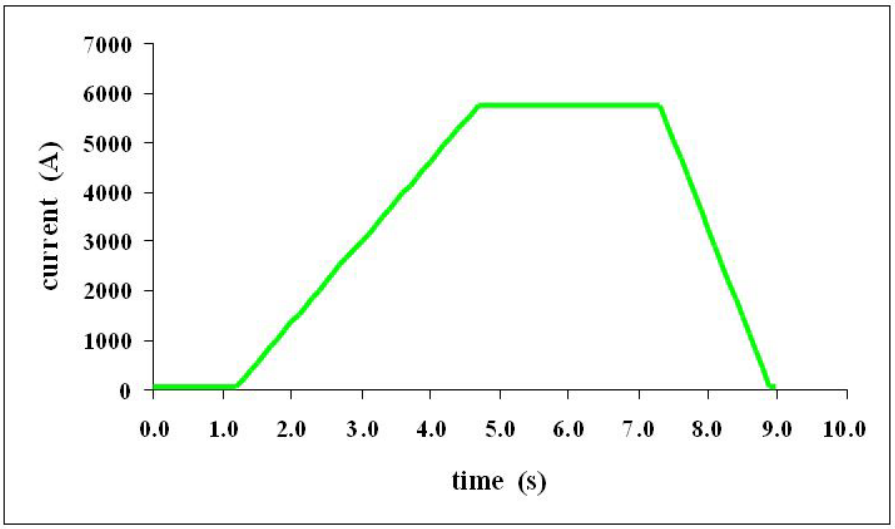

Fig. 8: Current waveform of the CERN SPS when operating in 'fixed-target' mode

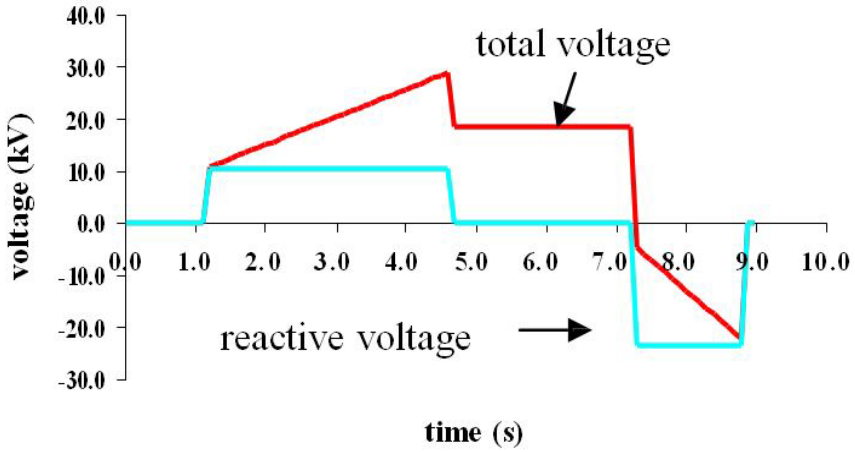

Fig. 9: Voltage waveforms of the CERN SPS corresponding to the current waveform of Fig. 8

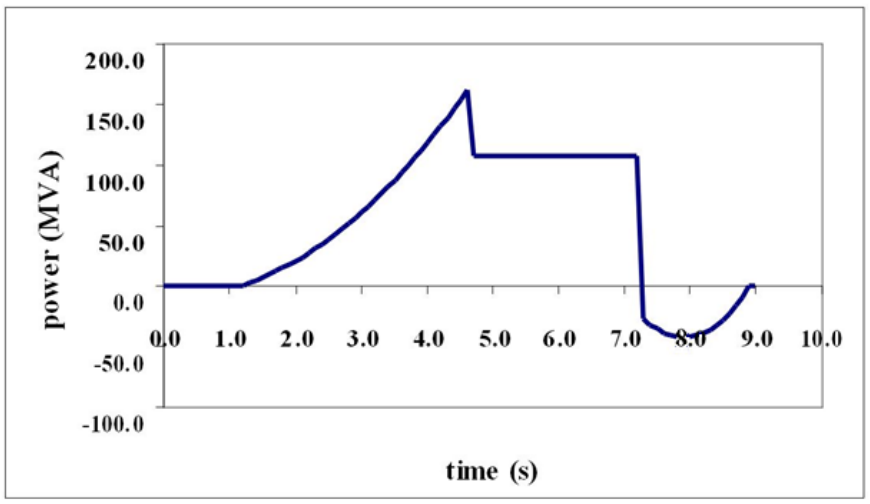

Fig. 10: Power waveform of the CERN SPS corresponding to the excitation levels shown in Figs. 8 and 9

It can be seen that the oscillation of energy between supply and load calls for forward voltages of 30 kV and reverse voltages of 20 kV. However, Fig. 9 demonstrates that the resistive voltage dominates during the acceleration and the flat-peak-field part of the cycle; reactive power is small compared to the resistive loss. Thus, the reverse power shown in Fig. 10 is small compared to the forward power in the earlier part of the cycle; however, the reverse power is still of the order of 50 MVA.

3.2.2 A fast-cycling system: the European Synchrotron Radiation Facility (ESRF) booster

The ESRF is a medium-sized electron storage ring which generates synchrotron radiation for a wide range of research applications; it has a full energy (6 GeV), 10 Hz (fast-cycling) booster synchrotron which accelerates electrons for injection into the main ring. The parameters of the booster's power system are as follows:

- peak electron energy 6.04 GeV;
- cycle time 100 ms;
- cycle frequency 10 Hz;
- peak dipole current 1467 A;
- magnet resistance 568 mΩ;
- magnet inductance 178 mH;
- magnet stored energy 191 kJ.

The power systems waveforms are shown in Figs. 11 and 12.

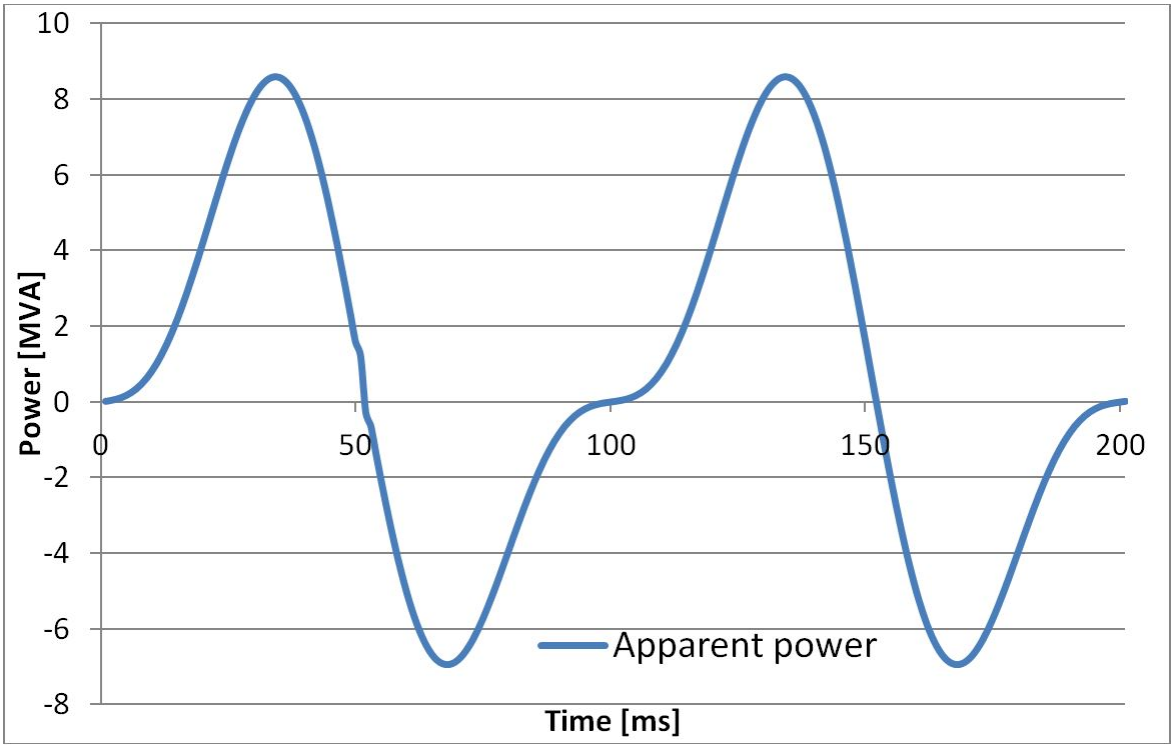

Fig. 11: Current waveform of the ESRF booster, and resistive and total voltage waveforms of the ESRF booster synchrotron.

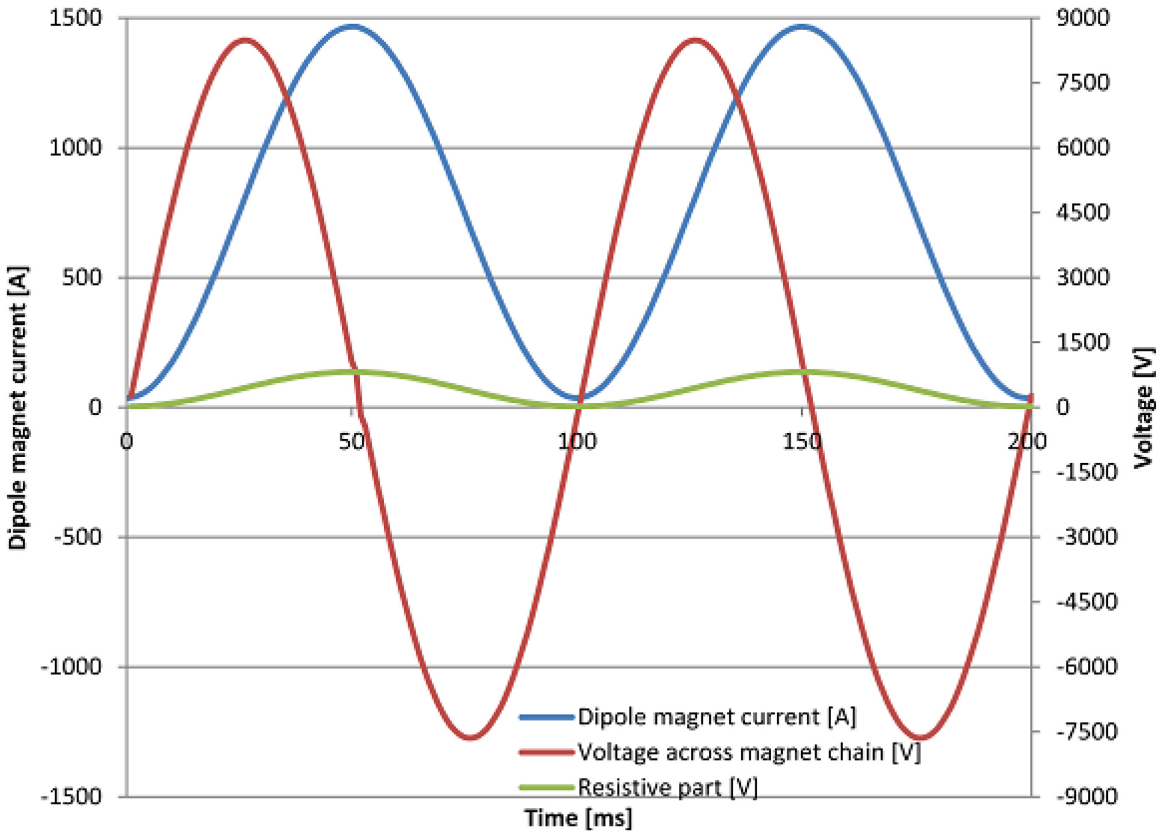

Fig. 12: Power waveform of the ESRF booster corresponding to the excitation levels shown in Fig. 11

It can be seen that the reactive voltage greatly exceeds the resistive voltage; the energy stored is more than an order of magnitude greater than the loss per cycle. Consequently, the power waveform is far more symmetrical about the time axis, compared to the SPS data, and energy storage is a vital feature of this power system's performance.

4 Cycling converter systems

Having examined the ratings of various cycling accelerators, it is now possible to discuss the nature of the power systems used to excite the magnet circuits. As the energy storage system is fundamental to the design, the various circuits can be categorized according to the elements used for this purpose. They fall into three categories:

- mechanical energy storage;
- inductive energy storage;
- capacitive energy storage.

When considering the circuits that need to be assembled around the central storage device, it is worthwhile emphasizing the basic requirements. The power converter system should:

- provide a unidirectional alternating waveform;
- provide accurate control of waveform amplitude;
- provide accurate control of waveform timing;
- provide storage of magnetic energy during low field for efficiency purposes;
- avoid disturbances on the neighbouring customers;

– if possible, provide waveform control to compensate for magnetic non-linearities;
– if needed (and possible), provide discontinuous operation for ‘top-up mode’.

4.1 Storing energy locally

One of the difficulties that influences the choice of the converter is to be as transparent to the supply network as possible. The large energy exchange with the public network is the potential cause of disturbances: this low-frequency perturbation is called the ‘flicker’.

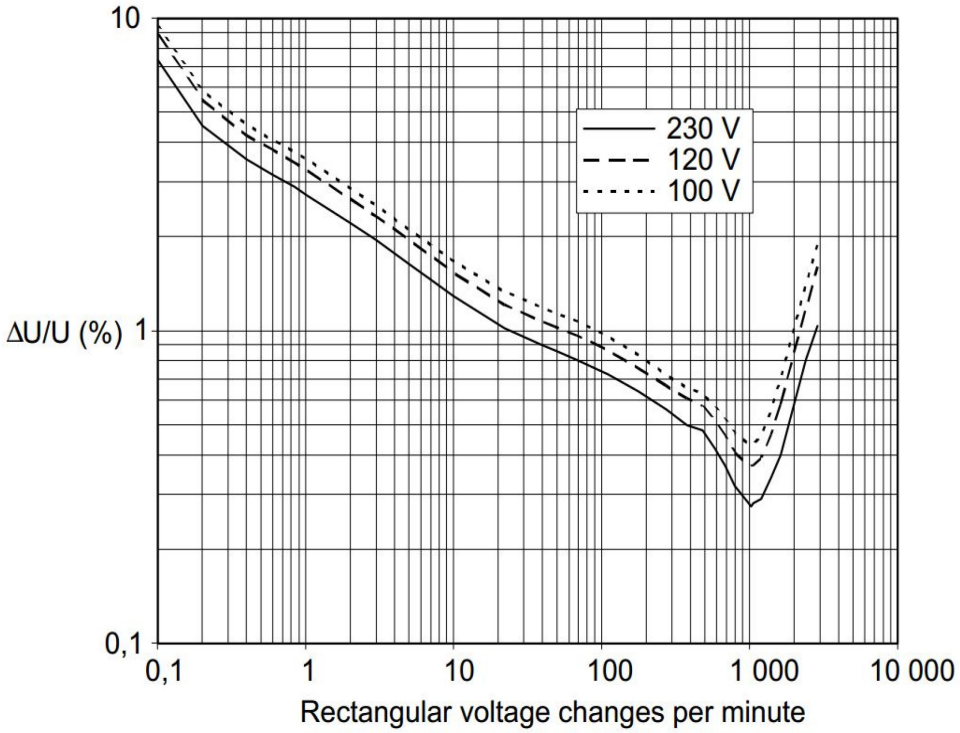

Fig 13: Curve of the maximum variation of supply voltage authorized on European networks. Note that two consecutive voltage changes (one positive and one negative) constitute one ‘cycle’, i.e., two voltage changes per second mean a 1 Hz fluctuation.

The worst case is at the bottom of the curve: 1200 voltage changes per minute yields 20 changes per second, and this is 10 Hz. The maximum tolerated value at 10 Hz is 0.29%, leading to a request for a public network rigidity 345 times higher than energy exchange. With the example of the ESRF booster dipole magnets, the power fluctuation of 15.5 MVA should produce less than 0.29% $\Delta U/U$ on the local network voltage. The current value at the ESRF on the 20 kV 50 Hz mains short-circuit power is 150 MVA. As a result, this power exchange will therefore produce more than 10% $\Delta U/U$ at 10 Hz. The maximum allowed is 0.29% × 150 MVA = 435 kVA for all systems including quadrupole and RF systems. Storage of magnetic energy during low field for flicker constraint is therefore mandatory to avoid disturbances on the neighbouring customers. The regional transport network at 225 kV–7 GVA short-circuit capacity allows 20 MVA power cycling at 10 Hz, which is just sufficient for the energy exchange requested at the ESRF.

4.2 Slow-cycling mechanical energy storage

These circuits were used to power and control the slow-cycling synchrotrons of the second half of the twentieth century. A diagram of a typical mechanical energy storage system is shown in Fig. 14.

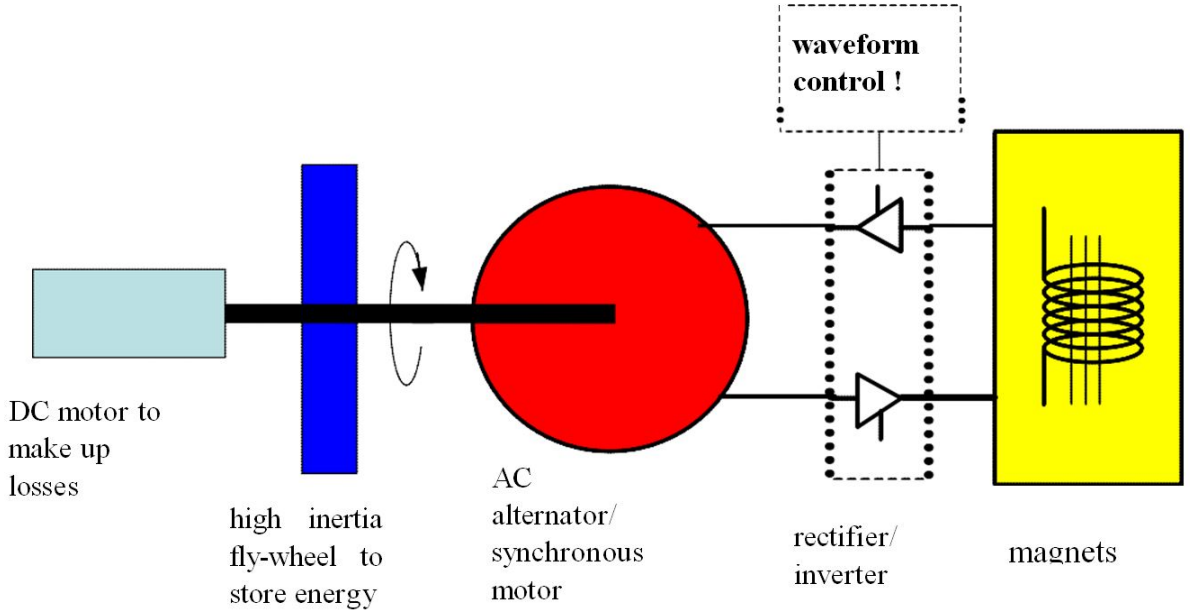

Fig. 14: Diagram of a typical mechanical energy storage system

The use of mechanical energy storage is only suitable for slow-cycling accelerators. Furthermore, the use of rotating machinery resulted in high capital and maintenance costs and, in some cases, the pulse duty caused faults in the alternators. In the later part of the twentieth century, the concept of mechanical storage was replaced by the use of direct connection to large very rigid national and international electrical supply grid systems using the large power plants' alternator inertia.

4.3 Slow-cycling direct connection

National supply networks have large, inductive stored energy. Given the correct interface, this can be utilized to provide and receive back the reactive power of a large accelerator.

Compliance with supply authority regulations must minimize:

- voltage flicker at the feeder with the curve indicated in Fig. 13;
- phase disturbances at the accelerator and neighbouring sites;
- frequency fluctuations over the entire network.

A very 'rigid' (i.e., high short-circuit capacity) high-voltage line into the accelerator equipment is necessary.

4.3.1 The magnet power supply system for the SPS (CERN)

A simplified diagram of this system is given in Fig. 15.

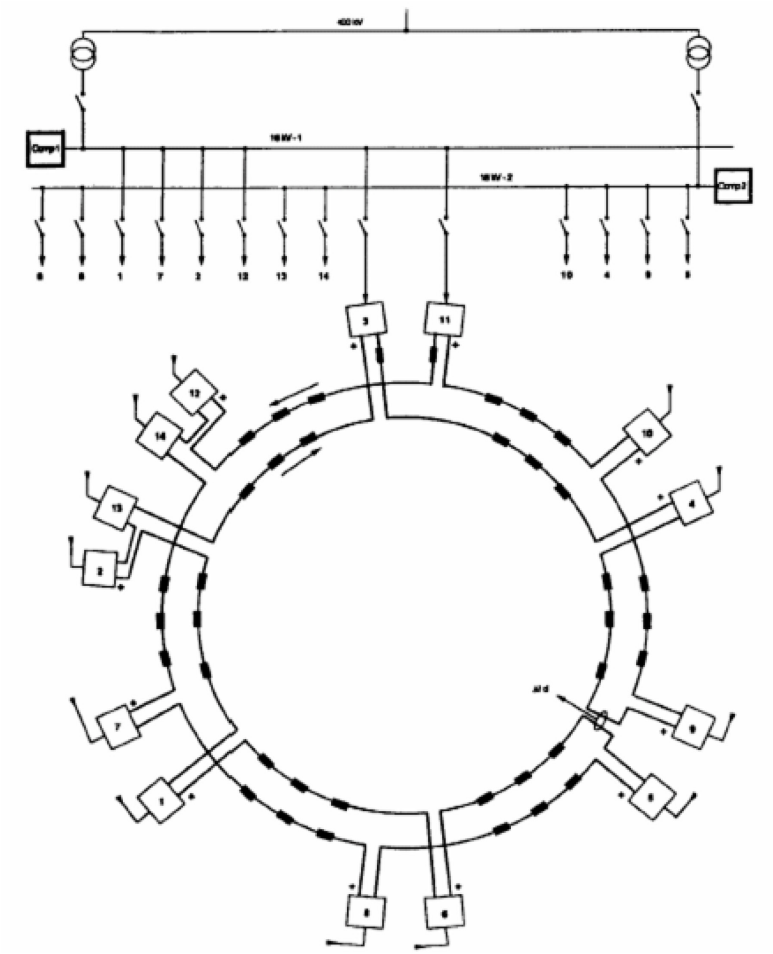

Fig. 15: The directly connected power supply system of the CERN SPS magnets

The diagram shows 14 converter modules, each comprising 2 sets of 12 pulse phase-controlled thyristor rectifiers. These are connected to the ring dipoles in series, with segments of the load located between successive power units; this prevents the required circuit voltage being applied in a single step. Each module is connected to its own 18 kV feeder, which is directly fed from the 400 kV French network.

As with the mechanical energy storage systems, the magnet current is controlled through phase-controlled rectifiers—solid-state thyristors in this case. Hence control of the magnet waveform, within the limitations of the converter's output voltage, is available.

Whilst the direct connection to the extensive and very rigid French grid provides an adequate source and sink of energy, compensation is necessary to prevent excessive phase swings at the CERN site. This is provided by a number of filters using saturable reactors, which are connected to the 18 kV line, as shown in Fig. 16 and also explained in Karsten Kahle's contribution in these proceedings.

This system represents significant capital savings compared to the earlier fly-wheel/alternator system. The maintenance costs and necessary downtime associated with rotating machines are reduced. This is therefore the preferred converter for large, slow-cycling accelerators; the CERN equipment has worked reliably and successfully since the commissioning of the SPS, and other particle physics laboratories have adopted this solution. However, it is strongly dependent on the energy storage characteristics of the local electrical network, on the availability of a very rigid high-voltage supply line, and on the agreement and co-operation of the electrical utility company, linked with rules for anti-flicker constraints.

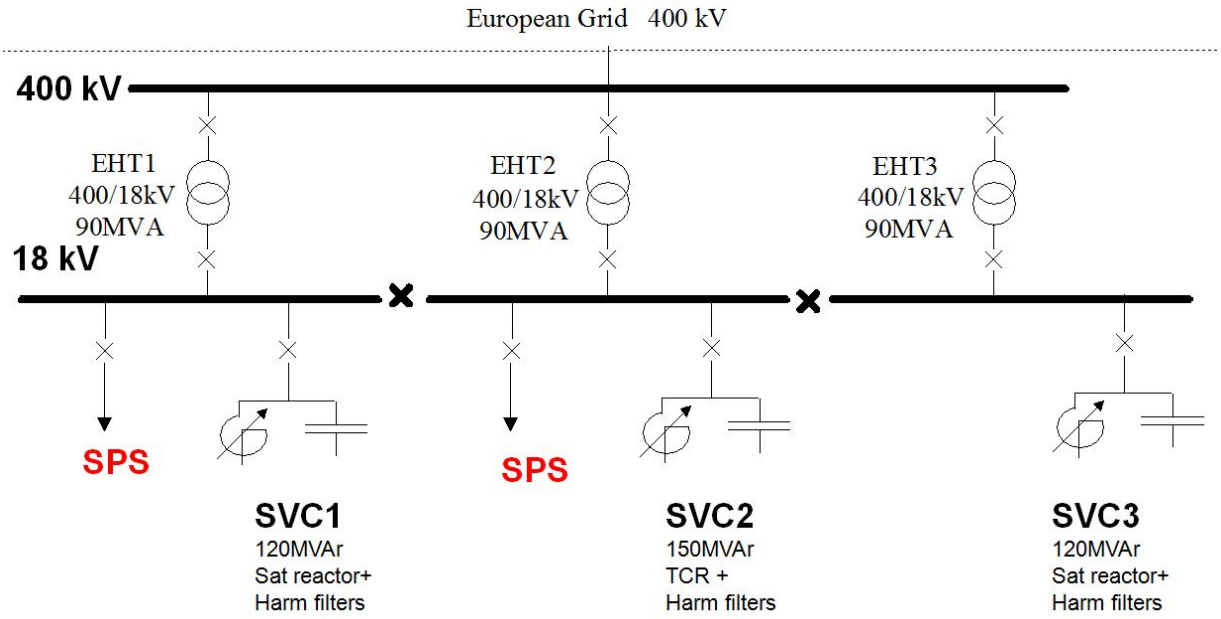

Fig. 16: Connection of filters using saturable reactors to the 18 kV feeder for the SPS magnet power supply system. The filters compensate for the inductive nature of the supply system and minimize phase swings that would otherwise occur, resulting from the power fluctuation during the acceleration and deceleration cycles.

4.4 Medium- and fast-cycling inductive storage systems

Neither mechanical storage nor direct connection is suitable for systems with cycling frequencies much above 1 Hz. Hence the fast- and medium-cycling accelerators (mainly electron synchrotrons) developed in the 1960s and 1970s used inductive energy storage. At that time inductive storage was roughly half the cost per kJ of capacitive energy storage, though this situation changed towards the end of the twentieth century (see the following). The 'standard circuit' was developed originally at the Princeton-Pen accelerator and was named the 'White circuit' after that laboratory's director, Professor Milton White.

4.4.1 The singe-cell White circuit

In its simplest form, the White circuit comprises a complete series string of the accelerator magnets, connected into a parallel network of resonating capacitors and an energy storage inductor. A diagram of such a circuit is given in Fig. 17.

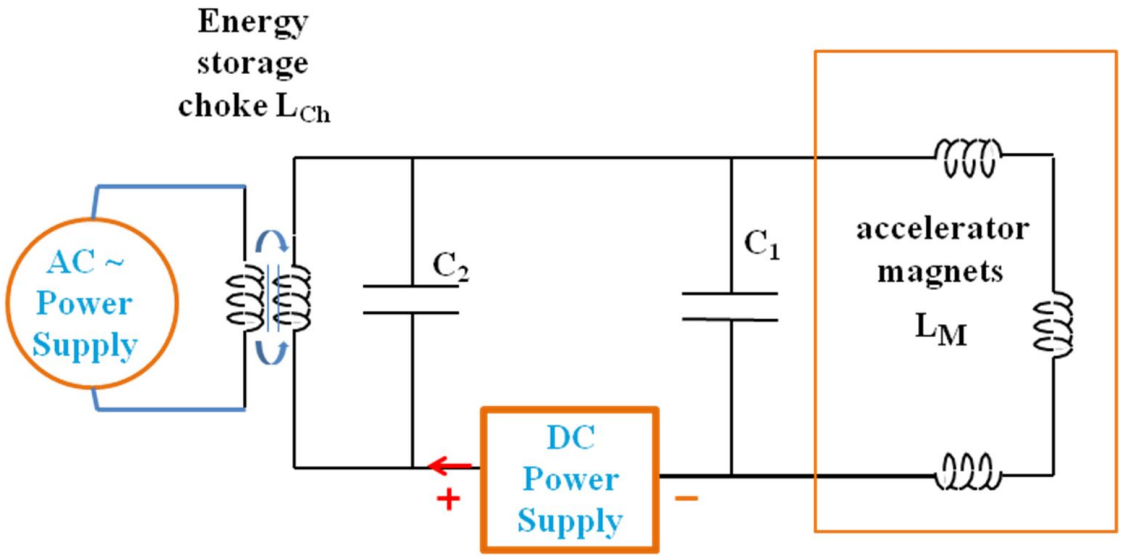

Fig. 17: Schematic diagram of a single-cell 'White circuit'

The series-connected accelerator magnets are resonated at the cycling frequency by capacitance C_1. In parallel with this circuit is another resonant system comprising an inductor, referred to as the 'energy storage choke' and the resonating capacitor C_2. The d.c. converter which generates the direct current required to bias the alternating sine wave is located between these two parallel circuits; providing the two circuits are correctly resonated, there will only be a small alternating current flowing through this rectifier set. The a.c. excitation is provided by an inverter supply powering the parallel circuits by means of a further winding on the inductor, which is closely coupled to the main inductive winding. Again, providing the resonant tunes are correct, the a.c. supply sees a resistive load and, of course, sees no direct current. Consequently, the basic feature of the system is to connect the magnets to two separate supplies—one d.c. and one a.c.—that do not interfere with each other, that are orthogonal in their control functions, and that, together, generate a fully biased sine wave in the accelerator magnets.

These features of the circuit are summarized as follows:

- magnets are all in series—this ensures field uniformity around the accelerator;
- circuit oscillation frequency given by ω;
- C_1 resonates magnet in parallel:
$$C_1 = \omega^2 / L_{\mathrm{M}} C_1; \tag{12}$$
- C_2 resonates energy storage choke:
$$C_2 = \omega^2 / L_{\mathrm{Ch}}; \tag{13}$$
- the energy storage choke has a primary winding which is closely coupled to the main winding;
- only small a.c. is present in the d.c. source;
- no d.c. is present in the a.c. source;
- the waveform control is very limited to a few per cent of adjustment to compensate saturation effects. This will not be developed here.

A diagram of the current waveform is given in Fig. 18; this defines the parameters used in the following section.

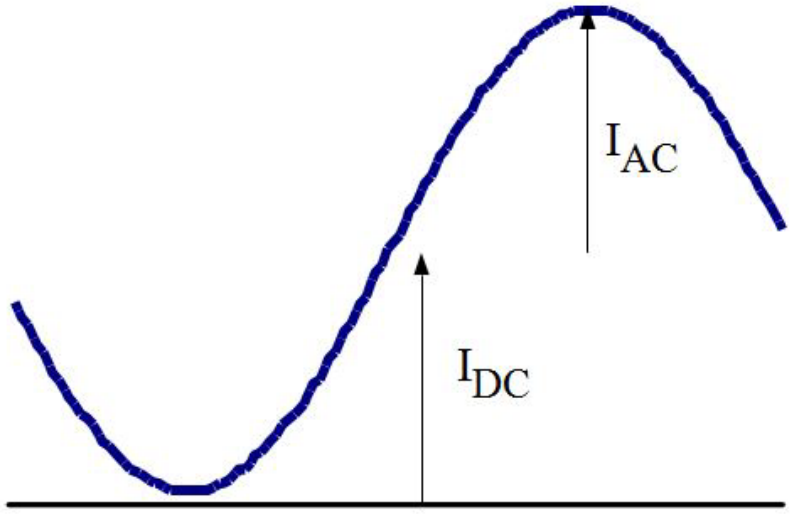

Fig. 18: Diagram of the current waveform generated in the accelerator magnets by the 'White circuit'

The equations corresponding to this circuit are as follows:

– magnet current,

$$I_{\mathrm{M}} = I_{\mathrm{dc}} + I_{\mathrm{ac}} \cdot \sin(\omega t); \tag{14}$$

– magnet voltage,

$$V_{\mathrm{M}} = R_{\mathrm{M}} I_{\mathrm{M}} + \omega I_{\mathrm{M}} L_{\mathrm{M}} \cdot \cos(\omega t); \tag{15}$$

– choke inductance,

$$L_{\mathrm{Ch}} = \alpha L_{\mathrm{M}} \ (\alpha \text{ is determined by inductor/capacitor economics}); \tag{16}$$

– choke current,

$$I_{\mathrm{Ch}} = I_{\mathrm{dc}} - (1/\alpha) I_{\mathrm{ac}} \cdot \sin \omega t; \tag{17}$$

– peak magnet energy,

$$E_{\mathrm{M}} = (1/2) L_M \cdot (I_{\mathrm{dc}} + I_{\mathrm{ac}})^2; \tag{18}$$

– peak choke energy,

$$E_{\mathrm{Ch}} = (1/2\alpha) L_{\mathrm{M}} \cdot (I_{\mathrm{dc}} + I_{\mathrm{ac}}/\alpha)^2; \tag{19}$$

– typical values:

$$I_{\mathrm{dc}} \sim I_{\mathrm{ac}};\ \alpha \sim 2. \tag{20}$$

Then,

$$E_{\mathrm{M}} \sim 2 L_{\mathrm{M}} (I_{\mathrm{dc}})^2; \tag{21}$$

$$E_{\mathrm{Ch}} \sim 9/4\, L_{\mathrm{M}} (I_{\mathrm{dc}})^2. \tag{22}$$

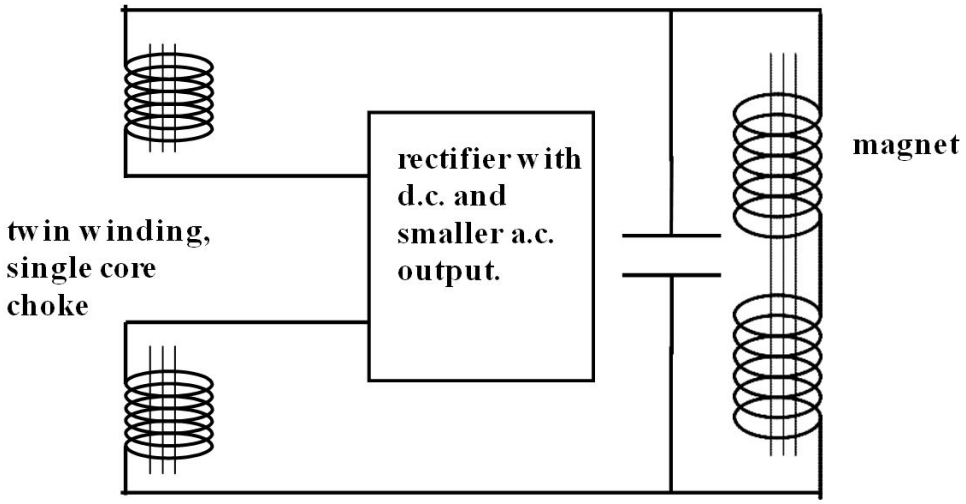

Fig. 19: Modified version of the single-cell White circuit which utilizes a single power source to generate both alternating and direct currents in the magnet.

4.4.2 The multi-cell distributed White circuit

The single-cell White circuit has all magnets series connected and resonated by a capacitor bank, the complete magnet voltage appearing across this single parallel circuit. For large fast-cycling accelerators, where the magnet alternating voltage significantly exceeds 10 kV, it is necessary to divide the White circuit into a number of separate cells, which are series connected, with a capacitor/choke parallel circuit separating each cell. Such an arrangement is shown in Fig. 20.

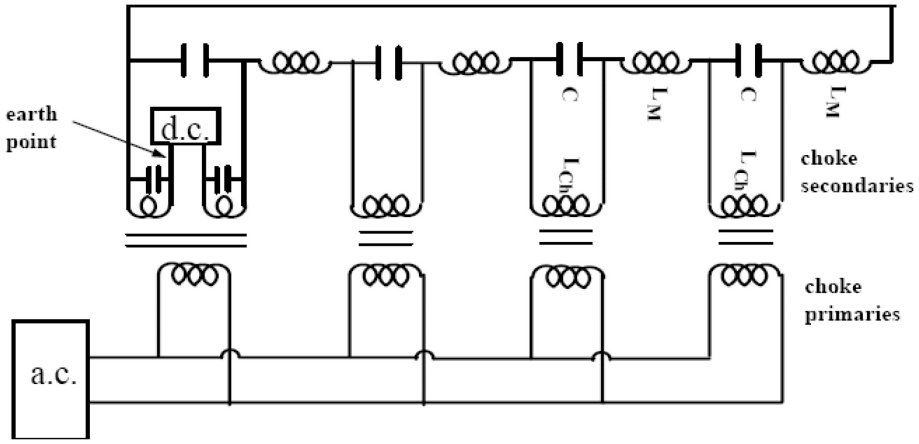

Fig. 20: The distributed White circuit arrangement, as required when the magnet series alternating voltage would be excessively high across a single cell; the example shown is a four-cell circuit.

The nomenclature used in Fig. 20 is as defined in Section 4.3.1, with the magnets identified as L_M. It can be seen that these are still series connected to ensure current continuity. The diagram is for a four-cell system but, in principle, the circuit can be assembled with any number of cells as required to limit the voltages to earth (see the following).

The energy storage choke is now divided into a number of separate secondary windings, each closely coupled to a corresponding primary. One secondary winding is further divided into two, with the source of the d.c. bias located at this point, which is also made the single firm earth point in the network. The capacitance in the circuit is also segmented, with a bank connected in parallel with each secondary; each bank combines the magnet and choke capacitances (C_1 and C_2 of Fig. 17). At the split secondary, the capacitances that resonate the choke in parallel and the magnets in series are separated. With these provisos, the equations of Section 4.3.1 for the single-cell circuit are equally valid for this circuit.

The primary windings are all connected in parallel; this prevents unwanted 'spurious modes of resonance' which can occur when multiple resonant systems are coupled. With primary windings absent, a four-cell secondary network has spurious resonances which are the four eigenvalues ω_n predicted by the following equation:

$$\begin{pmatrix}1\\1\\1\\1\end{pmatrix} - \omega_n^2 L_{\mathrm{Ch}} \begin{pmatrix} K_{1,1} & K_{1,2} & K_{1,3} & K_{1,4} \\ K_{2,1} & K_{2,2} & K_{2,3} & K_{2,4} \\ K_{3,1} & K_{3,2} & K_{3,3} & K_{3,4} \\ K_{4,1} & K_{4,2} & K_{4,3} & K_{4,4} \end{pmatrix} \begin{pmatrix} C_1 & 0 & 0 & 0 \\ 0 & C_2 & 0 & 0 \\ 0 & 0 & C_3 & 0 \\ 0 & 0 & 0 & C_4 \end{pmatrix} = 0 \qquad (23)$$

where

- K_{nm} are coupling coefficients between choke windings n, m;
- C_n is capacitance n;
- L_{Ch} is self-inductance of each secondary;
- ω_n are the frequencies of spurious modes.

The spurious modes do not induce magnet currents but can represent a serious energy loss mechanism in the circuit; hence, the use of closely coupled parallel-connected choke primaries is strongly advisable.

The use of paralleled primaries also ensures that the voltages across each section are equalized—an arrangement that prevents the alternating currents *at the fundamental frequency of oscillation* that pass through stray capacitances to earth resulting in dissimilarity of magnet current around the network. Given this equalization of voltage across each section, the voltage distribution to earth

along the magnet and choke secondary circuit is as shown in Fig. 21 (for clarity, the primary windings are not shown). It can be seen that the multi-cell arrangement prevents the magnet voltages accumulating to a level that would provide difficulty with coil and bus-bar insulation.

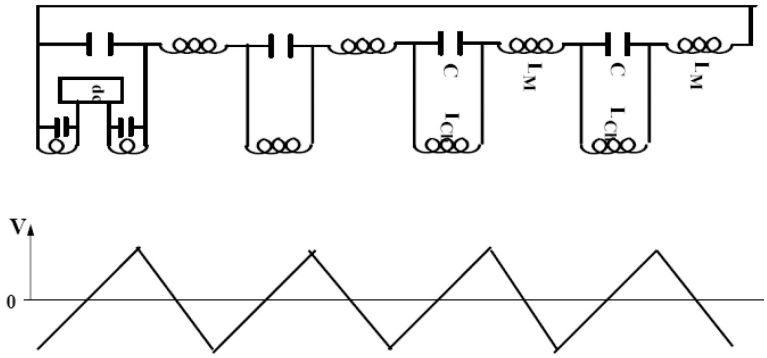

Fig. 21: Voltage distribution to earth in the secondary circuit of the multi-cell White circuit

The principle features of an *n*-cell White circuit are summarized as follows:

- the magnets are still in series for current continuity and equity;
- the voltage across each section is only 1/*n* of the total magnet voltage;
- the maximum voltage to earth is only 1/2*n* of the total;
- the choke has to be split into *n* separate windings;
- the d.c. supply is at the centre of one split secondary winding—this is the circuit's firm earth point;
- the a.c. is connected through a paralleled primary;
- the paralleled primary must be close coupled to the secondary to balance voltages in the circuit;
- there is *no* waveform control.

An example is shown in Fig. 22.

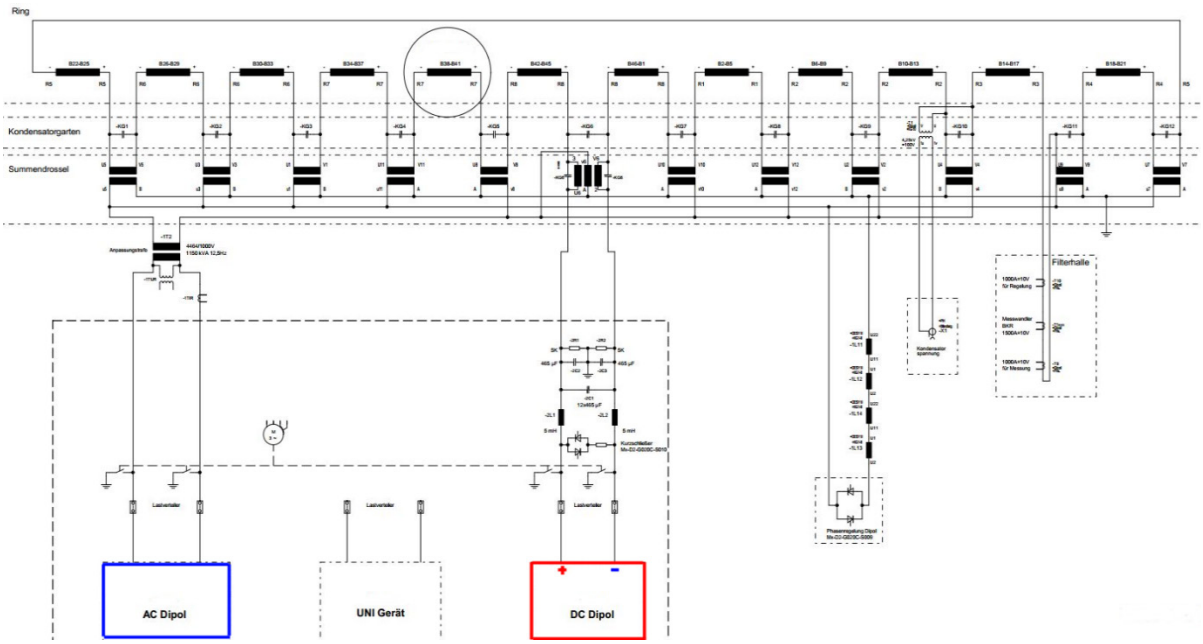

Fig. 22: Desy 12.5 Hz booster synchrotron example

4.5 Modern capacitive energy storage systems with switch-mode control

Technical and economic developments in electrolytic capacitor manufacturing now result in capacitive energy storage being of lower cost than inductive energy storage (providing voltage reversal is not required). Additionally, semiconductor technology now allows the use of fully controlled devices (Insulated Gate Bi-polar Transistors—IGBTs) giving waveform control at medium current and voltages, using the 'switch mode' principle. Medium-sized synchrotrons with cycling times of 1–5 Hz can now take advantage of these developments for cheaper and dynamically controllable power magnet converters, with waveform control available, within the limits of the current and voltage ratings. This innovation was pioneered by Irminger, Horvat, Jenni and Boksberger at the Swiss Light Source (SLS); the *single line equivalent* circuit that they developed to power the 3 Hz booster synchrotron is shown in Fig. 23.

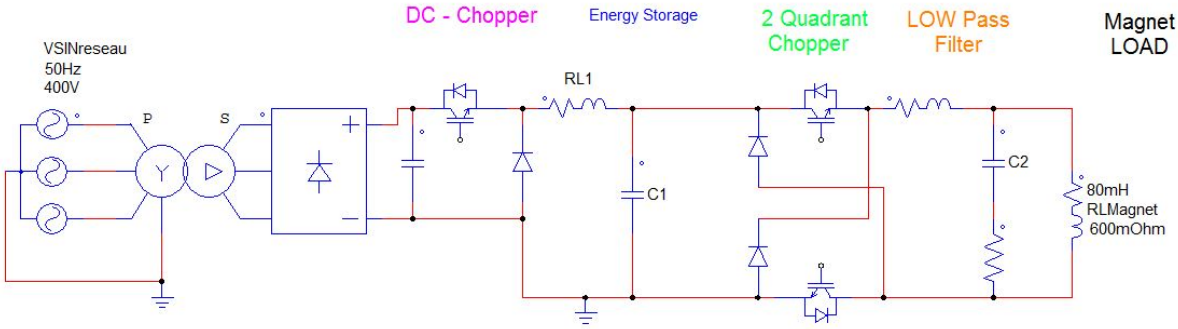

Fig. 23: Controlled capacitive energy storage system developed for the SLS

The accelerator magnets (identified as LOAD in Fig. 23) are series connected and are fed in reality by two power converter circuits, each comprising:

- a d.c. power source;
- a d.c. chopper, which controls the flow of energy to make up the system losses;
- the main energy storage capacitor;
- a high-frequency 'switch-mode' chopper circuit which is capable of transferring energy into the magnet, allowing the load to 'free-wheel' in a passive state or inverting the energy flow and recharging the capacitor from the energy stored in the magnet;
- a number of low-pass filters, which smooth out the chopping ripple and deliver the low-frequency voltage waveform to the magnet.

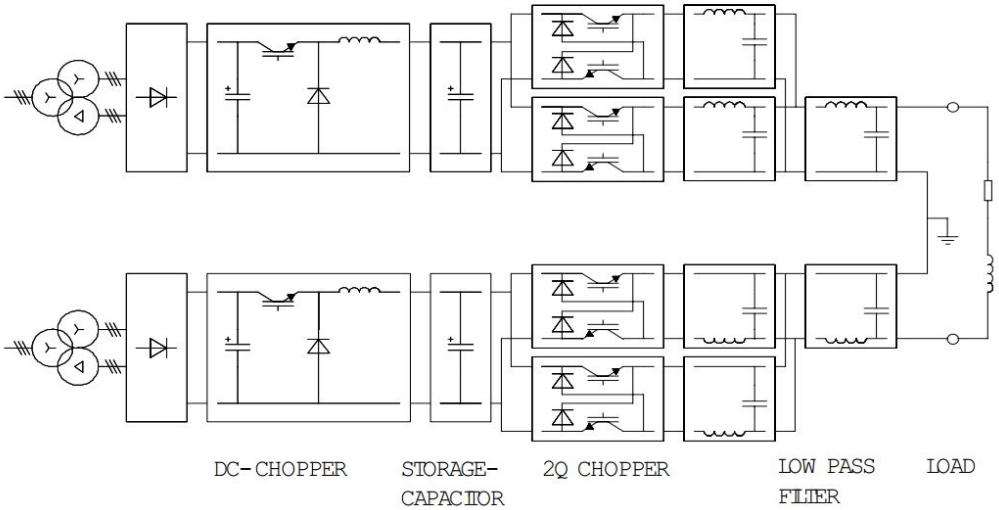

Fig 24: Real power circuit diagram

Each power unit carries half the current, i.e. 475 A and half the voltage, i.e., 500 V. The basic parameters of the SLS booster installation are given in Table 2.

Table 2: Parameters of the SLS booster synchrotron power supply system

Combined-function dipoles	48 BD; 45 BF
Resistance	600 mΩ
Inductance	80 mH
Maximum current	950 A
Stored energy	28 kJ
Cycling frequency	3.1 Hz

The waveforms associated with this circuit are shown in Fig. 25 (magnet current and voltage), Fig. 26 (total power into the magnet) and Fig. 27 (capacitor voltage and input current).

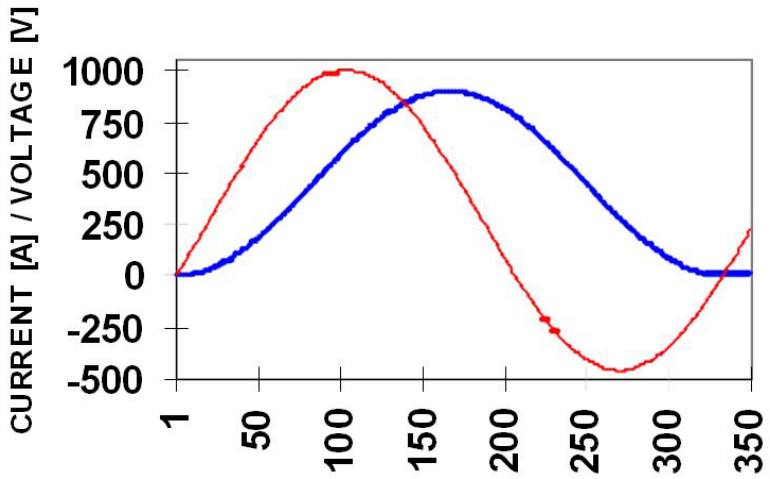

Fig. 25: Magnet current and voltage vs time (ms) in the SLS booster capacitive energy storage power supply system.

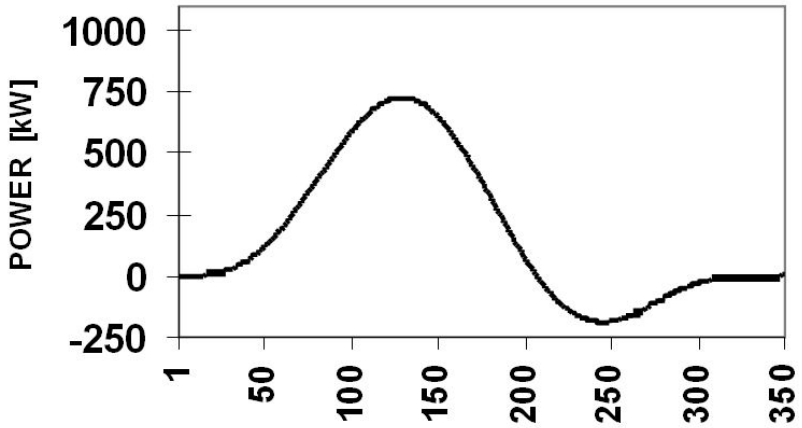

Fig. 26: Magnet power vs time (ms) in the SLS booster capacitive energy storage power supply system

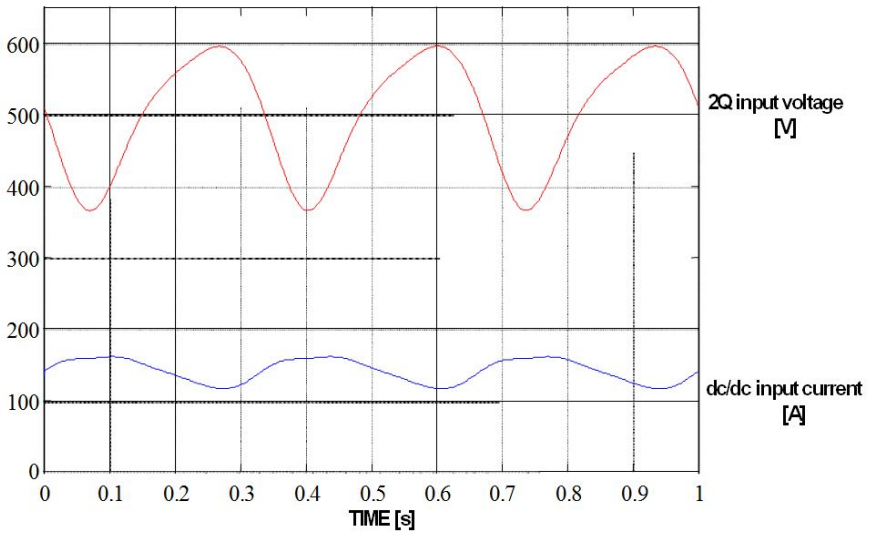

Fig. 27: Capacitor voltage and input current vs time in the SLS booster capacitive energy storage power supply system.

It should be noted that it is the development of the power IGBT that allows this switch-mode circuit to control the magnet waveform. The switching of the high-frequency chopper controls both the direction and the rate of flow of energy between the capacitor and the magnet, and this is only possible in the frequency domain of a few hertz with the use of the power semiconductors, which can switch on and off whilst conducting currents of the order of hundreds of amperes.

It is instructive to contrast this relatively new solution to powering a cycling synchrotron with the older White circuit:

– the switch-mode circuit does not need a costly energy storage choke with increased power losses;

– within limits of rated current and voltage, the switch-mode circuit provides flexibility of output waveform;

– after switch-on, the switch-mode circuit requires less than 1 s to stabilize (valuable in ‘top-up mode’).

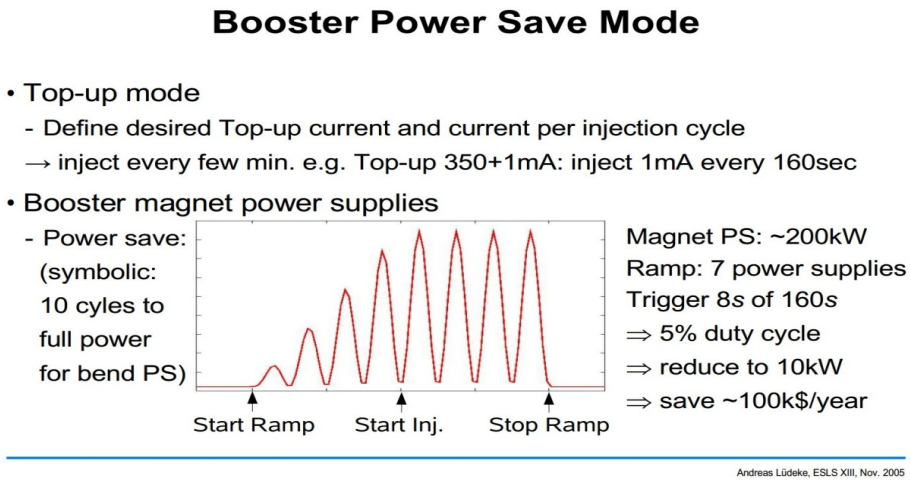

Fig. 28: An example from the SLS of the booster power save mode

The example shown in Fig. 28 from the SLS indicates an increase in efficiency of the injector of such an equipped machine. However, the current and voltages possible in switched circuits are currently restricted by component ratings. The power stress of the silicon die at a few hertz is the major difficulty to overcome for such power converters.

The booster synchrotrons of the next generation of light sources (Soleil, Diamond) are using this circuit, with component ratings now adequate to power the 3 GeV, 5 Hz booster for Diamond. However, the use of such a circuit for a 50 Hz fast-cycling accelerator is still some way off, and capacitor and IGBT voltage ratings will need to rise by approximately an order of magnitude before this becomes realistic.

5 Case of slow-cycling Pulse Width Modulation (PWM) with integrated capacitive storage

The CERN power converter for the Proton Synchrotron (PS) accelerator was powered by a rotating machine sized to 90 MVA. This system, described by Fig. 29, enables an acceptable energy exchange between magnets and mechanical storage to avoid exchange with the public network.

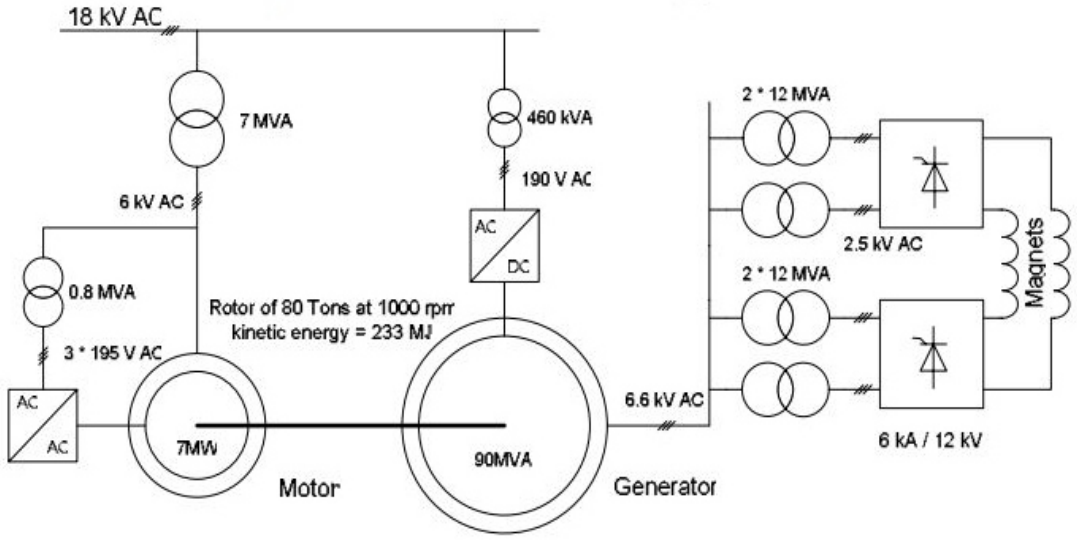

Fig. 29: Single line diagram of the 90 MVA electro kinetic system powering the PS at CERN

The basic data for the magnet are as follows: ±10 kV, 6 kA, 2.4 s pulse see Fig. 30

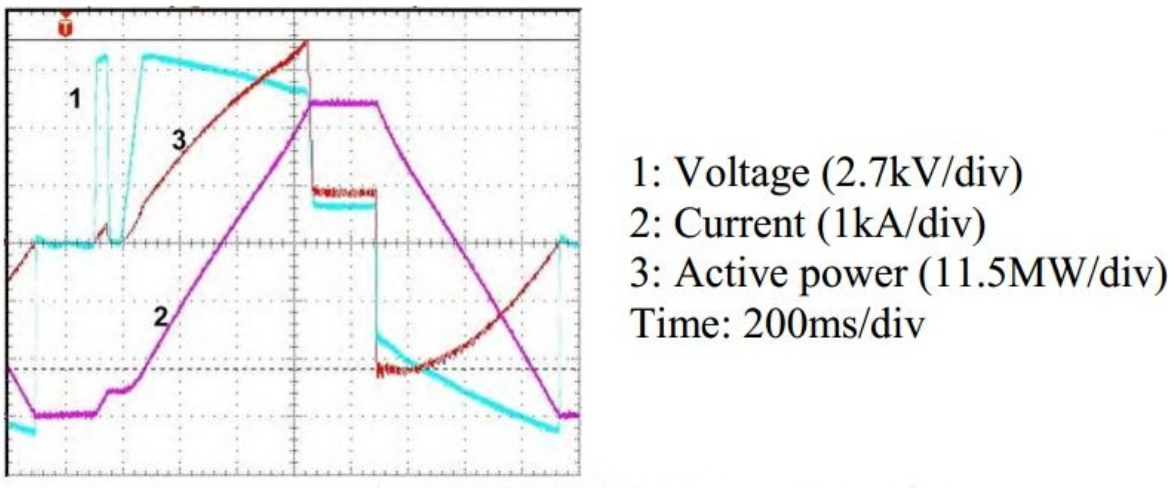

Fig. 30: Typical electrical waveform of the CERN PS accelerator magnets

In 2007 the mechanical storage was replaced by capacitive storage. Figure 31 is a global view of the single line diagram of such a system.

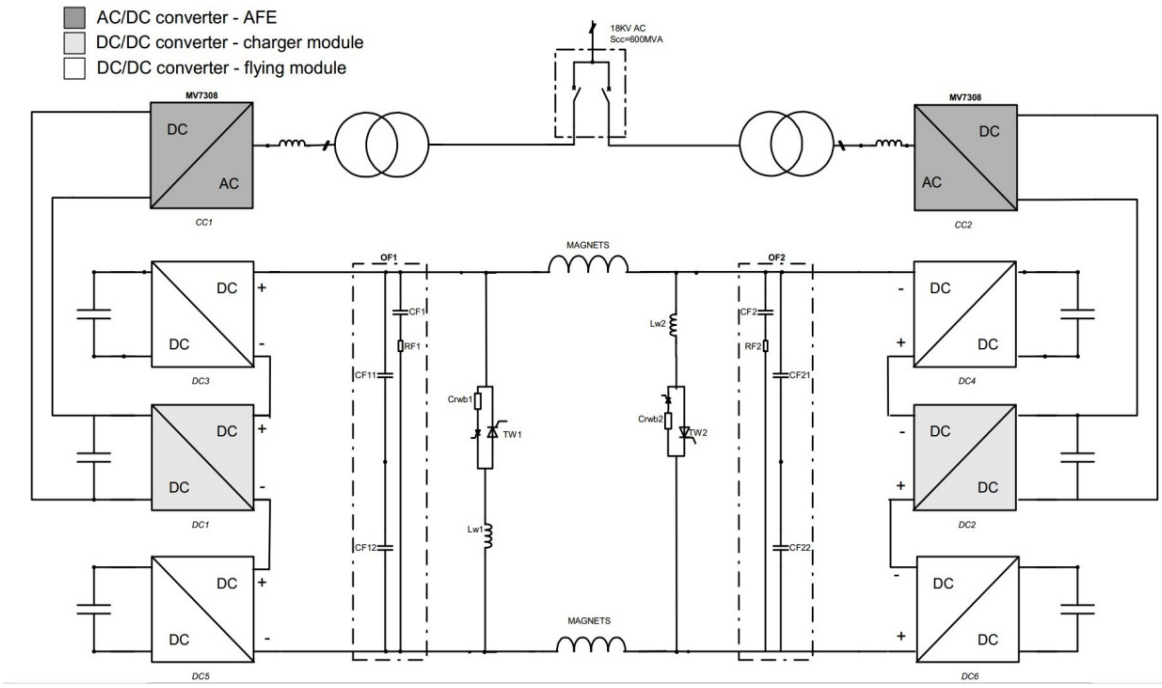

Fig 31: General view of the single line diagram of POPS

Each leg is based on three parallel neutral clamped legs allowing the production of three voltage levels to the output: (+VDC/2, 0, –VDC/2). The six capacitor banks are located in containers (40 ft shelters). Each of them contains 126 units parallel connected for a total value of 0.25 F, 5 kV. The 3 MJ of energy stored can vary from 5 kV to 2 kV, giving 2.5 MJ usable energy exchange. Six capacitor banks in total give 15 MJ of energy available to exchange with the magnet chain. The diagrams of Fig. 32 show the main current and voltage of such a system.

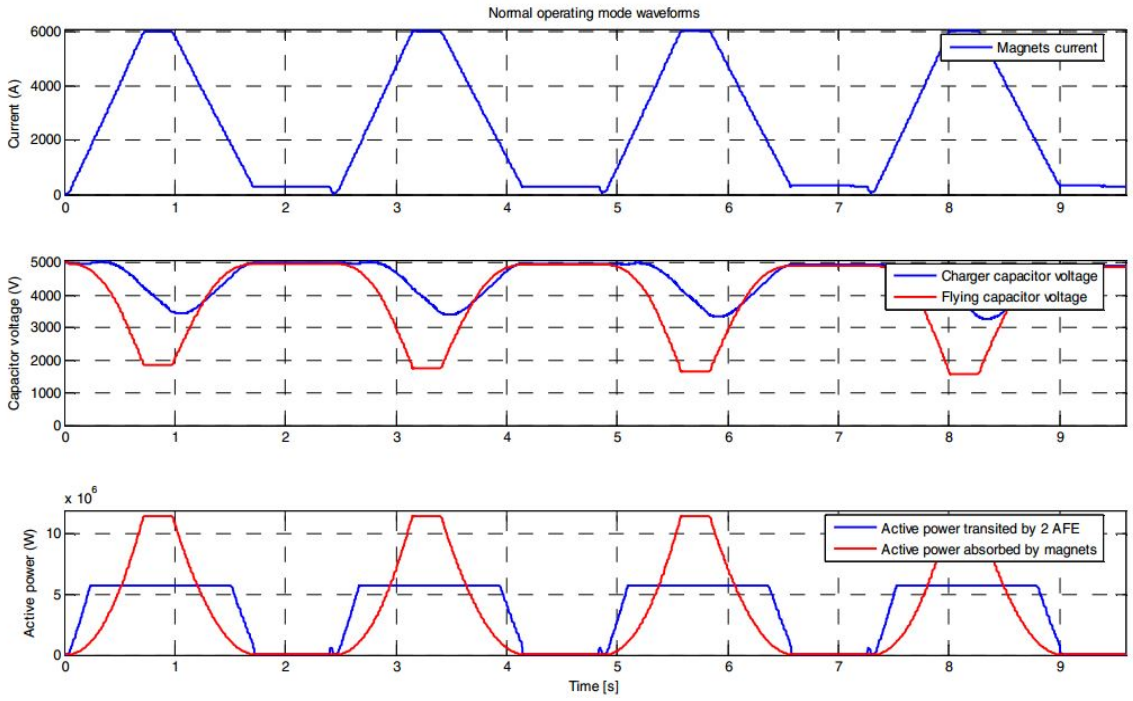

Fig. 32: Main current and voltage diagram of the magnet and capacitor storage elements

6 Conclusion

The power converters are a vital part of a cycling accelerator, and the operational efficiency and susceptibility of the machine to parameter drift are dependent on the stability and accuracy of the converters and whether their waveform can be adjusted to match the beam requirements during acceleration. It is therefore important that the engineers designing and operating the converters are in close collaboration and communication with the magnet designers and those defining the lattice and predicting the beam behaviour. In this way the most suitable circuit will be chosen and the optimum performance obtained.

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Radio Frequency Solid State Amplifiers

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Abstract
Solid state amplifiers are being increasingly used instead of electronic vacuum tubes to feed accelerating cavities with radio frequency power in the 100 kW range. Power is obtained from the combination of hundreds of transistor amplifier modules. This paper summarizes a one hour lecture on solid state amplifiers for accelerator applications.

Keywords
Radio-frequency; RF power; RF amplifier; solid state amplifier; RF power combiner, cavity combiner.

1 Introduction

The aim of this lecture was to introduce some important developments made in the generation of high radio frequency (RF) power by combining the power from hundreds of transistor amplifier modules. Such RF solid state amplifiers (SSA) were developed and implemented at a large scale at SOLEIL to feed the booster and storage ring cavities [1, 2]. At ELBE FEL four 1.3 GHz–10 kW klystrons have been replaced with four pairs of 10 kW SSAs from Bruker Corporation (now Sigmaphi Electronics, Haguenau/France), thereby doubling the available power [3]. The company Cryolectra GmbH (Wuppertal/Germany) delivers SSA solutions at various frequencies and power levels, such as a 72 MHz–150 kW SSA for a medical cyclotron [4].

Following a transfer of technology from SOLEIL, the company ELTA (Blagnac/France), a subsidiary of the French group AREVA, has delivered seven 352.2 MHz–150 kW RF SSAs to ESRF [5, 6]. These SSAs are used as an example to illustrate this technology. A compact SSA making use of a cavity combiner with fully planar RF amplifier modules that are suited for mass production is under development at ESRF: the aim is to reduce the required space and fabrication costs[1].

1.1 Typical radio frequency system layout

The typical layout of an RF transmitter powering an accelerating cavity in a particle accelerator is shown in Fig. 1. The low-level RF signal generated by the master source is distributed to all RF stations and other equipment such as, for example, the beam diagnostics systems. It is modulated in amplitude and phase by the low-level RF (LLRF) system, pre-amplified and amplified to high power by means of an RF power amplifier, which is the subject of this paper.

RF power amplifiers are often protected against reverse power by an isolator built with an RF power circulator that transmits the incident power to the accelerating cavity and deviates the reverse power into a high power load. The RF transmitter generally includes various auxiliaries, a power supply, a modulator, and fast interlock protection systems.

[1] This development has received funding from the EU as work package WP7 in the frame of the FP7/ESFRI/CRIPS project

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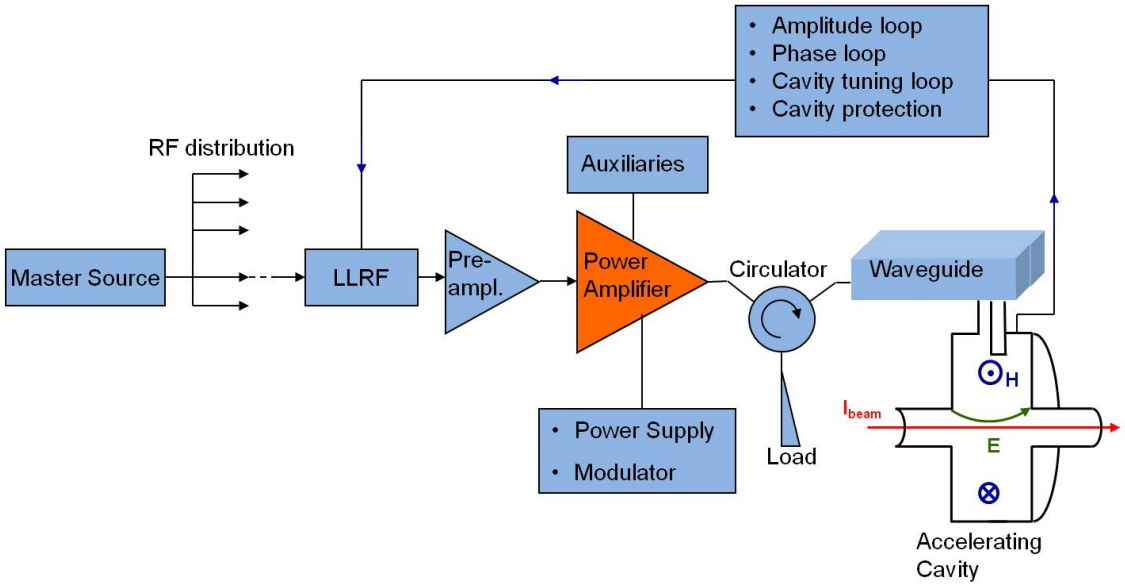
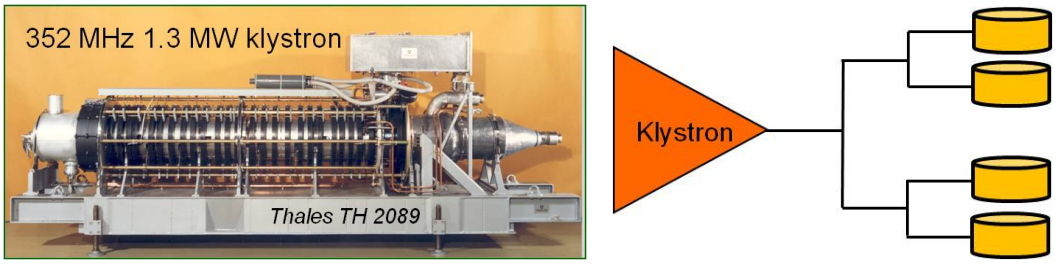


Fig. 1: RF transmitter for an accelerating cavity

1.2 Example: the ESRF transmitters

The 1.3 MW 352.2 MHz super klystron from Thales Electron Devices (TED, Vélizy/France) in Fig. 2(a) was initially developed for the CERN/LEP ring. Similar klystrons are or were manufactured by other tube manufacturers. Four transmitters using this type of klystron were implemented at ESRF in the 1990s: one to deliver 600 kW in 10 Hz pulses to the booster cavities, and three others to power the storage ring cavities in a continuous wave (CW). As shown in Fig. 2(b), the power from these klystrons needs to be split to feed two to four cavities with several hundred kilowatts each.



(a) (b)

Fig. 2: (a) 1.3 MW klystron from Thales Electron Devices (TED, Vélizy/France) used at ESRF. DC to RF efficiency $\eta_{max} = 62\%$, gain $G_{max} = 42$ dB. (b) Power splitting to provide several hundreds of kilowatts of RF to a number of ESRF cavities.

These klystron tubes have a high gain and a good efficiency. They are fed from 100 kV, 20 A DC high voltage power supplies with a sophisticated crowbar protection. In modern systems, fast insulated-gate bipolar transistor (IGBT) switched power supplies are used. Klystrons require many auxiliary power supplies for the modulation anode, the filament, and the focusing coils. Due to the high voltage, the electrons generate a substantial level of high energy X-rays when hitting the collector, which necessitates a sophisticated lead shielding hutch.

Out of the original three manufacturers, only one still produces the ESRF klystron shown in Fig. 2(a), and in the early 2000s there remained only a few customers. Seeing the potential risk of obsolescence of these klystrons, it was necessary to become prepared for an alternative RF power source in order to safeguard the operation of the facility. Following SOLEIL's great success with the development and operation of 180 kW SSAs [1] it was decided to implement an initial series of seven SSAs in the frame of the ESRF upgrade phase I over the years 2009 to 2015. Figure 3 shows one of the

seven new 150 kW SSAs at ESRF. Four SSAs have replaced the booster klystron transmitter, and each of the three remaining SSAs feeds one new Higher Order Mode (HOM) damped cavity in the ESRF storage ring [5, 6].

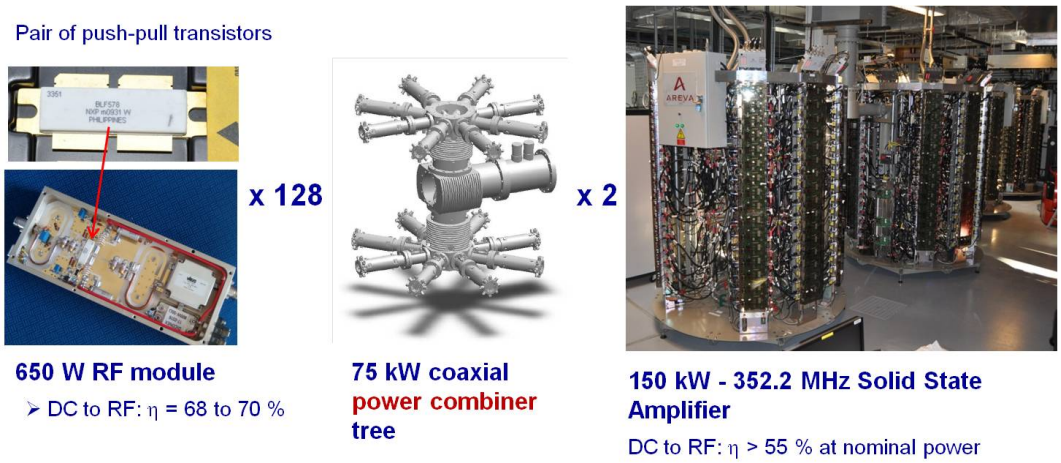


Fig. 3: One of the 150 kW–352.2 MHz solid state amplifiers obtained by combining the power of 256 RF transistor amplifier modules each delivering up to 650 W (seven such SSAs are in operation at ESRF, provided by ELTA/AREVA following a transfer of technology from SOLEIL). DC to RF power conversion efficiencies are denoted η.

An SSA combines the power from as many transistor modules as needed to provide the required nominal output power for one cavity with a given safety margin: 256 modules in the example shown in Fig. 3. The architecture and design of SSAs will be described in detail in Section 2 and a flavour of their performance will be given.

1.3 Radio frequency power sources for accelerating cavities – a brief history

This section concludes with a brief history and overview of the RF power sources used to feed accelerating cavities [7]. The graph in Fig. 4 shows the technologies used in various accelerator applications as function of the operating frequency and the required unitary power level.

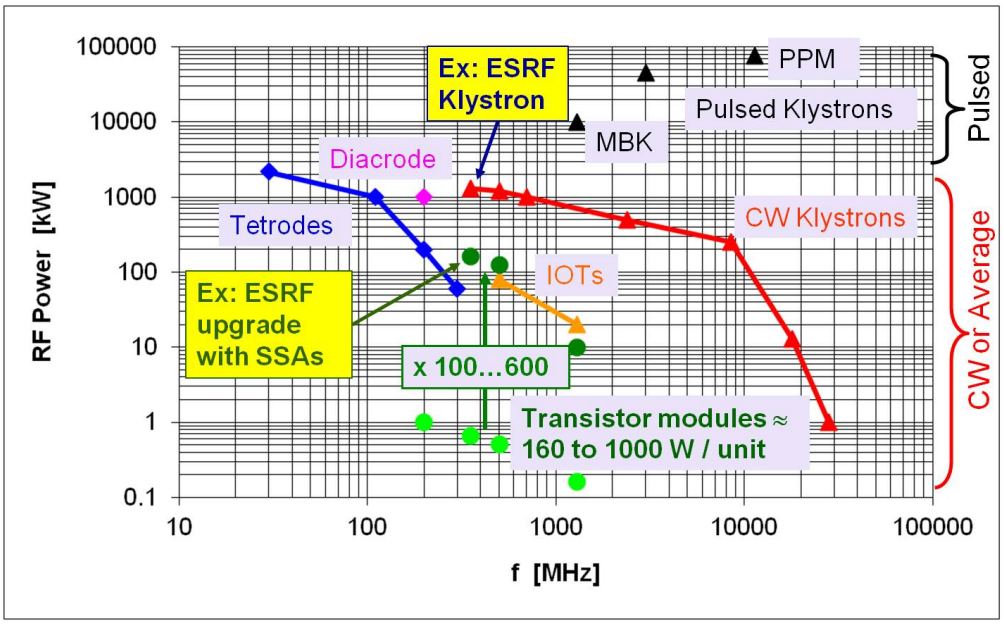


Fig. 4: Typical RF sources used in accelerators

Electronic vacuum tubes like triodes and tetrodes have existed since the early twentieth century. Due to their finite electron drift time they are basically limited to frequencies below 1 GHz. Tetrodes are still in use today for broadcast and accelerator applications to generate from kilowatts at 1 GHz up to hundreds of kilowatts below 100 MHz. Note that a small 3.5–5 GHz triode delivering 2 kW pulses exists for radar applications. With its optimized geometry the diacrode developed by Thales can deliver 1 MW at 200 MHz.

In the 1940s and 1950s tubes were developed for high frequency applications that benefit from the electron drift time. They are still widely in use, providing high RF power at high frequencies:

- klystrons: 0.3 GHz–10 GHz, delivering from 10 kW to 1.3 MW in CW and 45 MW in pulsed mode, with applications in TV transmitters, accelerators, and radar;
- IOTs (Inductive Output Tubes or klystrodes): a high efficiency mixture of a klystron and a triode, providing typically 90 kW at 500 MHz to 20 kW at 1.3 GHz, initially developed for SDI (Strategic Defence Initiative) in 1986, with current applications in TV and recently in several accelerators;
- travelling wave tubes (TWT): 0.3 GHz to 50 GHZ, broadband, highly efficient, with applications in satellite and aviation transponders;
- magnetrons: 1 GHz to 10 GHz, narrow band, mostly oscillators, highly efficient for applications in radar and microwave ovens;
- gyrotron oscillators: high power millimetre waves, 30 GHz to 150 GHz, delivering typically 0.5–1 MW pulses of several seconds duration, still subject to much R&D, used for plasma heating for fusion and military applications.

In the 1950s and 1960s the invention and spread of transistor technology also opened the way for many applications in the field of RF:

- bipolar, MOSFET, etc. transistors: delivering several tens of watts up to frequencies of about 1.5 GHz, recently up to 1 kW per unit with sixth generation MOSFETs;
- RF SSAs are increasingly used in broadcast applications, in particular in pulsed mode for digital modulation: 10 kW–20 kW obtained by combining several modules;
- SOLEIL: from 2000 to 2007 SOLEIL pioneered the development of high power 352 MHz MOSFET SSAs for accelerators: 40 kW for their booster, then 2 × 180 kW for their storage ring;
- ESRF: recent commissioning of seven 150 kW SSAs, delivered by ELTA/AREVA following a technology transfer from SOLEIL;
- increasing numbers of accelerator labs use, develop, or consider solid state technology for RF amplification, e.g. 1.3 GHz/10 kW SSAs from Bruker at ELBE/Rossendorf, 500 MHz SSAs for LNLS and Sesame designed by SOLEIL, etc.

2 RF solid state amplifier

In Fig. 5 is shown an RF SSA with its main components. The RF power from the drive amplifier system is split (2) and distributed to *n* amplifier modules (1) the outputs of which are recombined (3) and coupled to the RF waveguide feeder. A power converter system (4) supplies the amplifier modules with DC power. Components (1) to (4) are described in detail below.

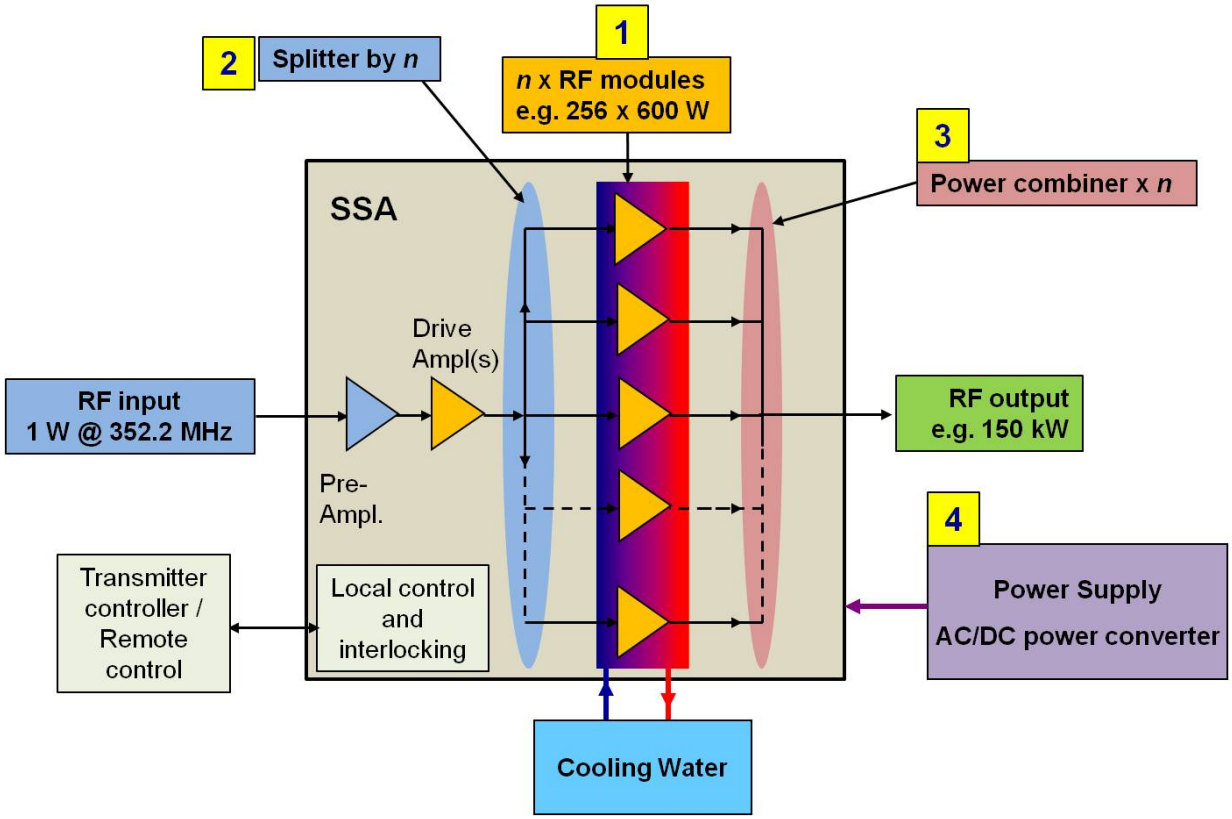


Fig. 5: Main components of an RF SSA. The example shown is an ESRF 352.2 MHz–150 kW amplifier

2.1 RF amplifier module

2.1.1 Transistor

Thanks to the latest developments in high power transistors such as the laterally diffused metal oxide semiconductor field effect transistor (LDMOS FET) and, in particular, the latest sixth generation devices with 50 V drain polarization, it is now possible to generate several 100 W up to 1 kW in CW with a single RF module, for frequencies up to about 1 GHz. Such transistors are, for instance, manufactured by NXP (Eindhoven/Netherlands) and Freescale semiconductor Inc. (Austin Texas/USA).

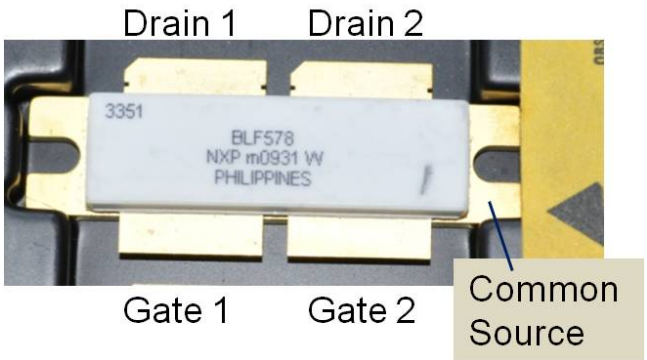


Fig. 6: Pair of push-pull transistors

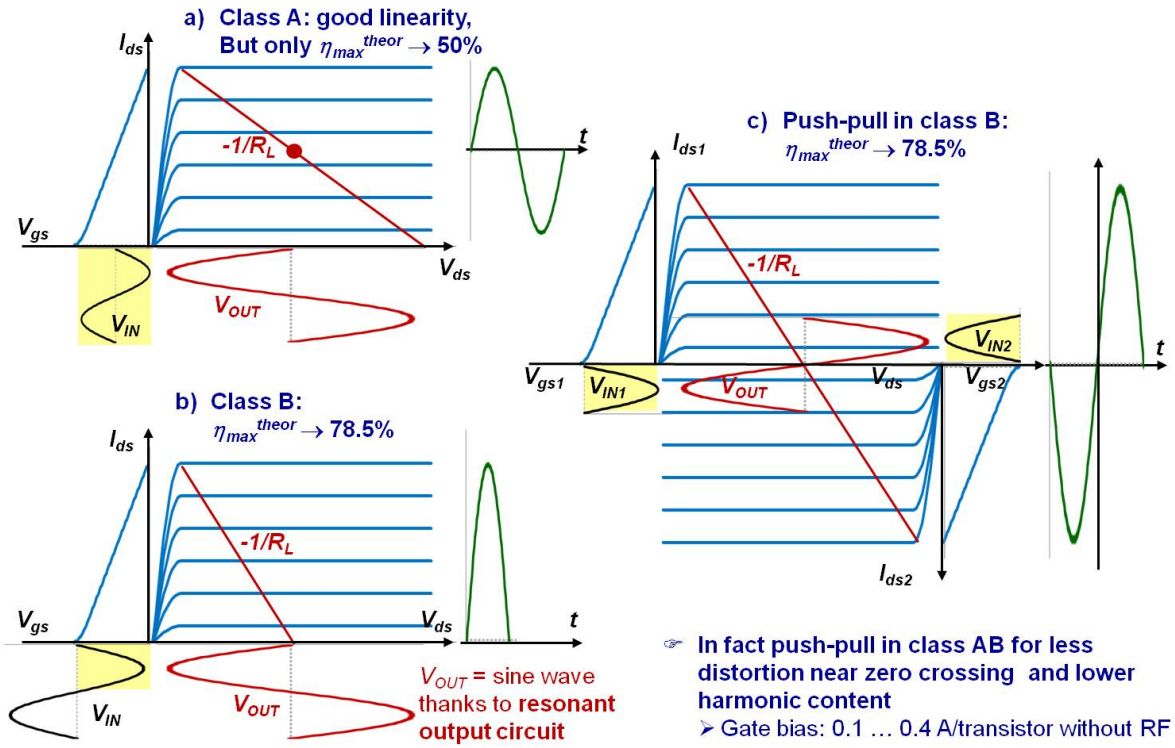


Fig. 7: Schematic of MOSFET operation modes. (a) Class A; (b) class B; (c) class B with two transistors in push-pull. In (a, b) drain-source current I_{ds} is given as a function of gate-source voltage V_{gs} on the left sides and as a function of the drain-source voltage V_{ds} on the right sides of the figures; In (c) drain-source currents I_{ds1} and I_{ds2} of both push-pull transistors are given as function of gate source voltages V_{gs1} and V_{gs2} on the left and right sides of the graphs, respectively, and as a function of the respective drain-source voltages V_{ds1} and V_{ds2} with V_{gs1} and V_{gs2} as a parameters in the centre of the graph. The red lines are the working lines of the load resistance R_L.

The ELTA/SOLEIL SSA implemented at ESRF uses the BLF 578 transistor from NXP in Fig. 6, which in fact contains two push-pull transistors with a common source, which are operated in class AB. As explained schematically in Fig. 7, this allows optimizing the DC to RF conversion efficiency while keeping the distortion and thereby the harmonic content low: the odd characteristic $I_{ds}(-V_{gs}) = -I_{ds}(V_{gs})$ minimizes the second harmonic H2 and higher even harmonics. As shown in Fig. 7, the working point for an amplifier in class A gives a good linearity as the complete input sine wave V_{in} is folded on the working line $-1/R_L$. But in class A the amplifier always consumes power, even without RF power. At best, the efficiency can approach 50% at full output power. In class B, the amplifier only consumes power when it is driven by RF. This provides a much better efficiency, approaching 78.5% for an ideal transistor. However, only one half of a sine wave is amplified and the signal must be filtered by a narrowband resonator in order to recover the RF signal: it is still polluted by a high harmonic content. Operating two transistors in push-pull in class B allows high efficiency to be maintained, and strongly reducing at least the even harmonics. In fact, the RF modules of the high power SSAs described in this paper are operated in push-pull in class AB with a slight gate bias to further linearize the amplifier characteristics and thereby minimize the harmonic distortions.

2.1.2 RF circuit

As shown in Fig. 8, the RF modules are fed with the unbalanced (unsymmetrical) RF signal from an incoming coaxial cable, which is transformed by a balun circuit into two RF signals that are 180° out of phase and drive the pair of transistors. The matching circuit, together with the bias circuit, determine the class AB working point to reach about 1 dB gain compression and a maximum efficiency of about

68–70% at a nominal output RF power of 650 W for the module shown in Fig. 8(c). Each RF module is protected by a circulator with a 1200 W load against reverse power, and can therefore withstand operating with full reflection. The small amount of power leaking backwards through the circulator slightly affects the gain; however, the impact is negligible when operating the device under normal conditions with up to 30% power reflection. The seven ESRF SSAs have been designed such that no power circulator is needed at an output of 150 kW after combining all of the RF modules.

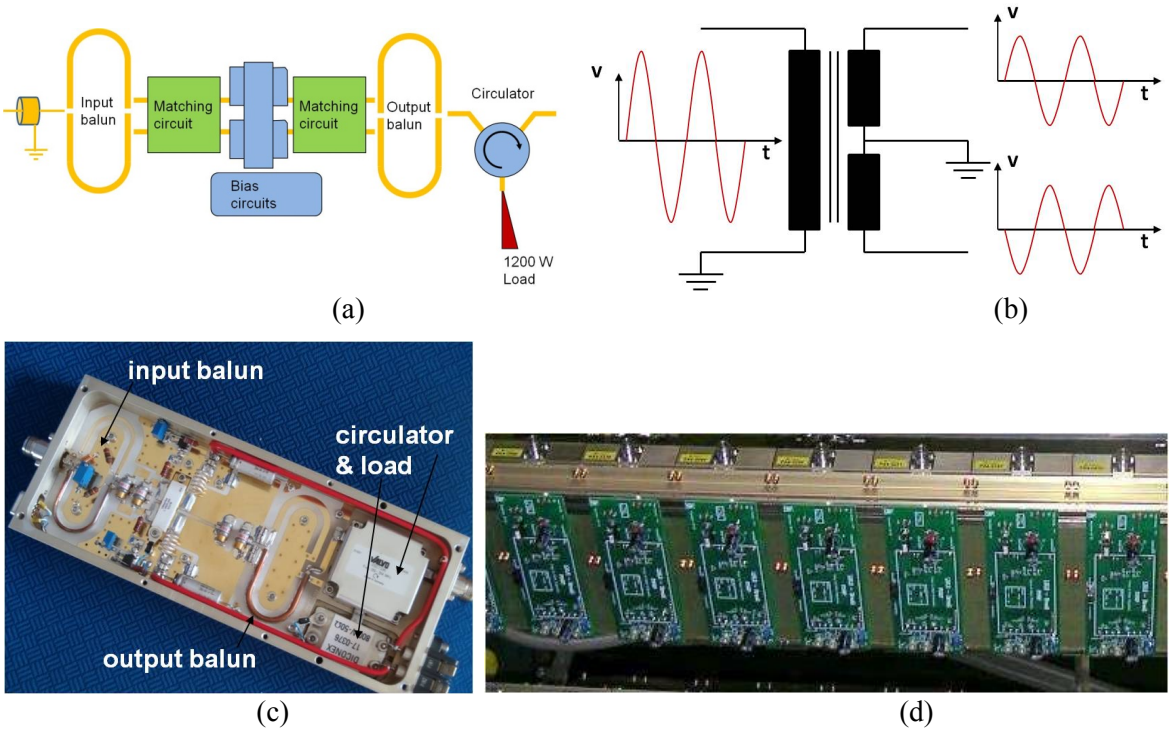
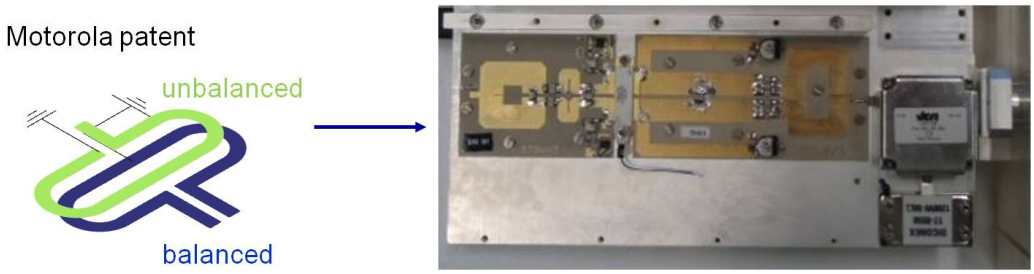


Fig. 8: RF circuit. (a) Schematic of the RF circuit comprising input and output balun transformers, matching circuits, a DC bias circuit, and a circulator with a 1200 W load to protect each transistor individually against excessive reverse power. (b) Input balun for the transformation of the unbalanced signal from the coaxial input into a balanced push-pull signal that drives the pair of push-pull transistors. (c) A 650 W ELTA/SOLEIL RF module as installed at ESRF. (d) Water-cooled plate supporting 16 RF modules on the rear side and 32 of the 280 V_{DC}/50 V_{DC} converter units (two per RF module) on the front side to feed each module with up to 1.2 kW DC power.

Each RF module is integrated in an individual shielded case. Sensors monitor the temperatures of the transistor socket and the load. The drain current of each pair of transistors is also monitored. These parameters allow the identification of damaged modules during operation.

Note that the input and output balun transformers in Fig. 8(c) are built with hand-soldered coaxial lines.

For the SSA under development at ESRF the fully planar 700 W RF module in Fig. 9 has been designed, and a series of these has been produced to equip a 75 kW prototype SSA. Hand soldering has been almost completely avoided by implementing a planar balun concept from Motorola, by replacing the RF drain chokes with planar quarter-wave transmission lines and minimizing the number of components, all of them surface-mounted devices (SMD) and prone for automated manufacturing. All of these measures allow cost-effective series production of the RF modules.



(a) (b)

Fig. 9: Development of a fully planar 700 W RF module at ESRF suited for cost-effective mass production. (a) Planar balun patented by Motorola; (b) fully planar ESRF module, efficiency 66% and gain 19.5 dB at 700 W output power.

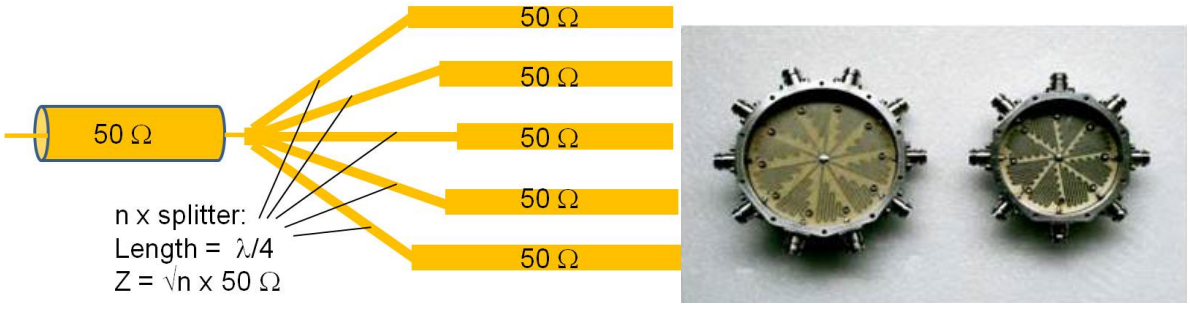
The parameters given in the caption for Fig. 9(b) are averages measured over the first series of 66 RF modules fabricated with automated SMD techniques. With a gain dispersion of 19.8 ± 0.6 dB and a phase dispersion of ±6°, a good combining efficiency is expected. Many factors contribute to these dispersions, such as the transistor dispersion and other components' parameters, as well as geometrical tolerances. The latter, however, are minimized by the automated pick-and-place technique. Apart from the gate bias, no other parameter has been tweaked.

There is still room for improvement in the achievable efficiency, which is still lower by 3% as compared to the ELTA/SOLEIL RF module. R&D is ongoing in the frame of a collaboration between ESRF and Uppsala University for the optimization of the circuit board.

Note that, as shown in Fig. 5, a few RF amplifier modules are required to amplify the low-level input RF power before splitting it again and distributing it to the inputs of all of the RF amplifier modules. In the ELTA/SOLEIL design, one pre-amplifier feeds four RF modules, each of which then feeds 64 RF power modules.

2.2 Power splitters

Power splitters are key components, designed to distribute the RF power from the drive amplifiers to the individual RF modules with minimum amplitude and phase dispersion. At 352 MHz a matched splitter distributing the drive power without reflections can be built as shown in Fig. 10. Each quarter-wavelength line transforms the 50 Ω at its output to $Z^2/(50\ \Omega) = n \times 50\ \Omega$ as seen from its input. The parallel connection of these n lines is thus matched to the 50 Ω of the incoming line.

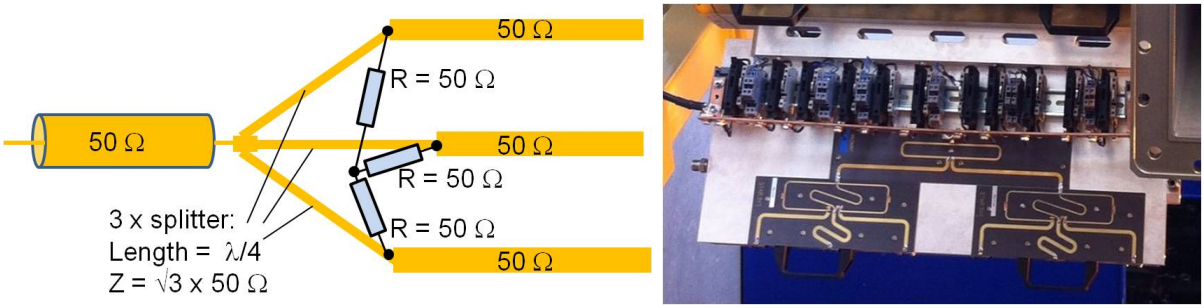


(a) (b)

Fig. 10: Matched RF stripline splitters for n outputs using quarter-wavelength ($\lambda/4$) transformers. (a) Schematic representation; (b) SOLEIL 10 and 8 line splitters (lids removed) [1, 2].

The Wilkinson splitter in Fig. 11 works in the same manner as the simple quarter-wavelength splitter shown in Fig 10. The additional 50 Ω resistors are not seen by the incoming split signals as they have the same amplitude and phase (common mode). However, differential signals are absorbed by

these loads, thereby decoupling the outgoing arms from each other. With a Wilkinson splitter, the connected amplifier inputs are therefore decoupled. Such Wilkinson splitters are implemented in the SSA in development at ESRF.



(a) (b)

Fig. 11: Wilkinson splitters: resistors absorb differential signals without perturbing the common mode, thereby decoupling the connected outputs from each other. (a) Schematic representation; (b) implementation on the SSA under development at ESRF.

2.3 Power combiner

SSAs are often built with several stages of power combiners that use quarter-wavelength transformers like the splitters shown in Fig. 10, except that they are operated in reverse and that the striplines are replaced with transmission lines that are adapted to higher power levels, mostly larger coaxial lines. As for the power splitters, the quarter-wavelength transformers guarantee that the combiner tree is matched in impedance to the connected high power output, provided that all of the inputs are at 50 Ω, which is the case thanks to the circulator/load system at the output of each RF amplifier module. However, as the combiners are non-directional, each individual amplifier does not at all see a matched impedance.

2.3.1 General considerations on power combiners

Before entering into the technology, let us first address some general characteristics of such power combiners. We consider a power combiner with n inputs in a single stage. One can easily derive the S-parameter matrix, which has the following general form:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ \dots \\ b_n \\ b_{n+1} \end{bmatrix} = \begin{bmatrix} (1-n)/n & 1/n & 1/n & \dots & 1/n & 1/\sqrt{n} \\ 1/n & (1-n)/n & 1/n & \dots & 1/n & 1/\sqrt{n} \\ 1/n & 1/n & (1-n)/n & \dots & 1/n & 1/\sqrt{n} \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 1/n & 1/n & 1/n & \dots & (1-n)/n & 1/\sqrt{n} \\ 1/\sqrt{n} & 1/\sqrt{n} & 1/\sqrt{n} & \dots & 1/\sqrt{n} & 0 \end{bmatrix} \times \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ \dots \\ a_n \\ a_{n+1} \end{bmatrix}, \quad (1)$$

where

$a_1 \dots a_n$ are the incident wave amplitudes at the input arms (coming from the amplifier modules);

$b_1 \dots b_n$ are the reverse wave amplitudes at the input arms (coming back to the amplifier modules);

b_{n+1} is the wave amplitude leaving the output arm of the combiner;

a_{n+1} is the reverse wave amplitude incident on the output arm (e.g. the reflection from the cavity).

Note that wave amplitudes a_i, b_i are measured in $\sqrt{W}$ and are generally complex, their arguments representing the respective phase of the wave at port i:

$|a_i|^2$ is the power of the wave incident on port i, where $a_i = |a_i|\, e^{j\varnothing i}$, and $\varnothing_i$ is the phase of the incident wave i;

$|b_i|^2$ is the power of the wave coming from port i, where $b_i = |b_i|\, e^{j\varnothing' i}$, and $\varnothing'_i$ is the phase of the reverse wave i.

The different terms in the S-matrix are also generally complex, their arguments depending on the exact geometry of the combiner. However, pertaining to the necessary symmetry of a single stage power combiner, all of the S-parameters $(1 - n)/n$ have the same arguments, as do all of $1/n$ and all of $1/\sqrt{n}$. The phases of the $(1 - n)/n$ and the $1/n$ are 180° apart. But the conclusions given below hold even if we neglect the additional phase terms.

a) Each connected RF module sees individually a strong mismatch with a reflection coefficient $(1 - n)/n$ that approaches −1 for a large n, corresponding to nearly full reflection.

b) The individual inputs for the amplifier modules are coupled to each other with a coefficient $1/n$ showing that this kind of combiner has no directivity at all.

c) However, *when all of the input waves are equal in amplitude and phase,* say with an amplitude a_0, their signals interfere perfectly well in the following way.

   i) For any $i,j \le n$,

   $$a_i = a_0 \Rightarrow b_j = a_j\,(1 - n)/n + \Sigma\,[a_{i\neq k,\le n}\,(1/n)] = [(1 - n)/n + (n - 1) \times 1/n]\; a_0 = 0\;, \tag{2}$$

   meaning that *any of the RF amplifier modules operates in matched condition* without any reflection. The strong reflection of its own signal is exactly compensated by the sum of the signals coupled from all other amplifier modules that have the opposite phase,

   ii) $$b_{n+1} = \Sigma\,[a_{i,\le n}\,(1/\sqrt{n})] = [n/\sqrt{n}]\; a_0 \Rightarrow |b_{n+1}|^2 = n\,|a_0|^2\;, \tag{3}$$

   meaning that, neglecting imperfections, *the power from all n inputs combines to 100% in the output arm* of the combiner, as expected.

So, the power adds up correctly at the output of a combiner only by constructive interference, i.e. if and only if the signals at their inputs have the same amplitude and phase. Any differential mode power is distributed as reverse power to the individual input arms, i.e. to the output stages of the RF amplifier modules, where it is absorbed by the circulator loads. So, good control of a flat amplitude and phase distribution are crucial for obtaining a good combining efficiency.

d) *If just one RF amplifier on arm i is switched off*, it will receive the reverse power coupled from all of the other arms without compensation by its own reflection:

$$b_i = \Sigma\,[a_{j\neq i,\le n}\,(1/n)] = [(n - 1)/n]\; a_0\;, \tag{4}$$

which approaches a_0 for a large n. The consequences are as follows.

   i) When one RF module is not providing power to the combiner, it receives from all the other modules a reverse power that is equivalent to the power of one module.

   ii) When one RF module is not providing any power to the combiner, the output power is lacking the equivalent power from two modules: the power from the missing module plus the power absorbed in the circulator load of the missing module.

   iii) When the SSA output is working on a mismatch with a reflection coefficient $r = |r|\, e^{j\varnothing}$, the reverse wave of amplitude $a_{n+1} = r\, b_{n+1}$ couples back to each module, including the unpowered RF module, as much as

   $$a_{n+1}/\sqrt{n} = r\, b_{n+1}/\sqrt{n} \approx r\,(n \times a_0/\sqrt{n})/\sqrt{n} = r\, a_0\;. \tag{5}$$

In total, an unpowered amplifier module on an arm i will see reverse power corresponding to the following reverse wave amplitude:

$$b_i = [(n-1)/n + r]\, a_0 \approx [1 + |r|\, e^{j\varnothing}]\, a_0 \Rightarrow |b_i|^2 \approx |1 + |r|\, e^{j\varnothing}|^2\, |a_0|^2 , \quad (6)$$

with the worst case

$$\varnothing = 0 \Rightarrow |b_i|^2 \approx (1+|r|)^2\, |a_0|^2 . \quad (7)$$

For full reflection $|r| = 1$, a non-powered RF module can therefore see reverse power as high as four times the nominal power of one module.

For the ELTA SSA, ESRF had specified a maximum reflection of one third of the incident power. Given the nominal module power of 630 W, this means that in the worst case as much power as

$$P_{\text{reverse}}^{\max} = |b_i|^2 \approx (1 + 1/\sqrt{3})^2 \times 630\ \text{W} = 1570\ \text{W} \quad (8)$$

can come back to the circulator and then into the load of an unpowered RF module. Such values were indeed measured on the real SSA shown in Fig. 3. The way to avoid overloading the 1200 W circulator loads of the RF modules is described in Section 2.3.2.

2.3.2 Coaxial combiner

In most of the existing high power SSAs the power from the individual RF amplifier modules is combined by means of several stages of cascaded coaxial combiners. The SOLEIL SSAs and the 150 kW SSAs in operation at ESRF are literally built around coaxial combiner trees that become amplifier 'towers' in the final assembly. As shown in Fig. 3, the power from two such 75 kW towers is further combined to feed up to 150 kW into an outgoing WR2300 waveguide. The size of the coaxial combiners depends on the power level as, for example, shown in Fig. 3:

- first stage: 630 W × 8 by means of EIA[2] 1 5/8″ coaxial combiners yielding 5 kW;
- second stage: 5 kW × 8 by means of EIA 6 1/8″ coaxial combiners yielding 40 kW;
- third stage: 40 kW × 2 by means of EIA 6 1/8″ coaxial combiners yielding 80 kW;
- fourth stage: 80 kW × 2 by means of an EIA 9 3/16″ coaxial combiner yielding 160 kW (maximum power, the nominal value being 150 kW).

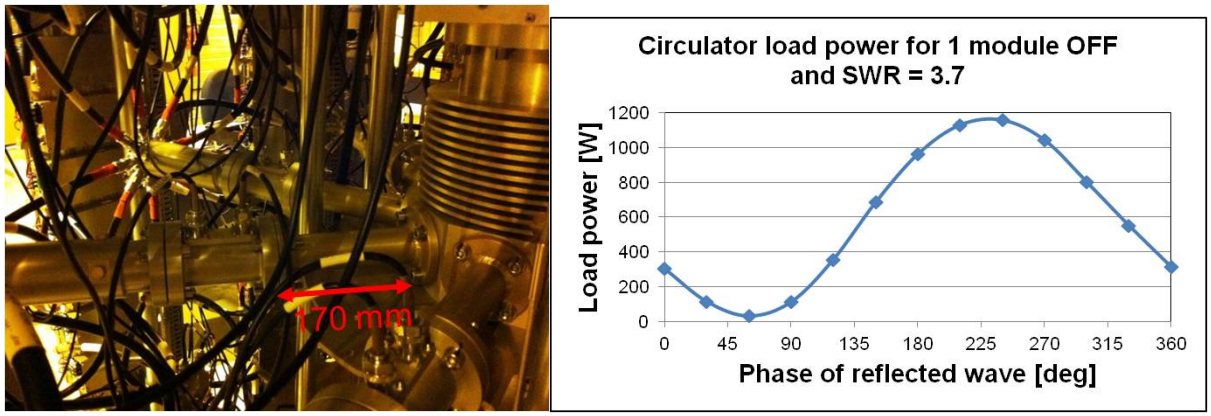
Dimensioning of the circulator loads and fine tuning of the coaxial combiner

Initially, the circulator loads of the 150 kW SSAs for ESRF were dimensioned so as to withstand full module power up to 650 W maximum in full reflection at any phase. This was met by selecting a corresponding circulator and an 800 W load. The SSAs were also tested successfully at full power with up to 30% power reflection at any phase. The SSAs had furthermore been designed with sufficient power reserve to benefit from the intrinsic redundancy of many combined RF amplifier modules, and full output power could easily be fed into a matched load with up to six missing RF modules! However, when testing the first SSA at full power with 30% reflection and some of the modules switched off, the output circuits and the loads of the unpowered RF modules were damaged, while the phase of the mismatch was varied. In fact, operating conditions as described in Eqs. (6–8) lead to an overloading of the circulator loads of the non-powered RF modules. As much as 1500–1700 W was measured depending on the location in the combiner, confirming experimentally the 1570 W predicted in Eq. (8).

Fortunately, the coaxial combiner in the 150 kW ESRF SSA has multiple stages. Its S-parameter matrix does not have the exact symmetry of the single-stage combiner in Eq. (1). When all n of the RF modules feed the combiner with equal amplitudes and phases, their power still combines perfectly into

[2] EIA: US American Electronic Industries Alliance standard

the output port $n + 1$. Depending on the length of the output arms of the combiners, for instance in the first stage as shown in Fig. 12, the reverse power coming to an RF module from its seven immediate neighbouring RF modules interferes more or less constructively or destructively with the power coming from the other RF modules [8]. The tests had revealed that this interference was close to maximum when the load was burnt. As suggested by the experts from SOLEIL [8] and shown in Fig. 12, this interference could be made destructive by inserting 170 mm long delay lines at all of the outputs of all of the first combiner stages. The measurements shown in Fig. 12(b) show that the load power of a switched-off module then remained below 1200 W when operating the SSA at the specified maximum mismatch and varying the phase of the reflected wave. To complement the modification shown in Fig. 12, the 800 W circulator loads were replaced with 1200 W loads, as already shown in Fig. 8.



(a) (b)

Fig. 12: Minimization of the circulator load power of a switched-off RF module when the 150 kW SSA operates on a mismatch corresponding to 30% power reflection. (a) Insertion of a 170 mm delay line at the output of the first combiner stage; (b) measured load power is reduced from maximum 1700 W down to 1200 W.

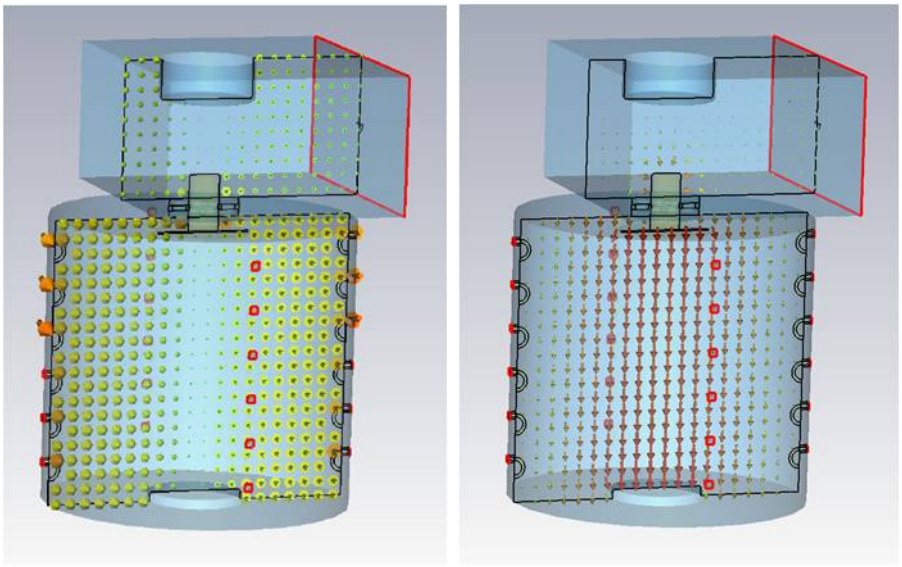
The modifications described above were implemented for the three SSAs that are operated in continuous wave (CW) on the ESRF storage ring. This was not necessary for the ESRF booster, which is run in pulsed mode and where the relevant average load power remains well below 800 W.

2.3.3 Cavity combiner developed at ESRF

A compact single-stage cavity combiner is under development at ESRF. As shown in Fig. 13, its E_{010} resonance has a homogeneous azimuthal and longitudinal field distribution. For the 352.2 MHz ESRF application, the outer cylindrical wall is equipped with six vertical rows of 22 input loops distributed around the circumference. In total 132 transistor modules like that shown in Fig. 9, delivering up to 700 W each, will be connected to these coupling loops. The total output power is expected to be between 80 kW and 90 kW.

The coupling β_{module} must be the same for all of the input loops. It is easily adjusted by means of the loop size (typically a few square centimetres). The coupling of the output waveguide $\beta_{\text{waveguide}}$ is mainly determined by the size of the capacitive disc that couples to the electrical field of the E_{010} resonance. To obtain matched conditions and an optimum combining efficiency for a number n of RF modules, the coupling factors must be set according to:

$$\beta_{\text{waveguide}} \approx n \times \beta_{\text{module}} >> 1 \ . \tag{9}$$



(a) (b)

Fig. 13: Strongly loaded E_{010} resonance of a cylindrical resonator to combine the power from 132 RF modules in a single stage. (a) H field: homogeneous magnetic coupling to 132 input loops on the cylindrical wall; (b) E field: strong adjustable capacitive coupling to the output waveguide.

As shown in Fig. 13 and implemented on the ESRF prototype in Fig. 14, the piston attached to the top of the waveguide can be moved up and down, and the back short-circuit plane can be moved back and forth. This allows adjustment of the coupling factor β_{module} in a range of about 1:3 and thereby matching the SSA for a variable number of connected modules. The nominal power of the SSA can therefore be easily adapted to changing operating conditions by simply removing a number of RF modules and re-adapting the waveguide coupling accordingly.

Figure 14 shows the prototype ESRF amplifier with cavity combiner. The water-cooled 'wings' that support six RF modules each constitute a section of the cavity wall with built-on coupling loops. The RF modules are hence directly flanged to the combiner and there is no need for coaxial RF power cables. The RF splitters for the distribution of the RF drive power as well as the DC power distribution are fixed onto the rear sides of the wings. The prototype in Fig. 14 with only three active wings and 19 blind flanges delivered as much as 12.4 kW of RF power with a DC-to-RF conversion efficiency of 63%.

(a) (b) (c)

Fig. 14: Prototype with three wings and a total of 18 700 W RF modules, successfully tested at 12.4 kW with a DC-to-RF efficiency of 63%. (a) Cavity combiner with WR2300 output waveguide; (b) direct coupling of RF modules; (c) water-cooled wing with six RF amplifier modules.

The extension of the prototype with a total of 22 active wings is close to completion and will be ready for power tests in 2015. The achievable output power is estimated to be between 80 kW and 90 kW, which is even slightly above the power obtained from one ELTA/SOLEIL coaxial tower. At the same time, the cavity combiner is more compact by far than an equivalent coaxial combiner.

2.4 Power supply

As shown in Fig. 8 the ELTA/SOLEIL SSAs are equipped with two 280 V_{DC}-to-50 V_{DC} converters per RF module. Each of the three 150 kW SSAs in operation on the ESRF storage ring is fed with one 300 kW/400 V_{AC}-to-280 V_{DC} converter, which was developed by the ESRF Power Supply Group. As may be seen in Fig. 15, a 280 V_{DC}-to-RF conversion efficiency of 57% is obtained at 150 kW output power. Beyond nominal power, the efficiency approaches 60%.

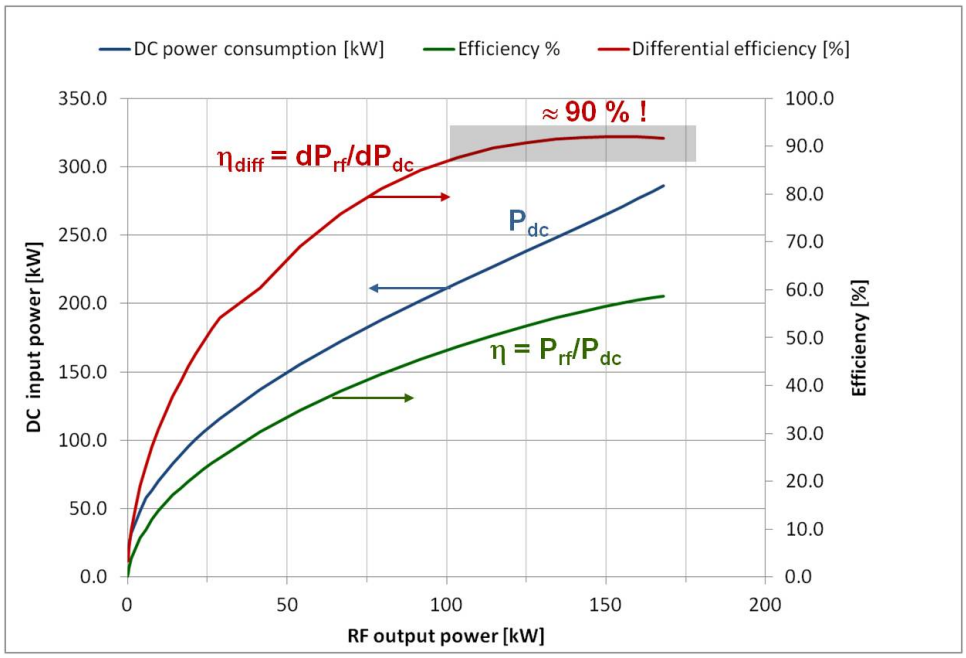


Fig. 15: DC-to-RF efficiency and required DC power as a function of the output RF power of the ELTA/SOLEIL SSA implemented at ESRF.

It is worth noting that the efficiency drops fast when operating the amplifier at reduced power, and is only about 47% at 100 kW, i.e. at ⅔ of the nominal power. Note also that in the upper range 100–150 kW, the differential efficiency is about 90%, meaning that, with 1 kW of additional DC power, one obtains as much as 0.9 kW of additional RF power. In other words: in order to make good use of the electrical power, it is important to correctly dimension the RF system and operate the SSAs close to their nominal power. Unfortunately, when designing an RF system, it is generally common practice to slightly over-dimension the available power in order to be able to overcome unforeseen transmission losses and to be prepared for possible power upgrades of the accelerator.

A nice feature of the cavity combiner described in section 2.3.3 is that one can at any time remove a number of RF modules and easily re-adapt the output coupling. This way it is easy to bring down the nominal power of an over-dimensioned SSA close to required operation level and recover a good overall efficiency. Reference [9] describes another method for recovering good efficiency at reduced power by modulating the drain voltage of the transistors. However, it is important to check the stability of the amplifier modules over the entire range of the drain bias.

Four 150 kW SSAs feed the accelerating RF cavities of the ESRF booster. Currently, a system of resonant AC and DC power supplies feed the booster magnets with a 10 Hz sine wave. The dipole magnet currents determine the modulation of particle energy *E* in the booster, as shown in Fig. 16. The

RF voltage V_{tot} performs the bunching of the beam injected from the linac at 200 MeV and accelerates it to 6 GeV where it is extracted to the storage ring. In this process, the largest portion of RF voltage is needed to compensate for the synchrotron radiation losses that scale with E^4 and lead to the red curve for the total accelerating voltage V_{tot} in Fig. 16. The total DC power $P_{dc\text{-}tot}$ absorbed by the SSAs to produce the RF power P_{rf} needed to obtain this voltage is oscillating at 10 Hz between about 100 kW and 1000 kW. An anti-flicker capacitor bank of 3.2 F has been installed to prevent this power fluctuation being transmitted to the mains. The residual flicker thus remains well below the legal limit of 0.29%. A good side effect is that an AC power of maximum 400 kW, slightly above the average DC power $P_{dc\text{-}aver}$ in Fig. 16, is drawn from the mains. This constitutes a reduction of nearly a factor 3 in power consumption with respect to the previous klystron transmitter, for which a 10 Hz filtering was not possible at 80 kV supply voltage. The klystron was operated with input RF modulation and constant beam power, most of this power being absorbed in the klystron collector.

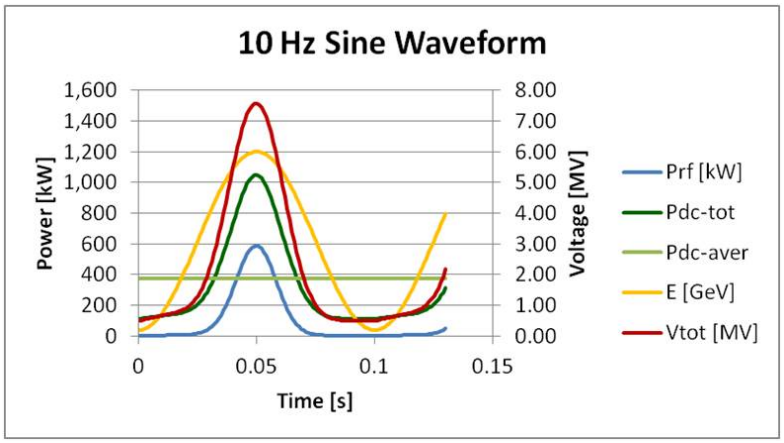


Fig. 16: Pulsed RF for the ESRF booster

For the SSA with the cavity combiner under development at ESRF, the RF modules will be fed from 22 power converters, one per wing, with a direct conversion from 400 V_{AC} to 50 V_{DC}. They will be installed close to the SSA in order not to carry the high currents over longer distances.

2.5 Specification

Having addressed the main ingredients of a high power RF SSA, typical performance data are now reviewed, however not exhaustively, based on the 352.2 MHz–150 kW SSAs delivered by ELTA to ESRF.

- The specified 280 V_{DC}-to-RF conversion efficiency was easily met:
  - ✓ $\eta > 57\%$ at $P_{nom} = 150$ kW (specified: $\eta > 55\%$);
  - ✓ $\eta > 47\%$ at ⅔ $P_{nom} = 100$ kW (specified: $\eta > 45\%$).
- Gain compression <1 dB at $P_{nom} = 150$ kW.
  - Figure 17 shows the typical gain curve of one 150 kW SSA at ESRF. The P1 point, at which the gain compression reaches 1 dB, has been set above the nominal output power to limit distortion and safeguard the transistor against drain over-voltage. The P1 point is adjusted by means of the load resistance R_L in Fig. 7.
- Avoid overdrive conditions.
  - High peak drain voltage can damage the transistor. It is thus crucial to implement an overdrive protection interlock.
- Short pulses (20 µs).

  - RF cavities and their power couplers need to be slowly conditioned to high RF power, starting with cycles of 20 µs short pulses, then increasing the pulse length up to CW operation.
  - Up to 1.3 dB transient gain increase has been measured in pulsed operation, which bears a risk of overdrive. The overdrive protection therefore needs to be adjusted carefully.

– Requested redundancy for reliable operation.
  - All of the points from the specification in terms of power and operating conditions are achieved with up to 2.5% missing RF modules, i.e. with up to six RF modules in fault. As never more than one or two modules fail at the same time, the SSA never stops for output module failures. One can wait until the next programmed maintenance shutdown to exchange faulty modules.
  - The requested redundancy requires some power margin that is paid for with a slightly lower efficiency than that which is ultimately achievable. The power margin thus needs to be dimensioned carefully.
  - Note that if one of the RF power modules used in the drive chain fails, the output power can no longer be maintained and the SSA may trip the accelerator.

– Harmonics:
  - ✓ H2 < −36 dBc (36 dB below carrier at 704.4 MHz);
  - ✓ H3 < −50 dBc (50 dB below carrier at 1056.6 MHz).

– Spurious sidebands/phase noise:
  - ✓ Sidebands < −68 dBc at 400 kHz (DC/DC converter switching, harmless).
  - ✓ A substantial improvement as compared with −50 dBc for klystrons from voltage ripples of the HV power supplies at 600 Hz, 900 Hz, 1200 Hz, etc., which are, moreover, much closer to the synchrotron frequency at which the stored beam is extremely sensitive.

– Operation on mismatched load:
  - ✓ 150 kW output power with ⅓, i.e. 50 kW, reflection at any phase,
  - ✓ 80 kW output power with 100% reflection at any phase,
  - ✓ 150 kW output power with 100% reflection at any phase for a duration of up to 20 µs.
  - Note that for high power reflections, due to the limited isolation of the circulators of the RF modules, the residual reverse power reaching the transistor output circuit provokes a gain modulation. Also, the power combiner itself contributes to some gain modulation in the presence of high reflected power. As a result, the specified output power cannot be reached for some phase values of the mismatch, due to the overdrive limitation.

– Reliability:
  - ✓ Not more than 0.7% of the installed RF power modules, including their individual DC/DC converters, are allowed to fail within one year.
  - With seven 150 kW SSAs gradually commissioned at ESRF between early 2012 and the end of 2013, not including early failures with less than 1000 hours of operation (debugging), the failure rate is in the range of the specified 0.7% per year. However, the cumulated operating time is still too low to give a statistically sound statement.

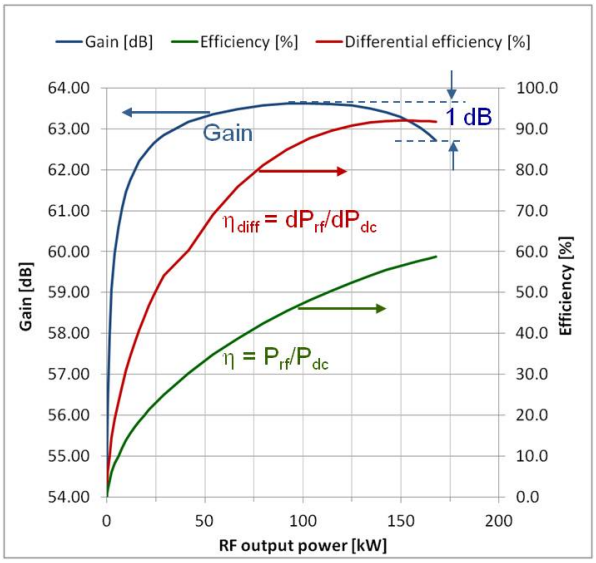
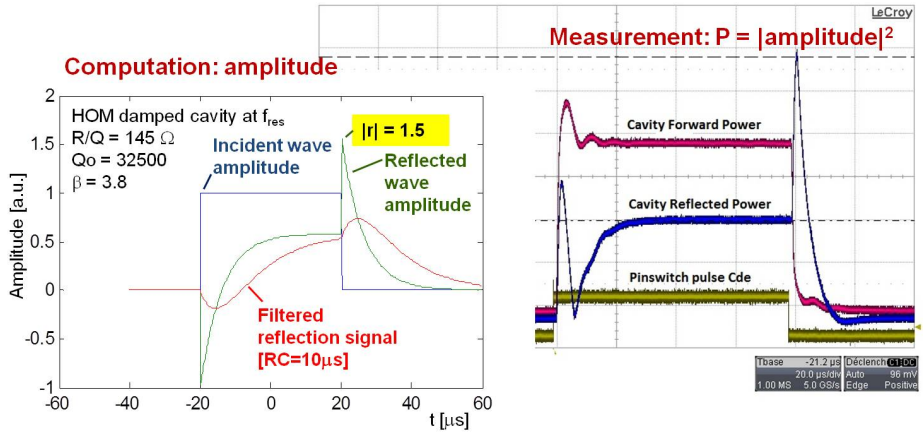


Fig. 17: Gain and efficiency of an ESRF 352.2 MHz–150 kW SSA delivered by ELTA

2.6 Transient reflections for pulsed cavity conditioning

For the RF conditioning of accelerating cavities they are fed with short RF pulses. The physical explanation for the transient wave amplitudes in Fig. 18(a) is straightforward:

- the leading edge of the incoming RF pulse sees the cavity as a short circuit and is reflected with a factor of −1;
- after the filling time of the cavity ($T_f = Q_o/(\pi f_{rf}\,(1+\beta)) = 6.1$ µs), the reflection coefficient approaches the steady-state value $r = (\beta - 1)/(\beta + 1) = 0.58$;
- the negative falling edge of the incoming pulse again sees a short with $r = -1$ and gives rise to a positive transient reflection of amplitude 1 that adds to the 0.53 amplitude of the almost steady reflection: the total transient reflection therefore peaks at more than 1.5 times the incoming pulse amplitude, corresponding to more than twice the input power;
- after the cavity filling time of 6.1 µs, the reflected pulse vanishes;
- The measurement of the incident and reflected power transients shown in Fig. 18(b) confirms this behaviour: the scope traces correspond to the squared amplitude plots shown Fig. 18(a).



(a) (b)

Fig. 18: Transient reflections when conditioning an accelerating cavity with short RF pulses. (a) Calculated transient wave amplitudes; (b) measured transient wave power.

The SSAs are protected against reflections exceeding the specified 50 kW as noted above. However, for a duration below 20 µs a reverse power of 150 kW is acceptable. Therefore, in order not to trip the SSAs for pulsed cavity conditioning, the signal triggering the 50 kW interlock was filtered as shown in the red curve in Fig. 18(a). This interlock then only triggers for power exceeding the maximum cavity conditioning power of 80 kW. The SSA is still protected by a second unfiltered fast interlock that triggers if the reflected power transient exceeds 150 kW. Taking into account the power reflection on the falling edge of the pulse, this interlock will trigger if the incident power exceeds the 80 kW needed for cavity conditioning.

3 Conclusions – a short comparison between klystrons and solid state amplifiers

To conclude this paper the pros (+) and cons (−) of implementing high power RF solid state amplifiers as an alternative to klystrons are tentatively addressed.

+ SSAs do not need a high voltage power supply (50 V instead of 100 kV):
  + consequently there is no need for X-ray shielding;
  + 20 dB less phase noise.
+ High modularity/redundancy providing a high reliability in operation:
  - the SSA is still fully operational if a few RF modules fail, except if a driver module fails.
− More space required per kW for a SSA than for a klystron:
  - however, thanks to the modularity, it is easier to precisely match the power of an SSA to the requirements;
  - the cavity combiner provides a substantial size reduction when compared to a coaxial combiner tree.
- Durability and obsolescence.
  - Klystrons: there is no problem with klystrons and tubes in general for as long as a particular model is still manufactured. But it can become very problematic in the event of obsolescence, as the development costs for new tubes are too high for medium-sized labs.
  - SSAs: transistors generally have a shorter product lifetime. However, there will always be comparable or even better transistors on the market. Nevertheless, operating SSAs commits the user to carefully follow the transistor market and react quickly enough to develop RF modules with new transistors that fit into the existing SSAs.
  + Easy maintenance of SSAs if sufficient spare parts are available.
- Investment costs:
  − SSAs have still a higher price per kW than comparable tube solutions.
  + But SSA technology is progressing. A significant cost reduction is for instance expected from the possible mass production of fully planar RF modules as the ones developed at ESRF (see Section 2.1.2). Also the use of compact cavity combiners will reduce the fabrication costs as compared to building up large coaxial combiner trees.
  + Prices for SSA components should sink while prices for klystrons have strongly increased over the last decades.
  + Low cost of possession:

    - With about 0.7% RF modules failing per year and relatively easy and inexpensive repair, the possession costs of SSAs are in principle very low and, in any case, substantially lower than for klystron transmitters, due to the high cost of spare klystrons.

- SSA and klystrons have comparable power efficiencies. However, this must be analysed case by case.
    + For the ESRF booster's pulsed RF system, for instance, a reduction of the power consumption by a factor of almost 3 was obtained, thanks to possible capacitive filtering of the DC supply voltage.

This list of arguments is far from being exhaustive. The question of the best selection of technology to provide high RF power for accelerator projects is a standing item on the agenda of RF workshops and conferences. Yet, more and more labs are considering SSAs as an adequate solution for their RF needs. For the moment, I would state that for multi-megawatt applications, klystrons remain advantageous. However, for accelerator applications of several hundreds of kilowatts, in particular for medium-sized projects with limited human resources, solid state amplifiers will become more and more attractive.

Acknowledgments

This paper is in tribute to Ti Ruan, who passed away in March 2014. In the early 2000s Ti Ruan initiated the design and the implementation of high power SSAs combining hundreds of transistors for larger accelerators. He is the father of the big SSAs implemented at SOLEIL, ESRF, and many other places around the world.

Many thanks are also due to the SOLEIL RF team: P. Marchand, R. Lopez, and F. Ribeiro; to the ELTA team: mainly J.-P. Abadie and A. Cauhepe; and to my RF colleagues at ESRF, in particular: J.-M. Mercier and M. Langlois. Their contributions constitute the backbone of this lecture.

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Long Pulse Modulators

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Abstract
Long pulse modulators are used to produce high-voltage, high-power pulses with durations of several hundred microseconds up to some milliseconds. The loads are one or more klystrons for producing RF power to accelerate the particle beam in superconducting cavities. After years of development and improvements in different institutes a variety of topologies exist, and are presented. The basics of modulators, pulse requirements and klystrons are explained. Additionally, the charging of internal energy storage will be addressed. The outlook for future developments is given.

Keywords
Modulator; long pulse modulator; klystron modulator; klystron supply; pulsed power; high-power pulses; RF-station.

1 Introduction

The development of long pulse modulators started in the early 1990s in combination with the development of superconducting cavities for accelerating particles. The design aim at that time was a linear accelerator called TESLA, which would have had a length of approximately 30 km. Although this accelerator was not built, the superconducting technology for cavities is being implemented in the European X-ray Free-Electron Laser Facility (XFEL) that is currently under construction in Hamburg.

Operating such an accelerator in continuous mode would form a large heat load for the cryogenics. The operating cost would be extremely high. Therefore these cavities are operated in pulsed mode with a duty factor of approximately 1.5%. As a consequence the high voltage supply to the klystron is pulsed for the duration of the RF that is required.

Long pulse modulators produce pulsed high voltage with a pulse length of a few 100 µs to some milliseconds. Fermilab National Accelerator Laboratory (Fermilab) [1] developed the first modulators of this type, which were later operated at DESY (Fig. 1). Here, further improvements and technology transfer to manufacturers were carried out.

In the following the basics of the RF station with the main components, basic specifications of the pulse and different types of modulators will be explained, including examples of modulators that have been built and operated in different laboratories. Finally, the outlook for future developments will be given.

2 XFEL RF station

The modulator is part of an RF station. Figure 2 shows the topology of the RF station at XFEL [2]. The unit producing the pulsed power is called a modulator. The high-voltage power supply (HVPS) takes electrical power from the grid and stores energy in order not to disturb the grid. By means of the pulse-forming unit high-voltage pulses are generated at a voltage level of 10 kV. A pulse transformer transforms the pulses to 120 kV. This is the voltage that is required by the klystron in which RF power is produced. Waveguides transport the RF to the superconducting cavities.

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Fig. 1: Bouncer modulator developed at FNAL

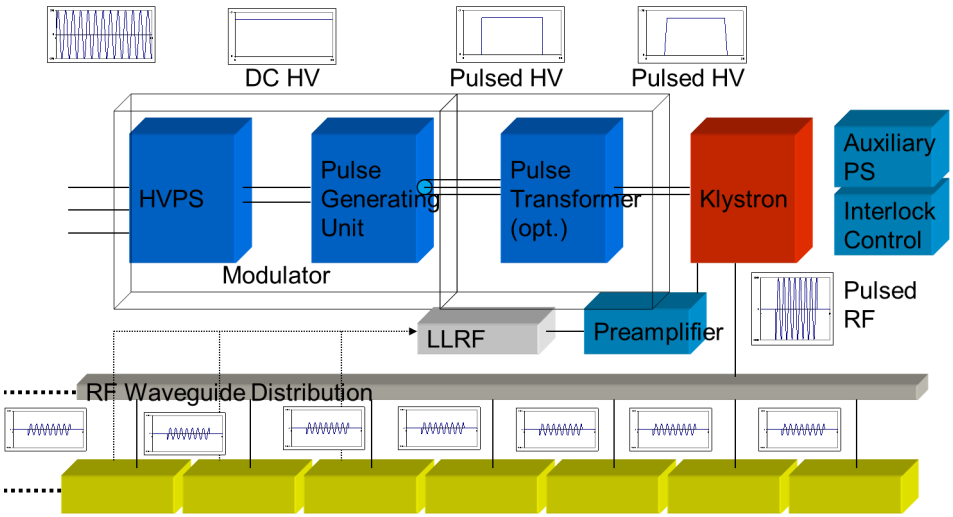

Fig. 2: Typical RF station as used in XFEL

2.1 Klystron

The klystron is a vacuum tube in which RF power is generated. A low-power RF signal is amplified and high-power RF is provided. A klystron is operated at high voltages, for example the nominal XFEL klystron voltage is 115 kV. At this working point, it can generate 10 MW RF at 1.3 GHz for 1.34 ms, which is 200 µs less than the modulator pulse. For the modulator the klystron is a load with the following relation between current and klystron voltage:

$$I = \mu P \times U^{3/2} \tag{1}$$

where I is klystron current, U is klystron voltage and μP is µPerveance.

The μPerveance is a parameter of the klystron. It is determined by the geometry and is constant for each klystron. The characteristic curves of the klystron represented by Eq. (1) are given in Figs. 3 and 4. These are the klystron current as a function of voltage (Fig. 3) and the resistance at the operating point as a function of voltage (Fig. 4).

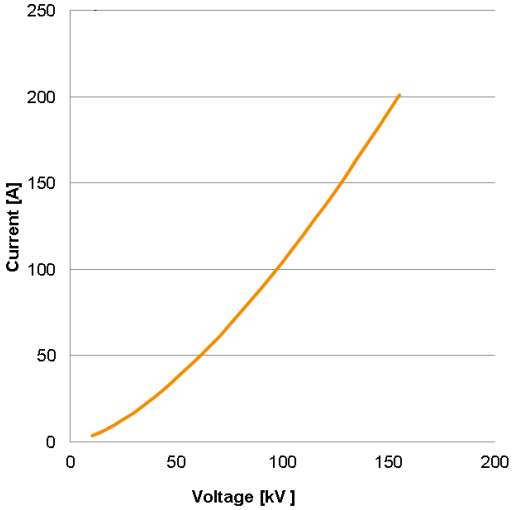

Fig. 3: Klystron current as $f(U_{\text{klystron}})$

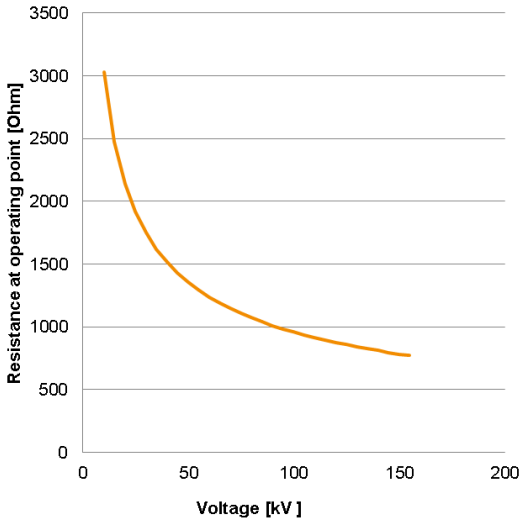

Fig. 4: Equivalent resistance as $f(U_{\text{klystron}})$

For simulation and calculation of the modulator behaviour it is possible to use a simple resistor with series diode. To enhance simulations in a wide range of operation, the resistance has to vary according to the characteristic curve.

The beam power of the klystron is approximately

$$P_{\text{Beam}} = \mu P \times U^{5/2} \tag{2}$$

and RF power is

$$P_{\text{RF}} = \eta P_{\text{Beam}} \tag{3}$$

where η is the efficiency of the klystron.

2.2 Electrical data for the XFEL Thales TH801 multibeam klystron

Figure 5 shows the Thales TH801 multibeam klystron used in the XFEL, and electrical data are given in Table 1.

Fig. 5: Thales TH801 multibeam klystrom

Table 1: Electrical data for the Thales TH801 multibeam klystron

Parameter	Value
Cathode voltage	117 kV
Beam current	131 A
µPerveance	3.27
Electrical resistance	893 Ω at 117 kV
Maximum RF peak power	10 MW
Electrical power	15.33 MW
Electrical pulse duration	1.54 ms (1.7 ms max)
RF pulse duration	1.34 ms
Repetition rate	10 Hz
Efficiency	65%
RF average power	150 kW
Average electrical power	280 kW

2.3 Klystron arcing

During operation arcs inside the klystron may occasionally occur. The HV collapses to the burning voltage of the arc and the short-circuit current increases. When an arc occurs the modulator has to detect it, interrupt the energy supply to the klystron and dissipate all energy stored in the current path to the klystron, in chokes, capacitors or even long cables, for example. Only 10 J to 20 J are allowed to be deposited in the klystron. More would damage the surface, leading to a derating or even damage to the entire klystron.

The equivalent circuit for an arcing klystron is a series combination of a voltage source of 100 V and a resistor. The 100 V corresponds to the burning voltage of the arc. Actually, no real measurements are available. In the literature, values of arc voltages are between 30 V to 100 V. To be on the safe side, for protection of the klystron, the conservative value was taken. The resistor represents a current-dependent component. The resistance is assumed to be 100 mΩ.

The equivalent circuit for the entire klystron is shown in Fig. 6. It represents the characteristic resistance given in Fig. 4 and the arc-model circuit. The following simulations are based on this equivalent circuit. During normal operation only the characteristic curve is valid, but it is important to have the protective part for the fault in mind.

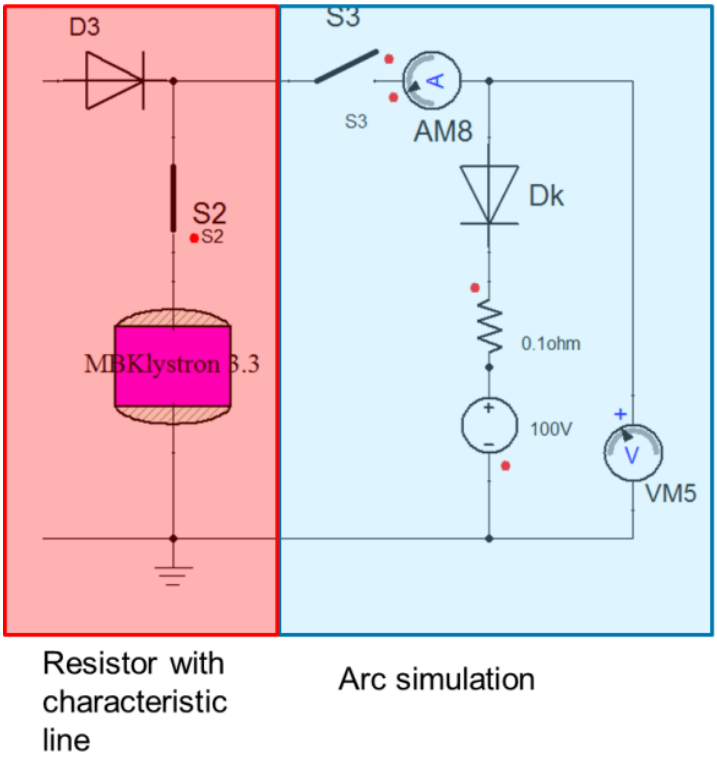

Fig. 6: Simulation model of a klystron

3 Definition of the pulse

When talking about pulsed power a few definitions are given to describe the performance of modulators and the pulse. These might differ at different laboratories.

Table 2: Pulsed power definitions

Term	Definition
HV pulse	At DESY the HV pulse duration is given from turn on of the pulse-forming unit, other labs use an uptime of, for example, 70% of the HV.
Rise time	Time from the start up to the flat top. This is often defined as 10% to 90% or 10% to 99%.
Flat top	The time when the pulse is at the klystron's operating voltage. Variations, called ripple, lead to RF phase shifts that have to be compensated for by the Low Level RF system (LLRF). The flat top is defined as x% or $\pm x$% of the voltage. At XFEL 0.3% pp was defined.
Fall time	The time that the modulator voltage requires to drop down.
Reverse voltage	Also known as the undershoot, this is the maximum allowed negative voltage, it is approximately 20% of the klystron operating voltage
Repetition rate	Frequency of pulse repetition.
Pulse to pulse stability	Value of the repeating value of the flat top.

Figures 7 and 8 show the above-defined values.

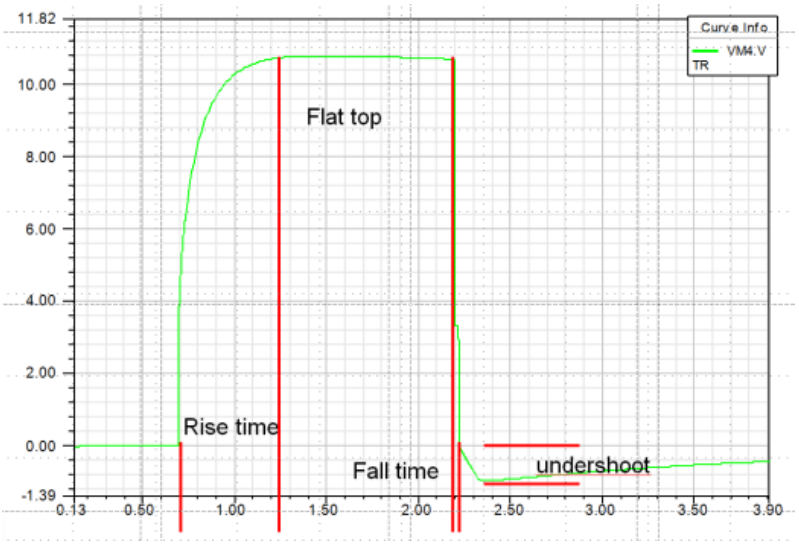

Fig. 7: Definitions of the output pulse

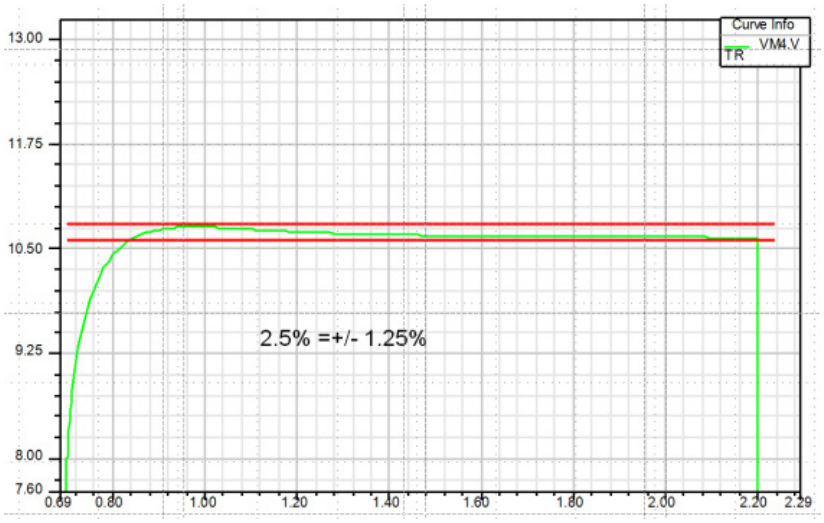

Fig. 8: Definition of flat top

4 Modulator basics

There are different modulator topologies. To understand the principle of modulators, in the following sections a bouncer modulator will be built step-by-step and real examples will be given. For the calculations the klystron data and the requirements for the XFEL are taken. The design pulse length for the hardware was chosen to be 1.7 ms.

4.1 Direct switching

A modulator contains energy storage. From this storage the energy is supplied to the klystron. The electrical component for storing energy is a capacitor. The simplest circuit for a modulator corresponds to the schematic shown in Fig. 9.

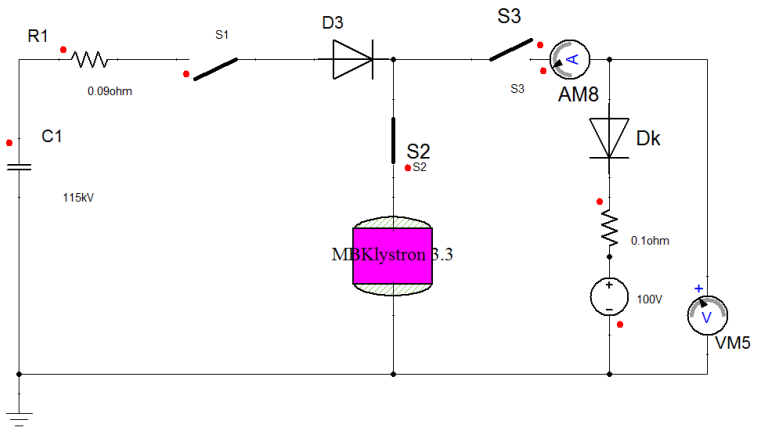

Fig. 9: Direct switching modulator

The voltage is 115 kV. As soon as switch S1 closes, a current flows in the klystron. The klystron at this voltage is equivalent to a resistor of 900 Ω, as shown in Fig. 4. During the pulse the voltage at the capacitor decreases, with an exponential decay of the RC discharge curve.

The advantage of a direct-switching modulator is the small number of components; however, the HV capacitor bank and the HV switch are problematic. There are very few suppliers of such a switch. Additionally, the stored energy in the system is very high, as shown in the following calculation.

Assuming the design values of the XFEL pulse (1.7 ms) with a flat top of 0.5%,

$$U = U_0 \times \mathrm{e}^{-\frac{t}{RC}} \tag{4}$$

where U_0 = 115 kV, R = 900 Ω and t = 1.7 ms,

$$\Delta U = 0.5\% = 0.005 \tag{5}$$

$$0.995 = \mathrm{e}^{-\frac{t}{RC}} \tag{6}$$

$$\ln(0.995) = -t/RC \tag{7}$$

$$C = -t/(R \times \ln(0.995) \tag{8}$$

$$C = 377\ \mu F\ . \tag{9}$$

For the stored energy of the capacitor,

$$E_{\mathrm{stored}} = \frac{1}{2} \times C \times U^2 \tag{10}$$

$$E_{\mathrm{stored}} = \frac{1}{2} \times 377\ \mu\mathrm{F} \times 115\ \mathrm{kV}^2 \tag{11}$$

$$E_{\mathrm{stored}} = 2491.8\ \mathrm{kJ}\ . \tag{12}$$

To calculate the pulse energy, the pulse is simplified to a rectangular waveform,

$$E_{\mathrm{pulse}} = U \times I \times t = \frac{U^2}{R} \times t \tag{13}$$

$$E_{\text{pulse}} = \frac{115\ \text{kV}^2}{900\ \Omega} \times 1.7\ \text{ms} \tag{14}$$

$$E_{\text{pulse}} = 24.98\ \text{kJ}\ . \tag{15}$$

The ratio between $E_{\text{pulse}}/E_{\text{stored}}$ is a factor of 100. It is obvious that this solution will be much too expensive for a series of modulators.

With reduced requirements this modulator type was realized for the ISIS front-end test stand [3]. The direct-switching modulator was built by Diversified Technologies, Inc, USA (Fig. 10).

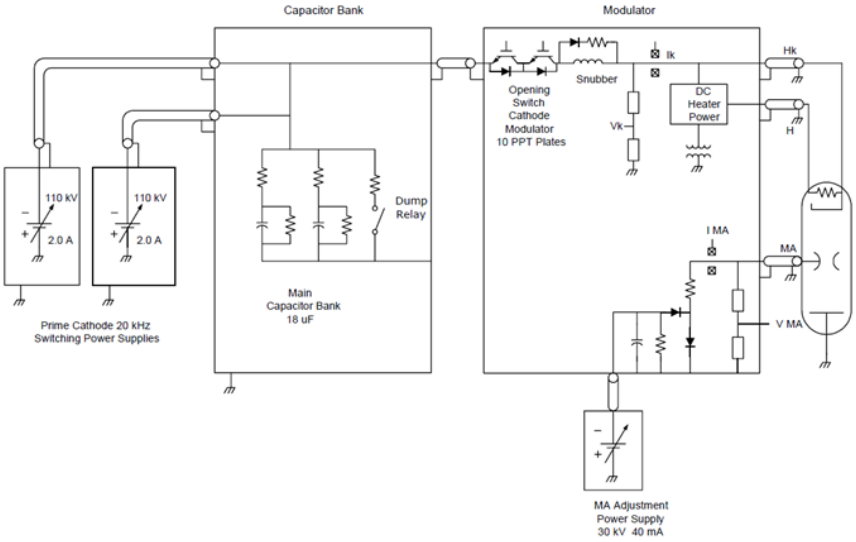

Fig. 10: ISIS test stand modulator [3]

4.1.1 ISIS modulator specifications

Table 3 contains the specifications for the ISIS modulator.

Table 3: ISIS modulator specifications

Parameter	Value
Cathode voltage	−110 kV
Cathode current	45 A
PRF	50 Hz
Beam pulse width	500 µs to 2.0 ms
Droop	5%

4.2 Modulator with pulse transformer

Since the design of a high-voltage switch is demanding, pulse transformer solutions were developed. A schematic is shown in Fig. 11. The primary voltage may be chosen freely, since the transformer will adapt to the required high voltage. For XFEL, 10 kV was chosen. Medium-voltage switches can be built more easily by stacking semiconductors. The first FNAL modulator used gate turn-off thyristors (GTOs), the next ones changed to insulated gate bi-polar transistors (IGBTs), and currently integrated gate-commutated thyristors (IGCTs) are used. Components that are able to handle voltages up to 6.5 kV are currently on the market. The semiconductor switch can be built without oil, but the pulse transformer has still to be under oil.

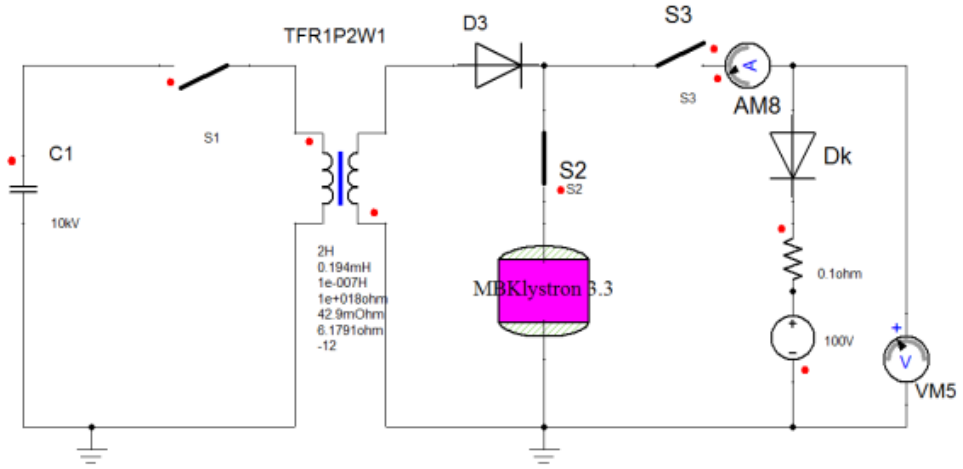

Fig. 11: Modulator with pulse transformer

The disadvantages are the volume and weight of the transformer. The additional leakage inductances increase the rise time, and even more energy is stored in the system, which has to be dissipated in the event of an arc.

According to the equivalent circuit for a transformer (Fig. 12) several inductances can store energy during the pulse. The stray inductances carry the main pulse current and short-circuit current of up to 2000 A, whereby the main inductance is loaded by the applied voltage of 10 kV. The stored energy is maximal at the end of the pulse.

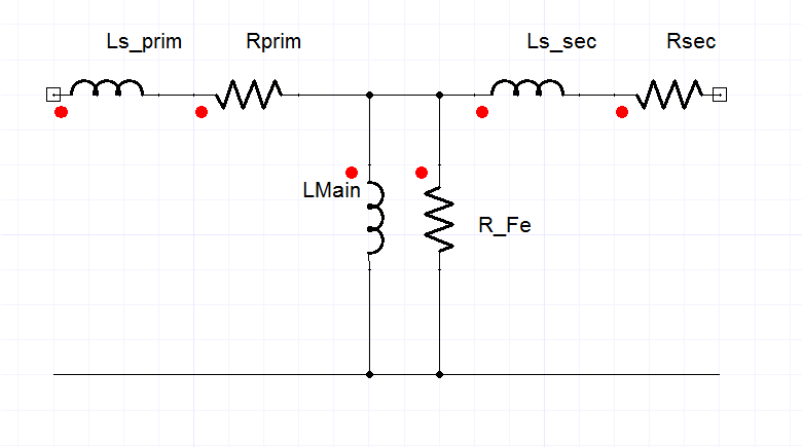

Fig. 12: Equivalent circuit for a transformer

Stored energy in the stray inductances are given by

$$E_{\text{stored Ls}} = \frac{1}{2} \times Ls \times I_{\text{short circuit}}{}^{2}\,, \tag{16}$$

where L_s for the XFEL transformer = 200 µH,

$$E_{\text{stored Ls}} = \frac{1}{2} \times 200\ \mu\text{H} \times 2000\ \text{A}^2\,, \tag{17}$$

$$E_{\text{stored Ls}} = 400\,J\,, \tag{18}$$

and the stored energy in the main inductance is given by

$$E_{\text{stored LM}} = \frac{1}{2} \times L \times {I_{\text{main}}}^2 \tag{19}$$

L_{Main} of the XFEL transformer = 5 H,

$$I_{\text{Main}} = \frac{U \times t}{L}, \tag{20}$$

and U = 10 kV, t = time of arc 0–1.7ms,

$$I_{\text{Mainmax}} = \frac{10\ \text{kV} \times 1.7\ \text{ms}}{5\ \text{H}} = 3.4\ \text{A}, \tag{21}$$

$$E_{\text{stored LM}} = \frac{1}{2} \times 5\ \text{H} \times 3.4\ \text{A}^2 = 28.9\ \text{J}. \tag{22}$$

In total, 428.9 J are stored in the transformer. The energy deposited in the klystron has to stay below 20 J. Therefore, a pulse transformer demands the introduction of the possibility of discharging. A simple circuit such as an RCD network as shown in Fig. 13 comprising Rvar, R8, C3 and a diode. For energy dissipation the resistance of the secondary winding also has to be taken into account.

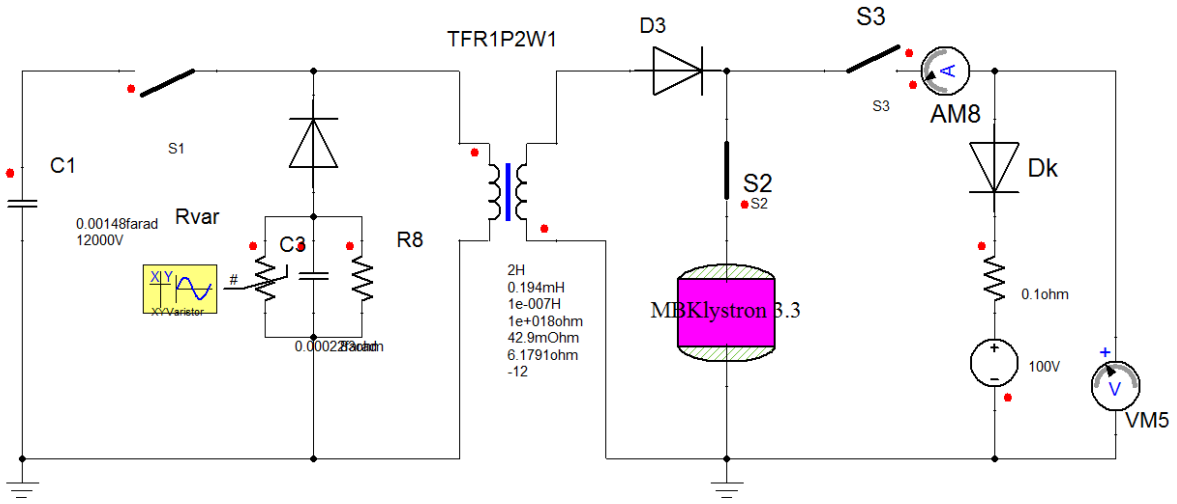

Fig. 13: Modulator with pulse transformer with discharge network

Note that the introduction of the pulse transformer does not affect the calculation of the stored energy inside the modulator. Only the voltage levels at the capacitor bank and the semiconductor have changed.

4.3 Bouncer modulator

To decrease stored energy, the bouncer modulator was developed at Fermi Lab [1]. An LC ringing circuit was introduced into the circuit as shown in Fig. 14. It compensates for the voltage droop at the capacitor bank during the pulse; Kirchhoff's law explains this behaviour. The sum of all voltages in a circuit equals zero. The voltage at the input of the pulse transformer plus bouncer voltage is equal to the capacitor voltage. If capacitor voltage and bouncer voltage now decrease by the same amount, the transformer voltage stays constant, as shown in Figs. 15 and 16.

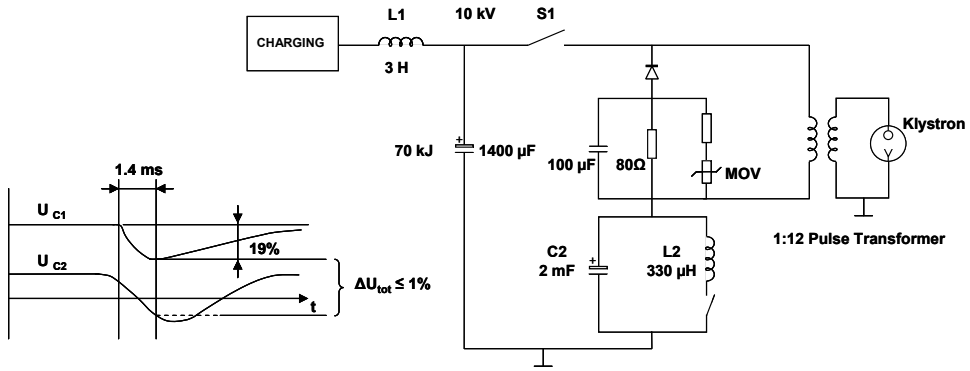

Fig. 14: Bouncer modulator

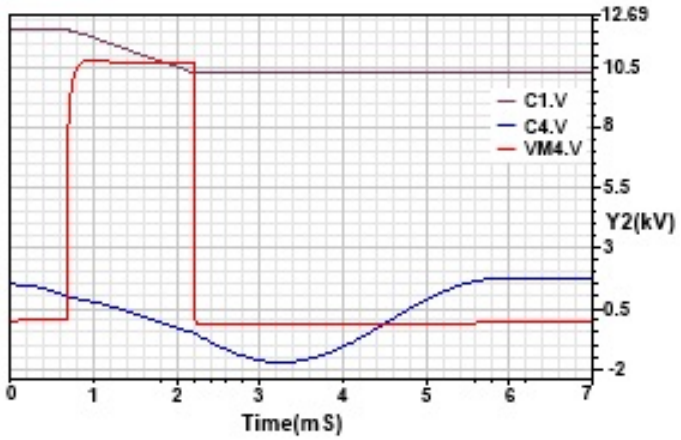

Fig. 15: Voltage waveforms in a bouncer modulator. Red: voltage at the transformer; violet, capacitor bank voltage; blue, bouncer cap voltage.

Since the capacitor voltage droop is an exponential decay and the bouncer oscillates with a cosine waveform, the voltages do not droop completely equally, leaving a ripple on the flat top as shown in Fig. 16.

This ripple is adjustable by the dimensioning of the bouncer elements, the timing between the main switch and bouncer switch and the voltage of the bouncer.

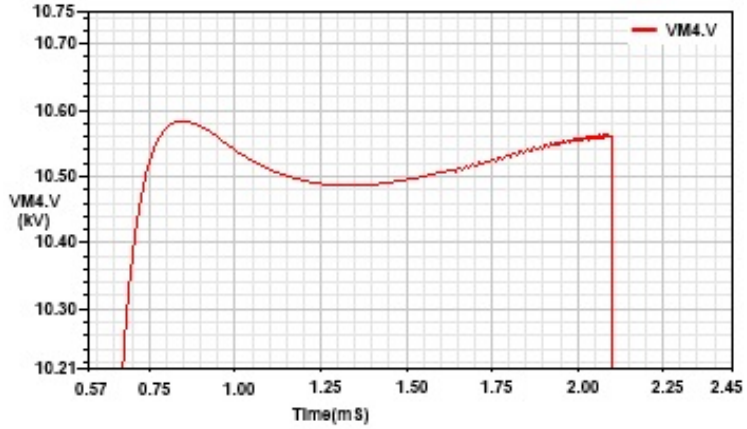

Fig. 16: Voltage ripple at the flat top of a bouncer modulator

To see the advantage of the bouncer principle, a calculation of the stored energy is given below. The stored energy in the modulator is:

Main capacitor energy:

$$E_{\text{stored}} = \frac{1}{2} \times C_{\text{main}} \times U^2 \,, \tag{23}$$

$$E_{\text{stored}} = \frac{1}{2} \times 1.4\ \text{mF} \times 10\ \text{kV}^2 \,, \tag{24}$$

$$E_{\text{stored}} = 70\ \text{kJ} \,. \tag{25}$$

Bouncer energy:

$$E_{\text{bouncer}} = \frac{1}{2} \times C_{\text{bouncer}} \times {U_{\text{bouncer}}}^2 \,, \tag{26}$$

$$E_{\text{bouncer}} = \frac{1}{2} \times 2\ \text{mF} \times 2\ \text{kV}^2 \,, \tag{27}$$

$$E_{\text{bouncer}} = 4\ \text{kJ} \,. \tag{28}$$

The sum is 74 kJ, which is only five times the pulse energy.

The first three bouncer modulators were built by FNAL and operated at DESY. At DESY further research and development was done and the modulator was brought to industry. The following modulators were built by Puls-Plasmatechnik GmbH (PPT), Germany, the nowadays Ampegon PPT GmbH [4] and are operated with the FLASH accelerator and test stands for the XFEL. Improvements were made for reducing EMI basically by improving the construction e.g. using sandwich structures for the current leads. A constant power charging of the capacitor bank as described in section 6 was introduced. The bouncer changed position to the high-voltage side. Because of this the pulse transformer primary stays at ground potential. In accordance with Kirchhoff's law the position of the different voltages does not influence the transformer voltage.

A disadvantage of the bouncer is the high current cycling in the LC network. Additionally, a new time-dependence of the triggering of the switch is introduced.

The bouncer principle was later also proposed by other enterprises such as, for example, JEMA, Spain [5] (Fig. 17). Here the single-pulse transformer is split into several smaller primary windings and one secondary winding. This approach takes advantage of the low energy storage due to the bouncer principle. Due to the splitting of the primaries the semiconductor switches do not have to handle the high pulse current. Also, the lower stray inductances in each branch result in a better rise time of the pulse.

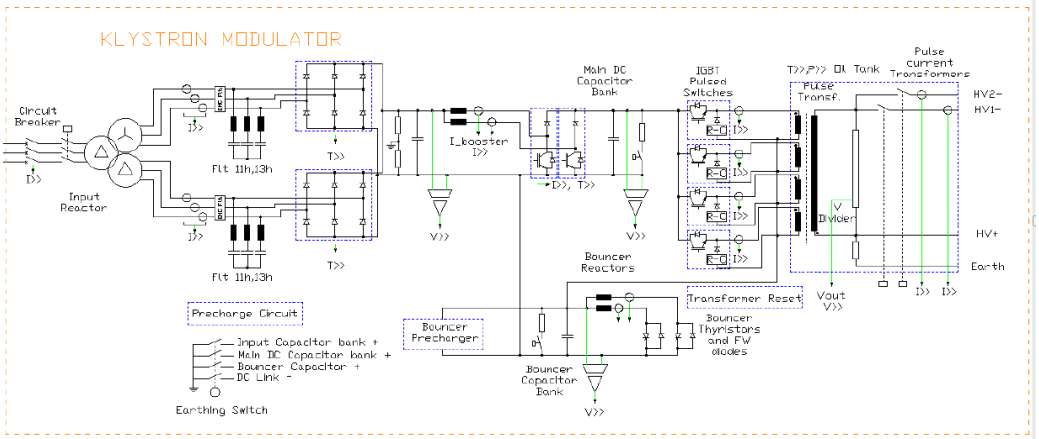

Fig. 17: Proposal for a klystron modulator by JEMA, using the bouncer principle

4.4 Active bouncer solutions

To further decrease the remaining ringing of the flat top using the LC bouncer, switched mode power supplies can be introduced. Here, high-frequency switching semiconductors have to be used. The development shown in Fig. 18 was done at CERN [6]. This topology was tested as a prototype and tests are ongoing. Other topologies for switched mode supplies are also possible.

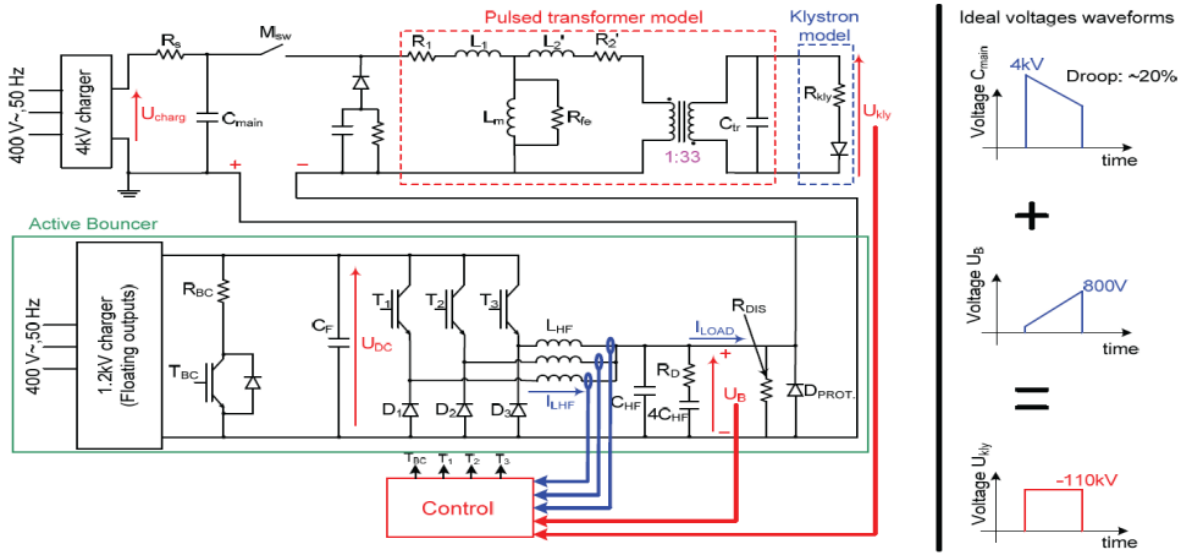

Fig. 18: Active bouncer solution tested at CERN [6]

4.5 Pulse forming by LC circuit

Another passive pulse-forming topology, instead of a LC bouncer, is an LR circuit, as shown in Fig. 19. Here time-dependent current flow in the inductance during the pulse is used. At the beginning of the pulse, the inductance has a high impedance. The current flows through the resistor having an initial voltage drop. During the pulse the current commutates into the inductance, which short-circuits the resistor. This solution is built by Scandinova, Sweden and PPT, Germany. In Fig. 20 the schematic for a Scandinova modulator is presented.

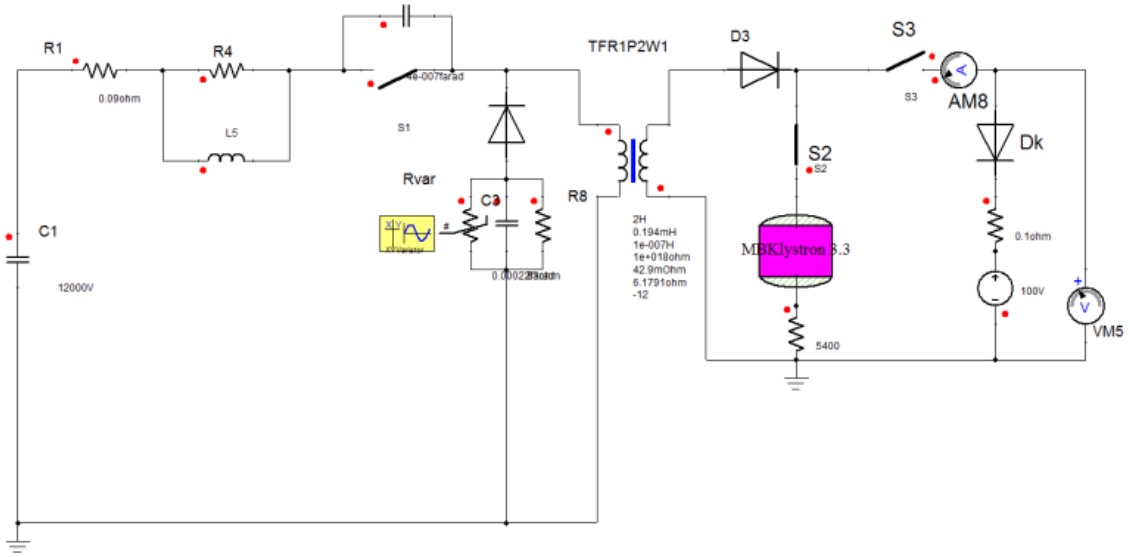

Fig. 19: Pulse forming by LR network

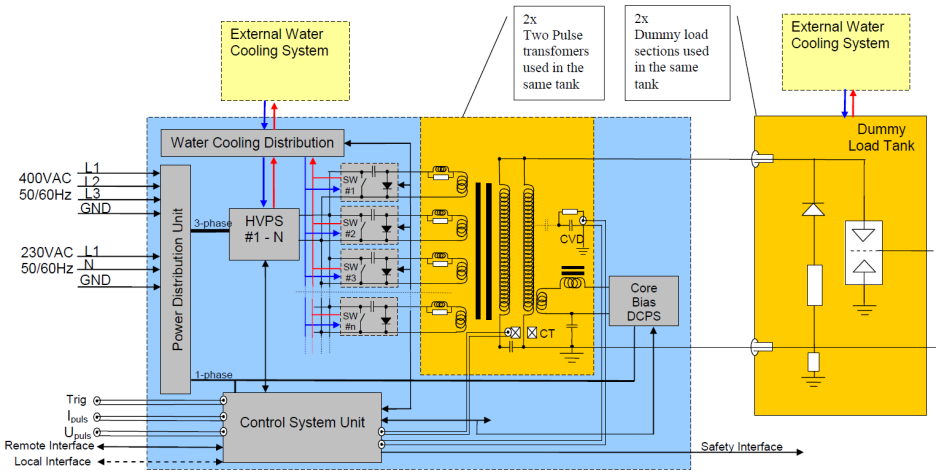

Fig. 20: Modulator with LR pulse-forming network

The advantage of the LR is definitely its simplicity. Once the LR circuit is optimized it does not require any further timing signals. However, it is also less flexible than the bouncer, where over a small range some changes in pulse shaping are possible. The additional losses in the resistor have to be taken into account for the efficiency calculation.

5 Modulators with switched mode power supplies

The development of better semiconductors and transformers has led to different solutions for modulators using switched mode power supplies for pulse generation. In this section three solutions are presented. These modulators are either already installed or prototypes have been proven to work.

5.1 Pulse step modulator

This technology was developed by Ampegon, Turgi, Switzerland [7, 8]. The original application was for shortwave transmitters to produce amplitude-modulated signals. A rectangular pulse is 'just' a special waveform that can be produced with this topology.

In the modulators, several voltage sources are stacked in series, as shown in Fig. 21. By means of appropriate regulation and time pattern the voltage sources are turned on to produce the required waveform.

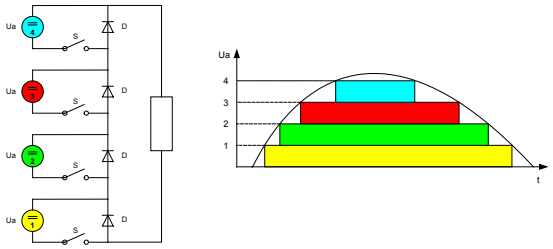

Fig. 21: Principle of the pulse step modulator

As shown in Fig. 21, the simple turning on and off of the voltage source would lead to a large quantification error. This is well known from digital signal processing. To achieve a more precise adaptation of the desired wave form, switched mode supplies are used. The principle shown in Fig. 22 is also described in Ref. [9].

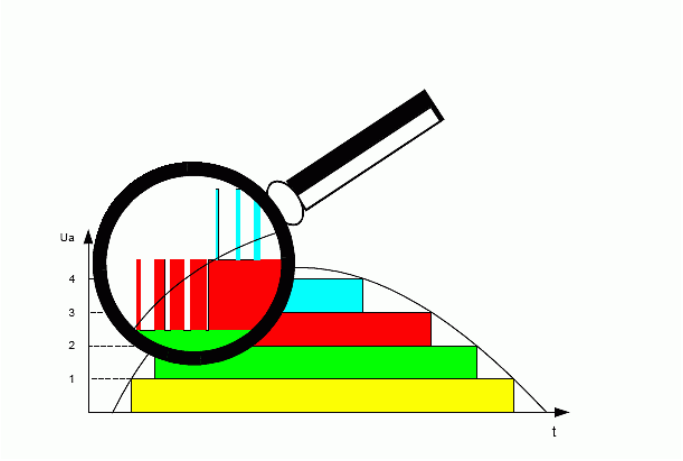

Fig. 22: Use of switched mode supplies to better shape the wave form

A complete RF station is presented in Fig. 23. The stacked voltage sources are built next to the switching modules. A low-pass filter is introduced to decrease the voltage ripple and suppress the switching frequency at the output of the modulator.

Specific to DESY is the use of pulse cables to transport the pulses from the modulator to the pulse transformer and klystron. The length of these cables is up to 1.7 km [10].

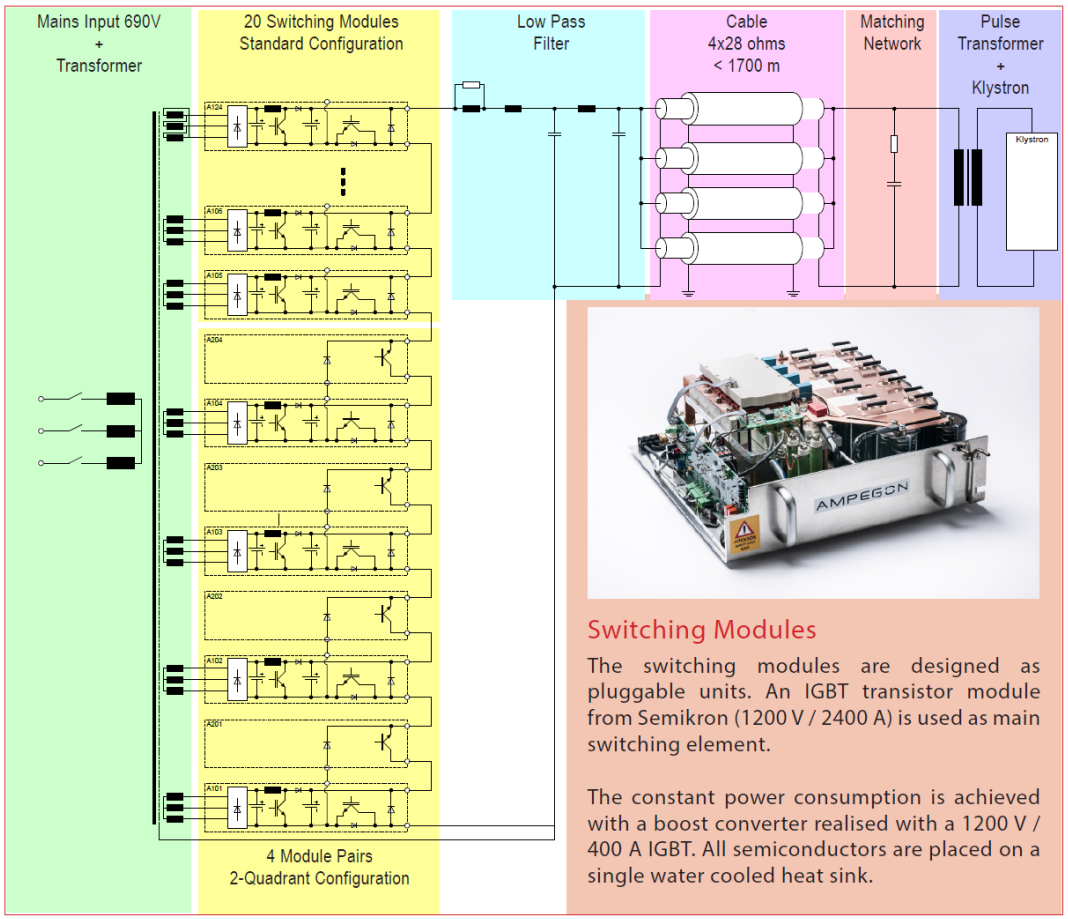

Fig. 23: Schematic of the RF station with Ampegon modulator [8]

The waveform of the klystron current and voltage, as well as the modulator current and voltage are shown in Fig. 24. The rise time is approximately 200 µs.

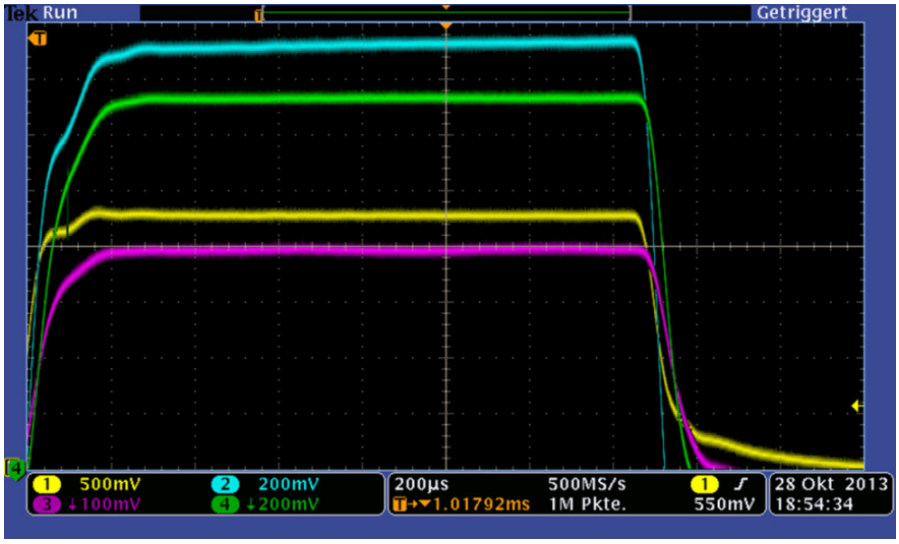

Fig. 24: Current waveforms of the Ampegon modulator. Yellow: modulator voltage (9kV), light blue: modulator current (1500A), pink: Klystron voltage (108 kV), green: Klystron current (125A).

The flat top is measured to be 30 V_{pp} on a 10 kV pulse. This corresponds to 0.3% pp, which is a very good result and stays within the specification. The measurement is shown in Fig. 25.

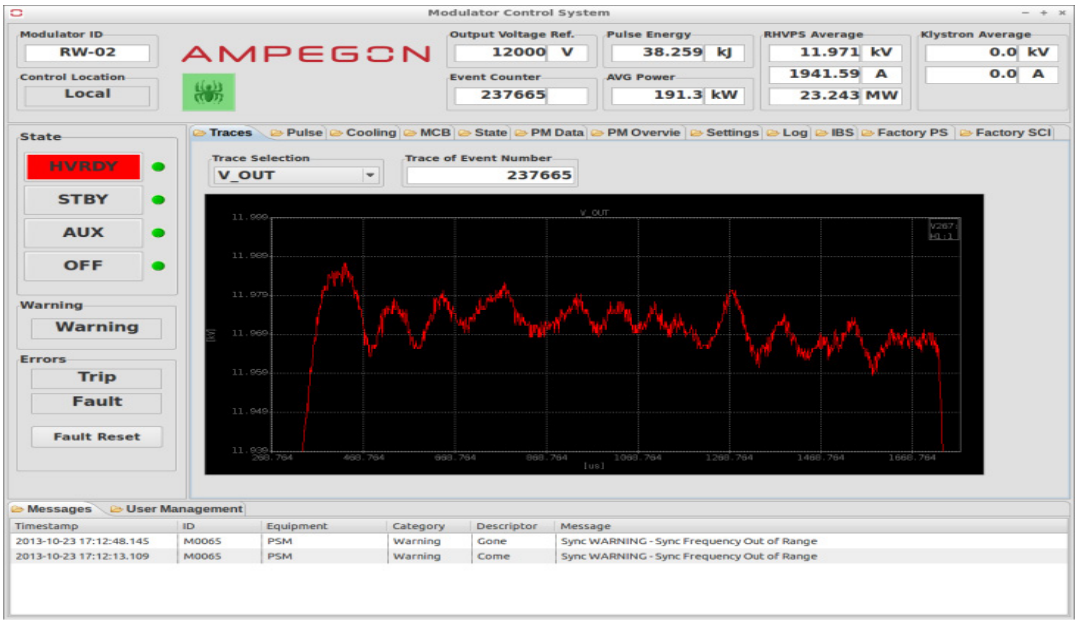

Fig. 25: Flat top measurement for the XFEL modulator

5.2 H-bridge converter/modulator

The topology chosen for the SNS modulator was H-bridge topology with interleaved switching pattern (Fig. 26); see Ref. [11]. For the input stage a three-phase SCR controller supplies a DC intermediate circuit. Via multiphase IGBT H-bridges, transformers and a secondary diode rectifier, 135 kV is generated. The switching frequency of the IGBTs is 20 kHz. The peak power is up to 11 MW with an operating repetition rate of 60 Hz at a pulse length of 1.35 ms. Figure 27 shows the modulator assembly.

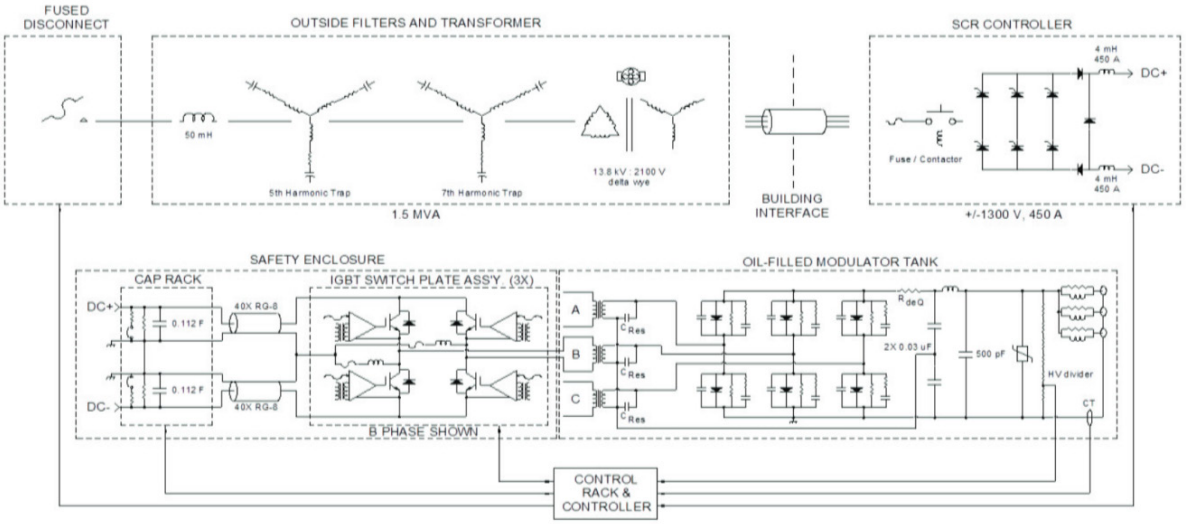

Fig. 26: Multiphase H-bridge SNS modulator

Fig. 27: SNS modulator assembly

5.3 Marx modulator

The principle of producing high voltage by using a Marx generator is well known. The parallel charging of high-voltage cells at a low voltage and then switching these in series was described in the 1920s. At SLAC this principle was used to build a modulator. The modulator is divided into modules that are loaded at low voltage [12]. During the pulse the modules are connected in series. Figure 28 presents the schematic of the modulator. An additional droop compensation circuit regulates the flat top to compensate for the storage capacitor voltage droop (Fig. 29).

This modulator was built as a prototype with full power and voltage.

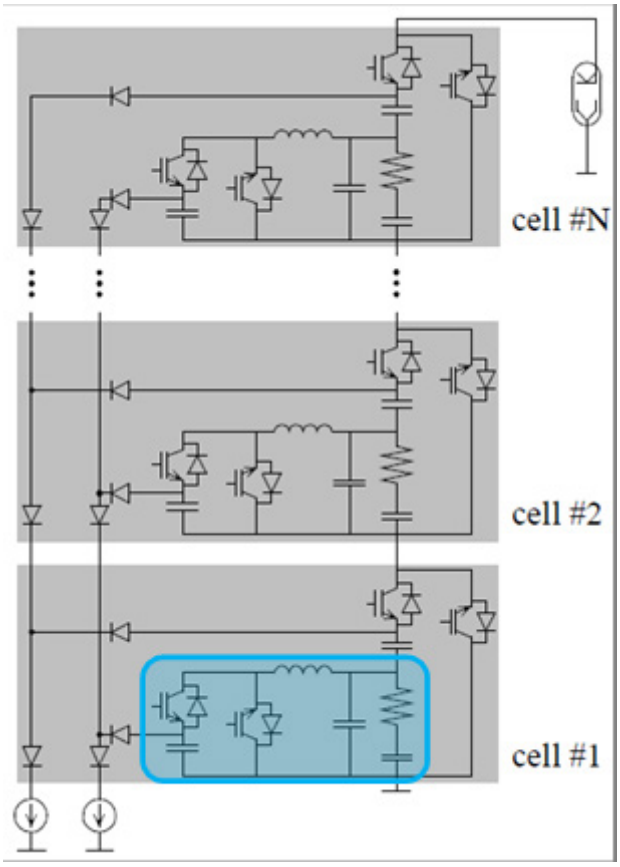

Fig. 28: Schematic of Marx modulator

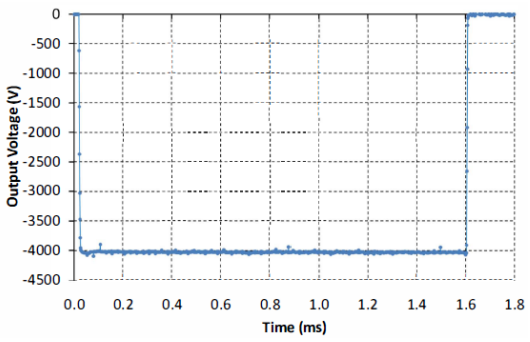

Fig. 29: Waveform for one cell

6 Connecting modulators to the electrical grid

By means of capacitors modulators constantly draw electrical energy from the mains to supply pulsed output power. As an example, the bouncer modulator is shown in Fig. 30. During the pause between pulses this energy has to be recharged. Figure 31 shows the waveform of the capacitor voltage of a bouncer modulator in pulsed operation. Recharging this circuit with either a diode rectifier or SCR rectifier would draw high peak currents, and therefore high peak power from the mains, leading to severe disturbances to the grid.

The first modulator installed at DESY used a SCR primary regulated charging unit. The pulsing of this one modulator could be measured at the ppm level in the HERA magnet power supplies. It is

easy to imagine that a large number of modulators, as at XFEL with an integrated pulse power of 450 MW, cannot be connected to the grid without taking special care for compensation.

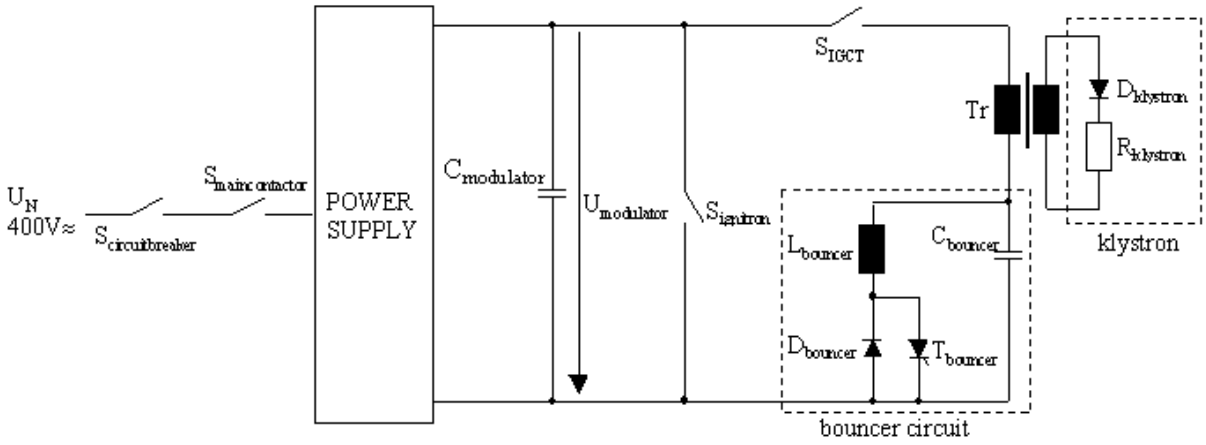

Fig. 30: Topology of the bouncer modulator; energy is stored in the main capacitor bank

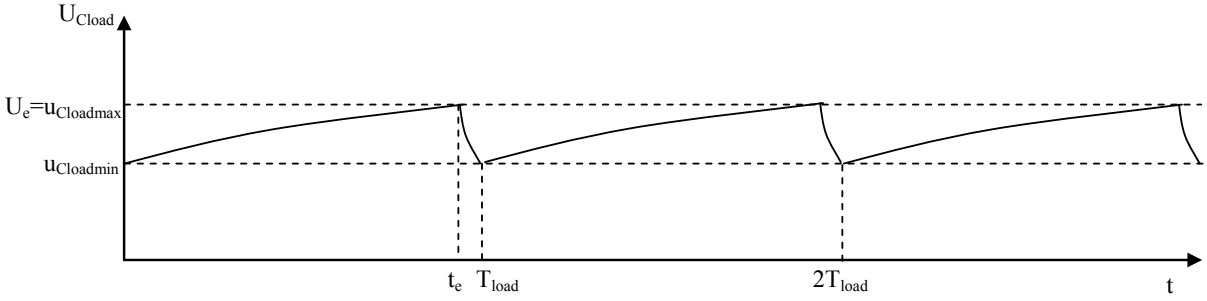

Fig. 31: Voltage waveform of the main capacitor bank

To prevent disturbing the consumers connected to the mains, the level of allowed disturbance is defined in the German standard VDE 0838, IEC 38 or the equivalent European standard EN 61000-3-3. In general, no consumer is allowed to produce more distortion than 3% of the voltage variation of the mains. At the low frequencies at which the distortion can be seen as a fluctuation in the intensity of lighting, these disturbances are even more restricted. At these frequencies, the human eye is very sensitive to changes in light intensities. The eye sees a flickering, which gives the name 'flicker frequencies'. Figure 32 shows the maximum grid distortion as a function of voltage changes per minute. It is important to understand that the definition is voltage changes per minute. A pulse would be represented by a negative voltage change and then a positive voltage change. Therefore the double repetition rate has to be taken as

$$\Delta U/\mathrm{min} = 2\times f_{\mathrm{rep}}\ [1/\mathrm{s}]\times 60\ [\mathrm{s/min}]\ . \tag{29}$$

In order to fulfil the required standard a constant power loading for the modulator was developed. The power of the modulator has to be

$$P = U \times I = \mathrm{const}\ ! \tag{30}$$

The current has to be regulated according to Eq. (30), to be the inverse of the ΔU that occurs during pulsing. If U decreases the current has to be increased by the same ratio.

It has to be taken into account that an SCR bridge generates reactive power dependent on the firing phase angle; therefore, these are not suitable. Instead either a diode bridge rectifier with intermediate DC link or active front-ends with self-commutated converters have to be used.

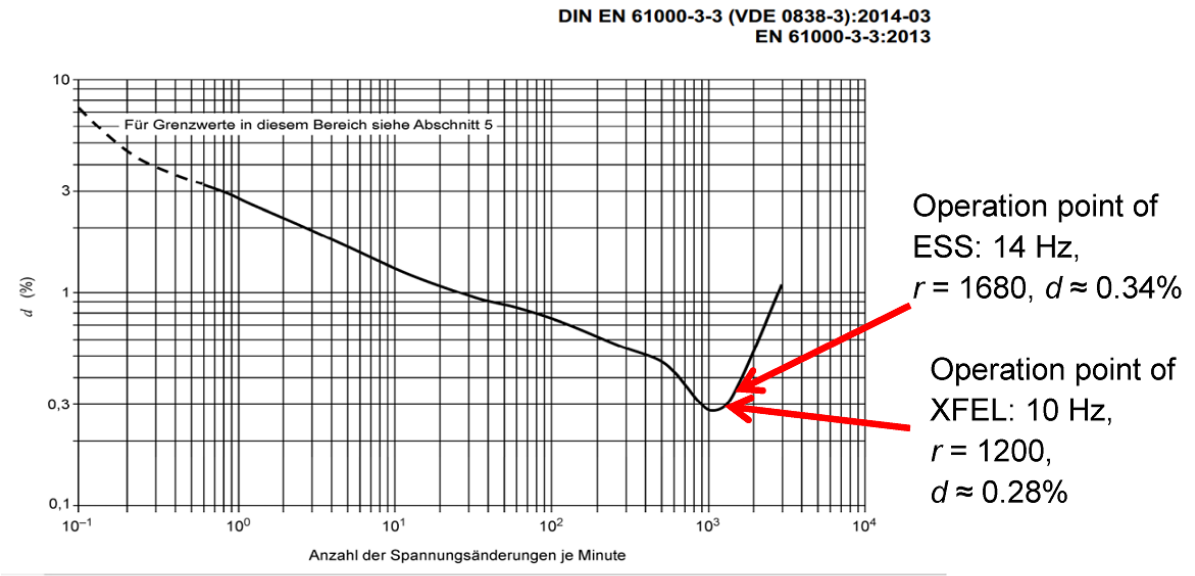

Fig. 32: Number of voltage changes per minute with allowed amount of distortion

6.1 DESY mains specification and specification of the modulator

Unfortunately, particle accelerators are using repetition rates that are close to the frequency of minimum of allowed distortion. The XFEL is operated at 10 Hz, giving 1200 voltage changes. According to Fig. 32, $d = 0.28\%$. The found value of d defines the actual allowed power changes (ΔP)/modulator. Here, d is defined by the equation

$$d = \frac{\Delta S}{S_{sc}} = \frac{\Delta U}{U_{\mathrm{nom}}} = 0.28\% \tag{31}$$

where d is allowed distortions, ΔS is the variation in apparent power, S_{sc} is the short-circuit power of the mains and U_{nom} is the nominal voltage of the mains

At DESY the intermediate voltage is 10 kV. The short-circuit power of the mains station to which the modulators are connected to, is 250 MVA. The allowed power variation is:

$$250\ \mathrm{MVA} \times 0.28\% = 700\ \mathrm{kVA}\ . \tag{32}$$

In the design, including future upgrades, the number of XFEL modulators is set to 35. This would allow 20 kVA/modulator deviations to fulfil the requirement of the grid operator.

Since other components in the machine are assumed to be more critical than the human eye, the budget was cut by two. A value for the specification of 10 kVA/modulator was defined, a challenging, but not impossible value.

6.2 Different power supplies for constant power

The first market analysis during the middle of the 1990s showed that no constant-power power supplies were available. Capacitor charging units at that time usually provided the possibility of voltage or constant current regulation. A research and development programme was launched to make

a first prototype to cope with this problem. The result was the power supply shown in Fig. 33. This was built as a 300 kW prototype, able to supply a modulator in the test stand [9, 13].

With this topology the converter delivers a constant power into the capacitor C_{load} at a fixed switching frequency. Charging a resonant capacitor C to a *constant voltage* U_B or 0 V, by taking current from the mains, results in a *constant charge* from the mains and is independent of the load.

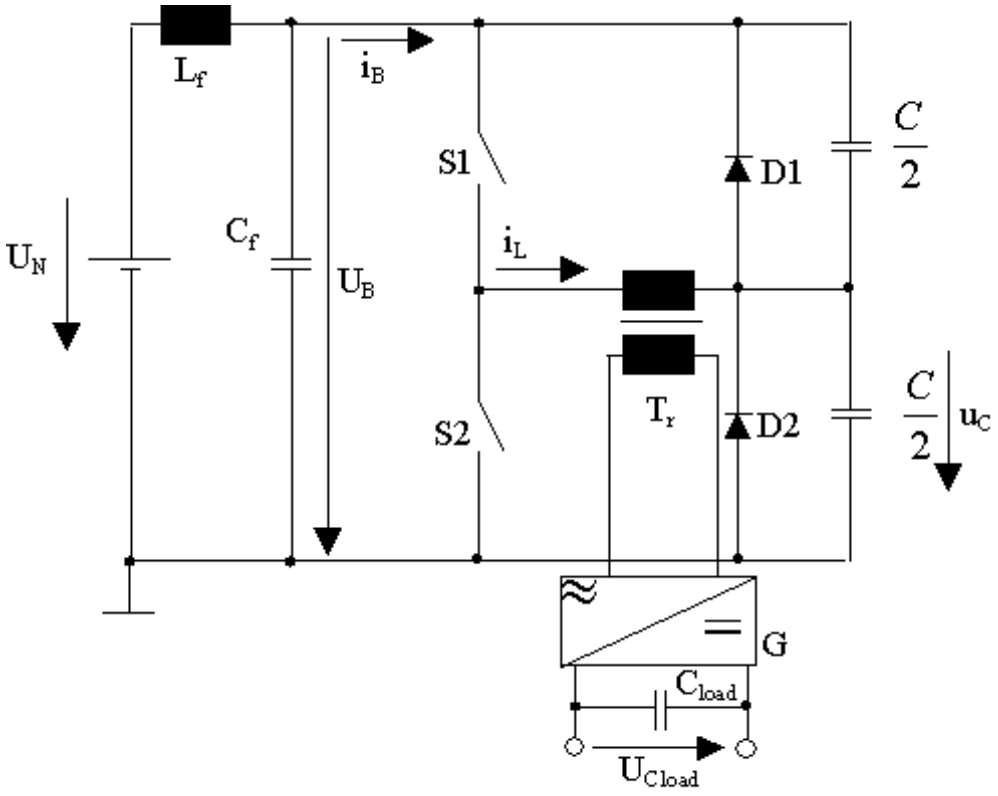

Fig. 33: First constant power power supply developed at DESY. G, rectifier; i_b, supply current; i_L, transformer primary current; u_C, resonance capacitor voltage; U_{Cload} output voltage at modulator capacitor bank; i_{Btl}, current i_B at time t_1; L, primary stray inductivity of the transformer; f, resonance frequency of the resonant LC circuit; n, gear ratio of the transformer and rectifier; T, time period of the switching frequency of S1 and S2; C, resonance capacitor; U_B, DC link supply voltage; U_N, primary rectifier voltage; C_f, DC link capacitor; L_f, filter inductance.

A very nice analogy of the working principle is the comparison with a water bucket. This bucket is filled with water per period. Afterwards it is poured into a pool. The water quantity that is poured into the pool is dependent upon the filling/pouring frequency. It is independent of the water-level of the pool.

In the tendering process, this topology was not chosen because of the price. Instead, a series combination of buck converters was shown to have a better price. The schematic can be seen in Fig. 34. It was produced by FuG, Germany. These power supplies have been working in FLASH for several years. The regulation is analog and consists of three regulation loops: voltage, current and power regulation.

During normal operation the power is regulated. In the event of too high currents or voltages these regulation loops guarantee that none of the values are exeeded. For example, the power supply stops loading when the required voltage is reached.

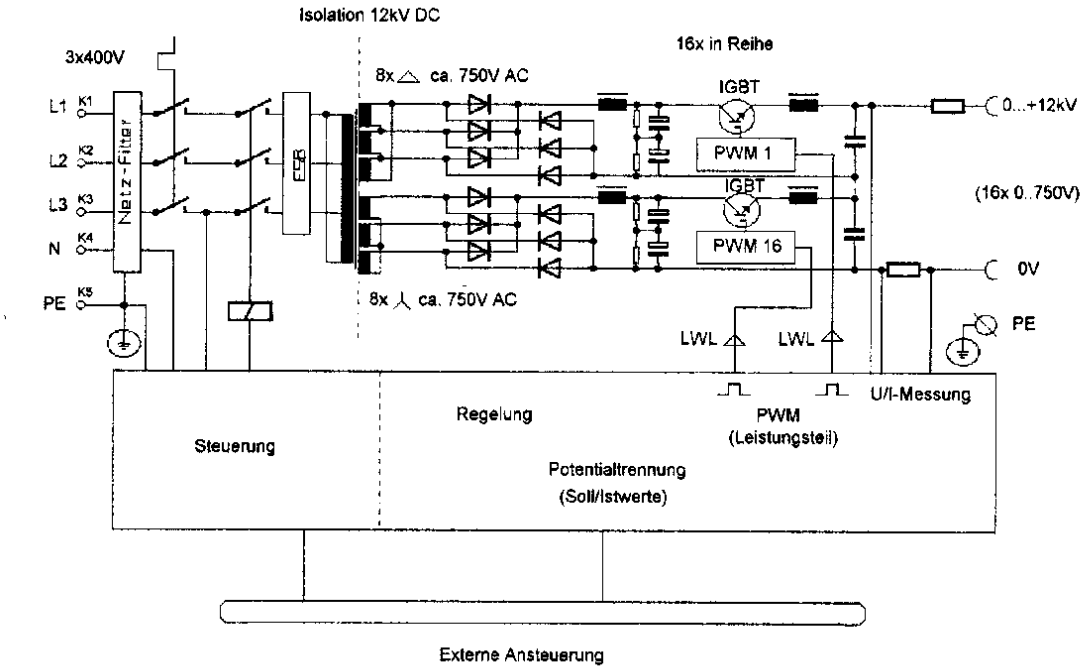

Fig. 34: Contant-power power supply using buck converters installed at FLASH

The third solution is installed in the Ampegon modulator for XFEL as shown in Fig. 35. The modules have a combined function of constant power charging (main rectifier and boost converter), energy storage in the capacitor and the pulse-forming IGBT. The boost converter is regulated in constant power mode according to Eq. (30).

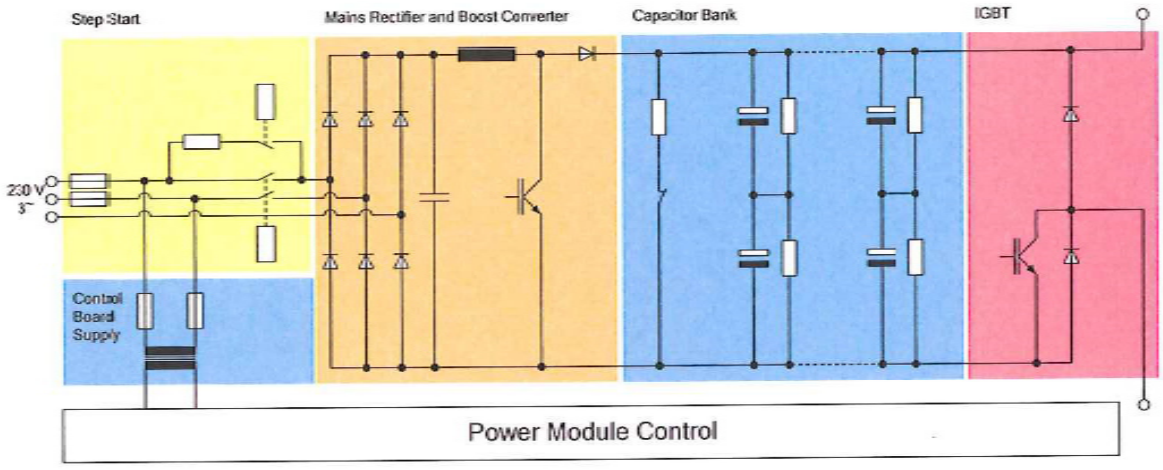

Fig. 35: Ampegon power module, combining constant power loading, energy storage and pulse IGBT

The measurement results are shown in Figs. 36 and 37. Figure 36 shows the waveform that was measured during the acceptance test. The 50 Hz fundamental wave is taken to calculate power deviation due to pulsing.

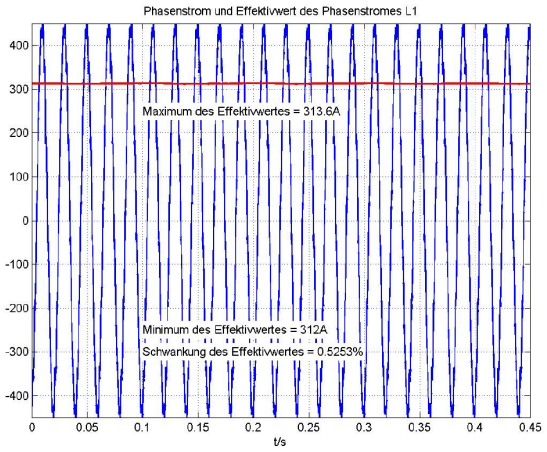

Fig. 36: 50 Hz signal with measured 10 Hz deviation

As described the specified value of power variations should be <10 kVA/modulator. This would correspond to a current variation of

$$\Delta I = \frac{\Delta S}{\sqrt{3} \times U} = \frac{10\ \text{kVA}}{\sqrt{3} \times 690\ \text{V}} = 8.4\ \text{A}\ . \tag{33}$$

The measured result shows that:

$$\Delta I = 2.5\ \text{A}\ \text{what corresponds to a}\ \ \Delta S \approx 3\ \text{kVA}\ . \tag{34}$$

The performance of the power regulation is approximately a factor of 3 better than the requirement. Figure 37 shows the measured three-phase currents of a modulator input. The typical frequencies of the diode rectifier also appear. However, no variations in the peak-to-peak values of the amplitude or frequency variations occur.

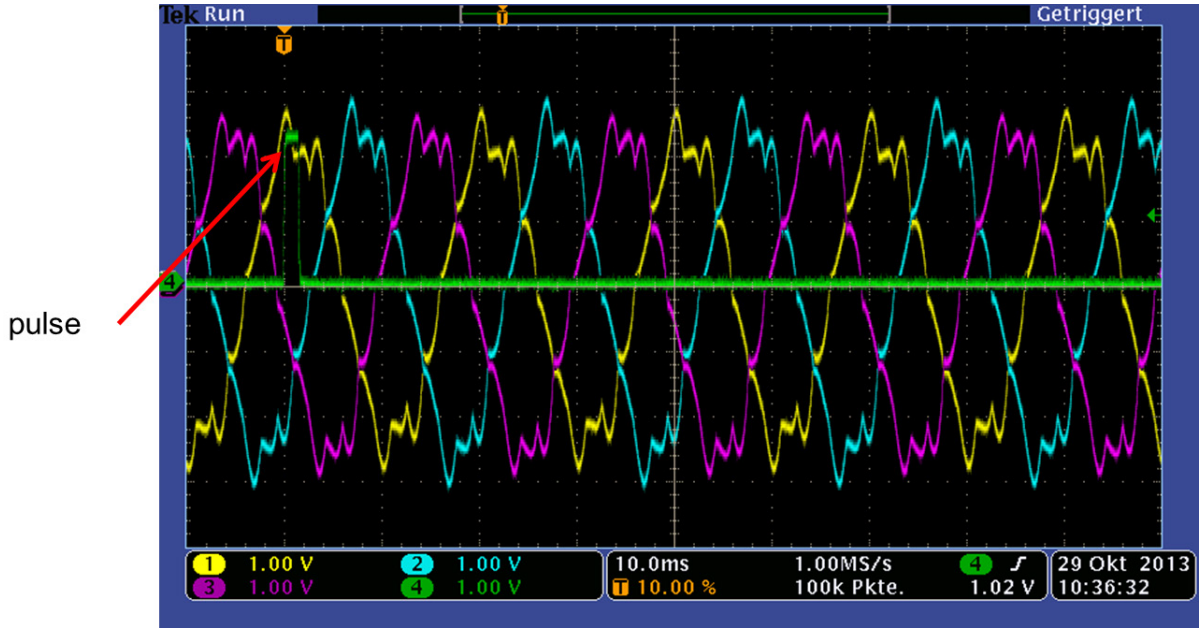

Fig. 37: Measured input current; waveform is not influenced by the modulator pulse. Yellow, light blue, pink: line currents of modulator (270A). Green: HV-pulse (9kV).

7 EMI aspects

In the pulsed modulator applications one deals with high voltage and high currents that are switched at high dV/dt and di/dt values. It is obvious that it is extremely important to start, from the very beginning, building in features that minimize EMI.

Presenting a complete overview of correct EMI construction in this paper is not possible. Only a few very basic hints are given:

- think in currents instead of voltages: find the paths where the return current will flow;
- never think that a cable is just a conductor, it is also an inductance;
- each component can and will form a resonant circuit with its neighbour;
- put the current path and return path close together;
- use low inductive ground planes;
- read, study and put into practice the lectures by A. Charoy during this CAS and [15].

In Fig. 38 the Ampegon modulator is shown. A few additional stray components are inserted into the basic schematic. These are capacitors to ground that achieve a high dV/dt and inductances in the return paths of the high currents.

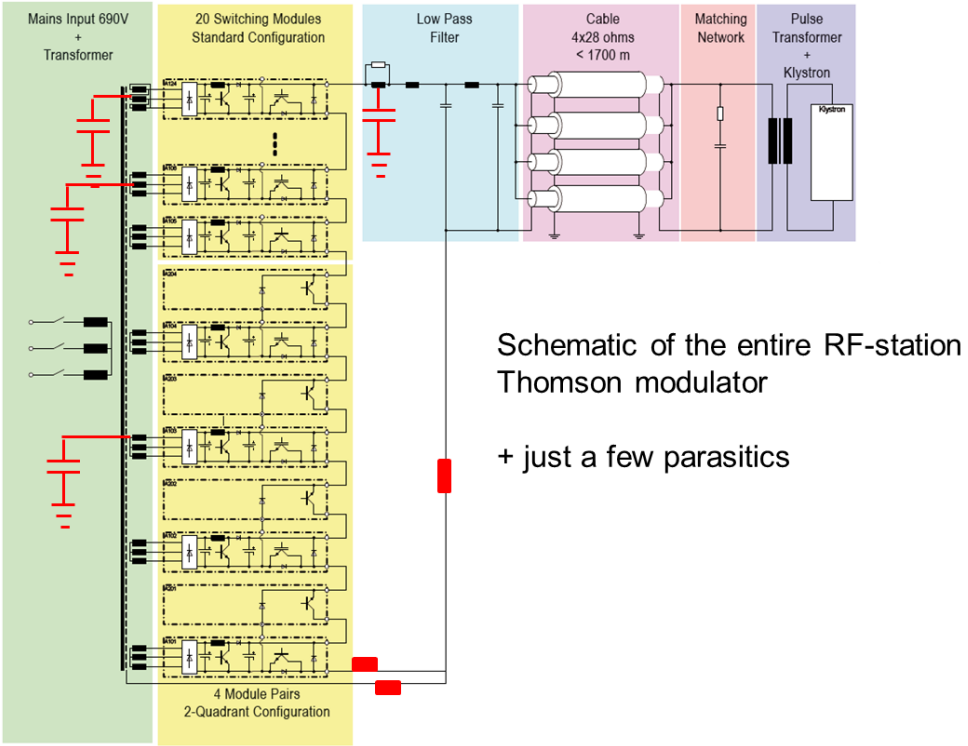

Fig. 38: Ampegon modulator with a few parasitics

Figure 39 is a simulation model of the PPT modulator for FLASH in combination with the pulse cables [14]. The circle indicates inductance L3 in the return path. The di/dt of the main pulse is transformed into a real voltage change. The inductance represents a voltage source that produces common mode currents. In Fig. 39 every component that is connected to this inductance experiences a severe change of ground potential.

Please remember: minimize the inductances in the current's return path!

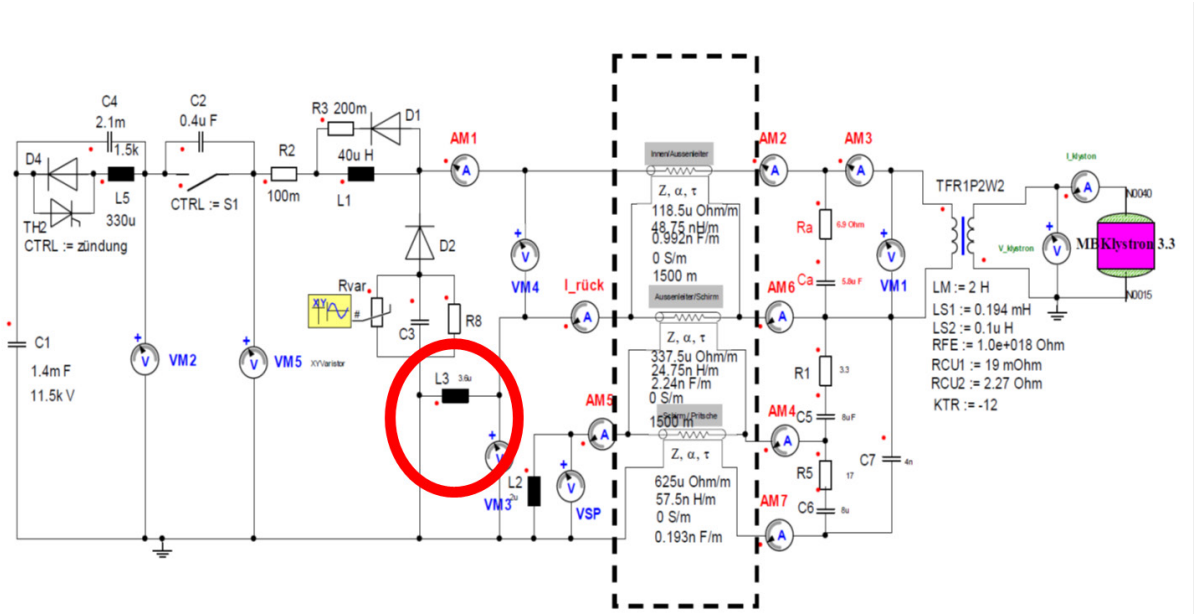

Fig. 39: Simulation model of the bouncer modulator. L3 is common mode relevant

8 Future developments

The ongoing development of semiconductors and new materials for magnetic devices allow new approaches. High switching frequencies of semiconductors are possible, and transformers are able to handles them without large losses. In general, there is a trend to modules with lower voltage at switching levels. By this the series connection of large semiconductor devices is obsolete. The large pulse transformer will be replaced by smaller high-frequency types. The advantage is that less energy is stored during the pulse, which makes klystron protection much easier.

Three types of modulators will be introduced. These are either under construction or prototypes are being built.

8.1 JEMA hybrid inverter Marx system with custom potted transformer

The first modulator is presented by JEMA [5], and is shown in Fig. 40. It is called the hybrid inverter Marx system with custom potted transformers. A primary SCR rectifier supplies a common DC bus. The SCR rectifier is only used for the soft start and loading the intermediate DC bus. Once it is loaded, the bridge is in permanent conduction mode and reacts as a diode bridge. Paralleled H-bridges installed in modules deliver the required AC waveformThe transformer consists of a primary winding and several secondary windings. . By stacking thesecondary windiings , the output HV is achieved. The switching frequency is 4 kHz. The flicker compensation in this proposal is done via the DC link reactor. The inductance would be large for small repetition rates and would have to be looked at in detail when the requirements are known.

8.2 The stacked multi-level topology

The stacked multi-level (SML) topology in Fig. 41 was proposed by C. Martins (ESS). It is in the prototyping phase in collaboration with the University of Lund.

It also works with several modules at the 1 kV level with IGBTs as semiconductor switches, operating at 16 kHz. Each module has its own transformer and rectifying unit. Several of these units are connected in series at the output, forming the HV pulse.

Each module comprises power factor correction and precise capacitor charging. Here again, constant power charging is done to reduce flicker. Energy is stored in a capacitor. An H-bridge excites a resonant circuit to supply the transformer. At the secondary winding of the transformer a rectifier with LC filter is introduced.

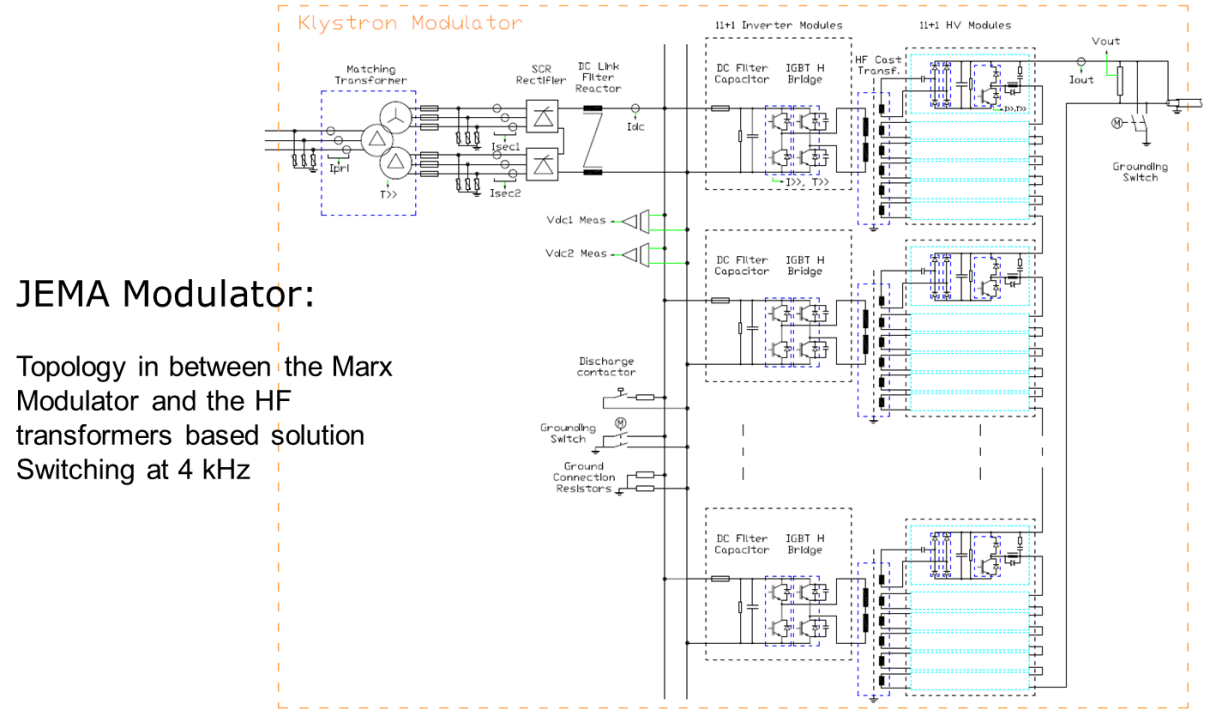

Fig. 40: Hybrid inverter Marx system with custom potted transformers

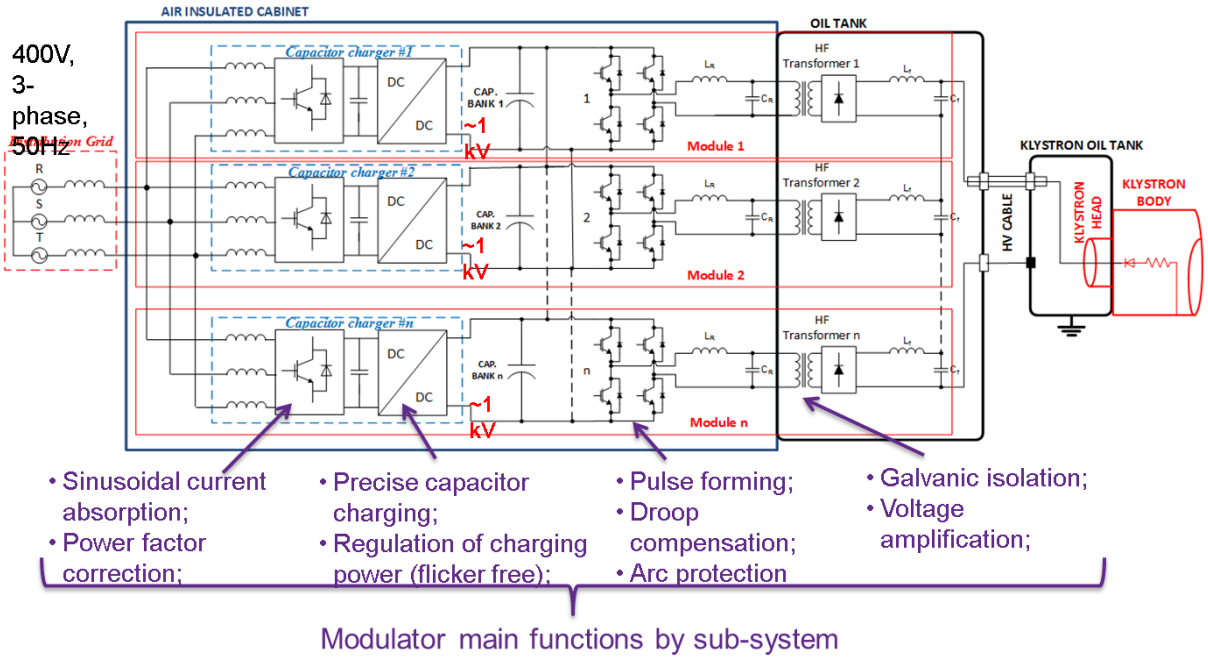

Fig. 41: Stacked multi-level (SML) topology, ESS

8.3 Ampegon proposal for ESS modulator

The last proposal is introduced by Ampegon for ESS. The basic topology of the schematic shown in Fig. 42 is very similar to the ESS SML topology. However, there are different approaches. The intermediate voltage is at 400 V. Instead of using IGBTs, metal oxide semiconductor field-effect transistors (MOSFETs) will be used, allowing a switching frequency of up to 150 kHz. This high switching frequency allows a very compact transformer, as also shown in Fig. 42.

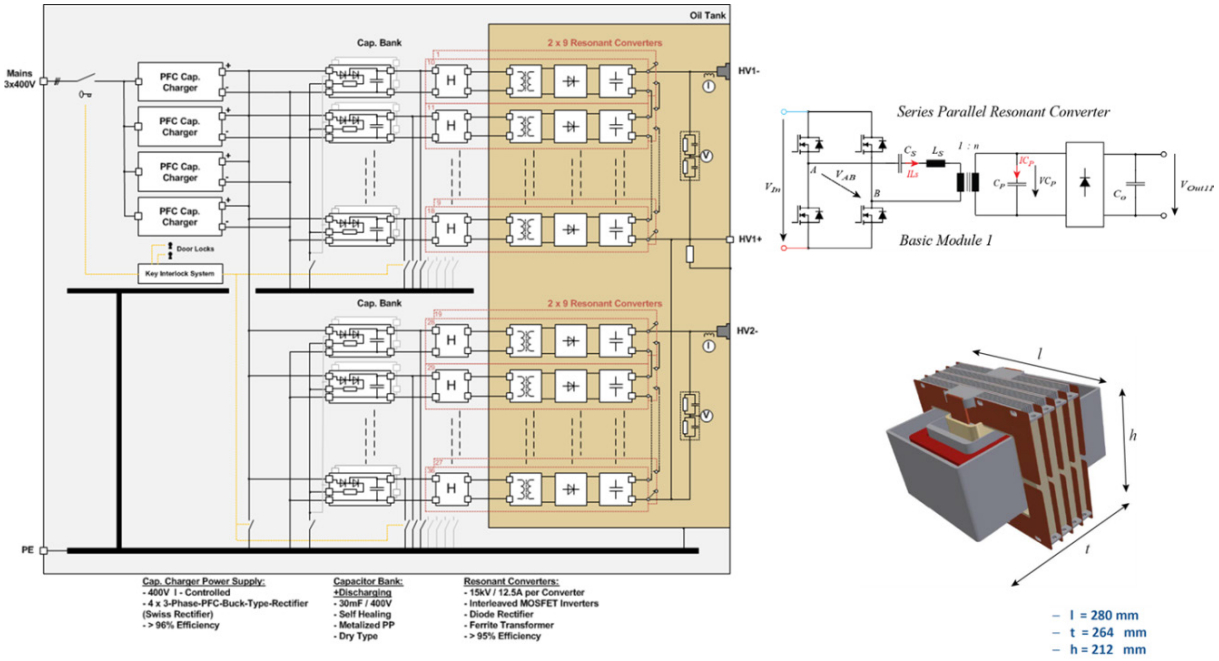

Fig. 42: Ampegon proposal for the ESS modulator with new transformer

8.4 New semiconductor technologies

Although beneficial for high voltages and fast switching, components made of silicon carbide or gallium arsenide are not yet in use. There is additional potential here for future applications.

9 Conclusions

It has been an interesting time for developments and improvements in long pulse modulators. This has been from the first idea, to prototyping, and finally to the series production of different topologies. The questions that had to be solved, ranging from the basic pulse-forming units, klystron protection and flicker rejection with a constant power loading, were solved at different accelerators. However, the improvements achieved by new technologies are still ongoing.

In the near future several large projects will use long pulse modulators. Some of these are:

- XFEL commisioning and operation;
- European Spallation Source (ESS);
- International Linear Collider (ILC);
- Project X;
- CLIC.

With the construction of modulators for these machines, power electronic engineers will have an interesting time and a lot of fun in the near future.

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Radiation Risks and Mitigation in Electronic Systems

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Abstract

Electrical and electronic systems can be disturbed by radiation-induced effects. In some cases, radiation-induced effects are of a low probability and can be ignored; however, radiation effects must be considered when designing systems that have a high mean time to failure requirement, an impact on protection, and/or higher exposure to radiation. High-energy physics power systems suffer from a combination of these effects: a high mean time to failure is required, failure can impact on protection, and the proximity of systems to accelerators increases the likelihood of radiation-induced events. This paper presents the principal radiation-induced effects, and radiation environments typical to high-energy physics. It outlines a procedure for designing and validating radiation-tolerant systems using commercial off-the-shelf components. The paper ends with a worked example of radiation-tolerant power converter controls that are being developed for the Large Hadron Collider and High Luminosity-Large Hadron Collider at CERN.

Keywords
Radiation effects; dependability; controls.

1 Introduction to radiation-induced effects

Radiation has the potential to interfere with electronic devices and systems, creating so-called radiation-induced effects [1].

At ground level, atmospheric neutrons due to cosmic rays are a primary source of radiation. Cosmic rays are high-energy particles reaching Earth from space. These interact with Earth's atmosphere, producing a shower of particles: neutrons, protons, electrons, and many others, some of which reach the Earth's surface.

In particle accelerators, *the accelerators themselves* are sources of radiation. The Large Hadron Collider (LHC) at CERN is underground, hence it is somewhat protected against cosmic radiation. In this case, the main sources of radiation are the protons in the two circulating LHC beams. These can escape from the closed beam orbit, leaving the confines of the accelerator and be lost into local materials. There are several mechanisms for beam loss:

- intentional beam losses occur, due to the collision of beam in LHC experiments;
- direct beam losses can occur, where beam strikes collimation systems or absorbers;
- beam gas interactions can occur, where circulating beam hits residual beam gas.

A single escaping proton has the potential to create a significant shower of particles that propagate from the machine into the surrounding area. To understand the effects that this can have,

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one must consider the basic metal oxide semiconductor field effect transistor (MOSFET), which is the fundamental basis of electronic systems. An N-channel MOSFET is shown in Fig. 1.

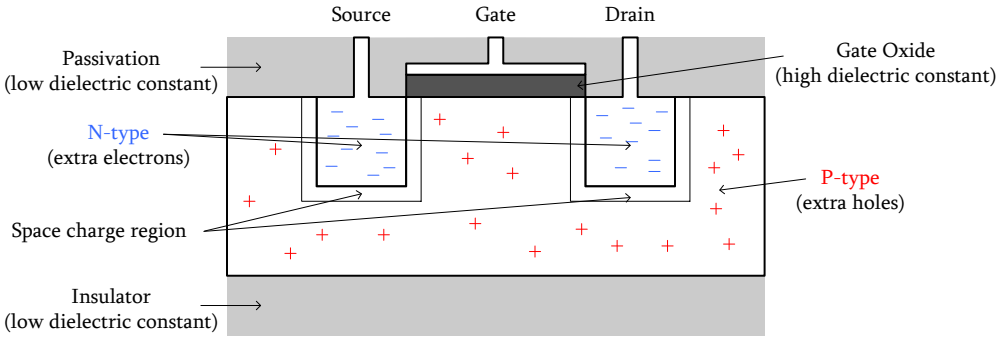

Fig. 1: N-MOS transistor schematic

Such electronic circuits are at risk from three principal types of radiation-induced effects: total ionizing dose (TID), single event effects (SEE) and displacement damage (DD).

1.1 Total ionizing dose (TID)

An incident particle can cause direct or indirect ionization of the semiconductor (Fig. 2).

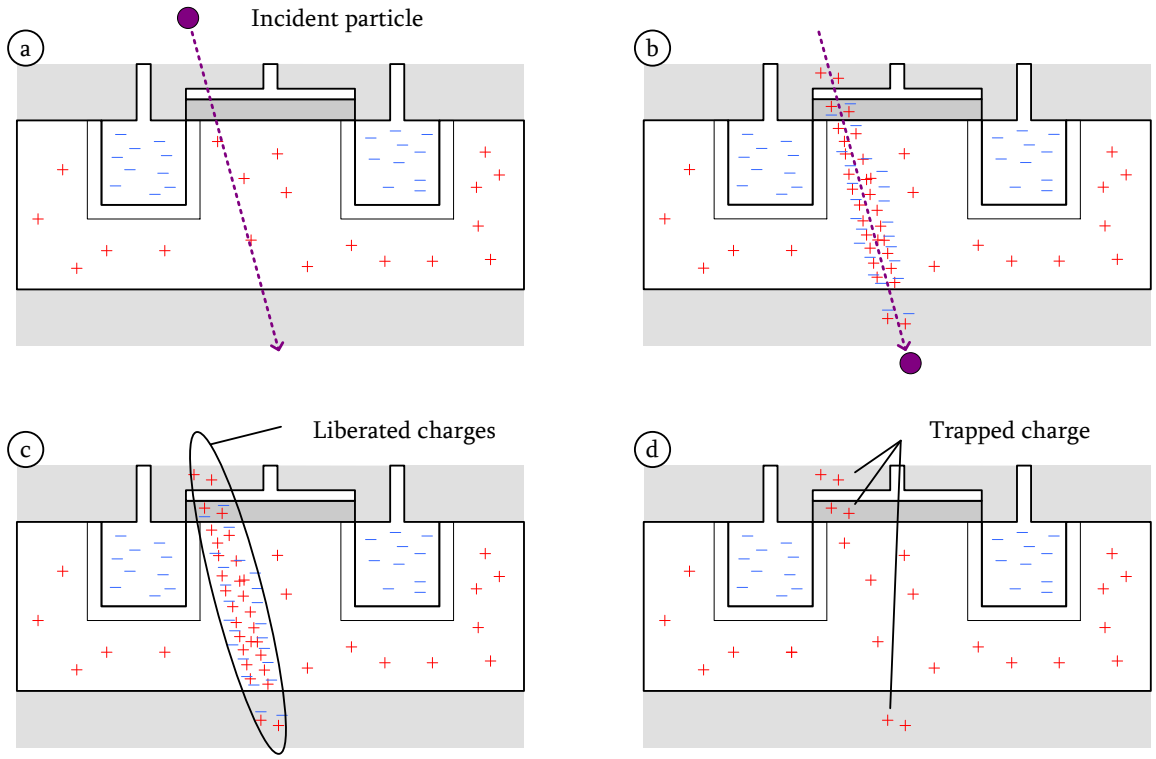

Fig. 2: Total ionizing dose process

Figure 2 shows an example of *direct* ionization, where the primary particle causes ionization:

(a) a charged particle passes through a semiconductor material;

(b) the charged particle interacts with the semiconductor;

(c) electron–hole pairs are generated along the path of the particle due to its energy loss;

(d) holes that are created remain trapped in the integrated circuit oxides (such as passivation, gate oxides, etc.)

Indirect ionization occurs when a primary particle causes nuclear reactions that then lead to ionization.

In both cases, the holes created within the oxides cause changes to device characteristics. The absorbed dose or total ionizing dose (TID) is a *cumulative* effect measured in Grays [Gy]. This increases over time causing gradual degradation of semiconductor performance.

This leads to several adverse effects. For example, consider the positive charge collected in the gate oxides: N-MOS semiconductors have a decrease in switch-on voltage, as the gate is progressively activated by the slow build-up of trapped positive charges. In the same example, P-MOS devices exhibit an increase in switch-on voltage, as the positive charges progressively inhibit the switch-on of the gate. The first observation of these effects will be changes in timing margins and increases in leakage current. Board-level power consumption can increase. Eventually, N-MOS devices will fail so that they are permanently activated, and P-MOS devices are permanently de-activated

All active components are potentially susceptible to TID.

1.2 Single event effects (SEE)

A single event effect (SEE) is prompt, having a certain probability (cross-section) of occurring with every particle interaction. An SEE manifests in several ways, however the root cause is generally the same (Fig. 3).

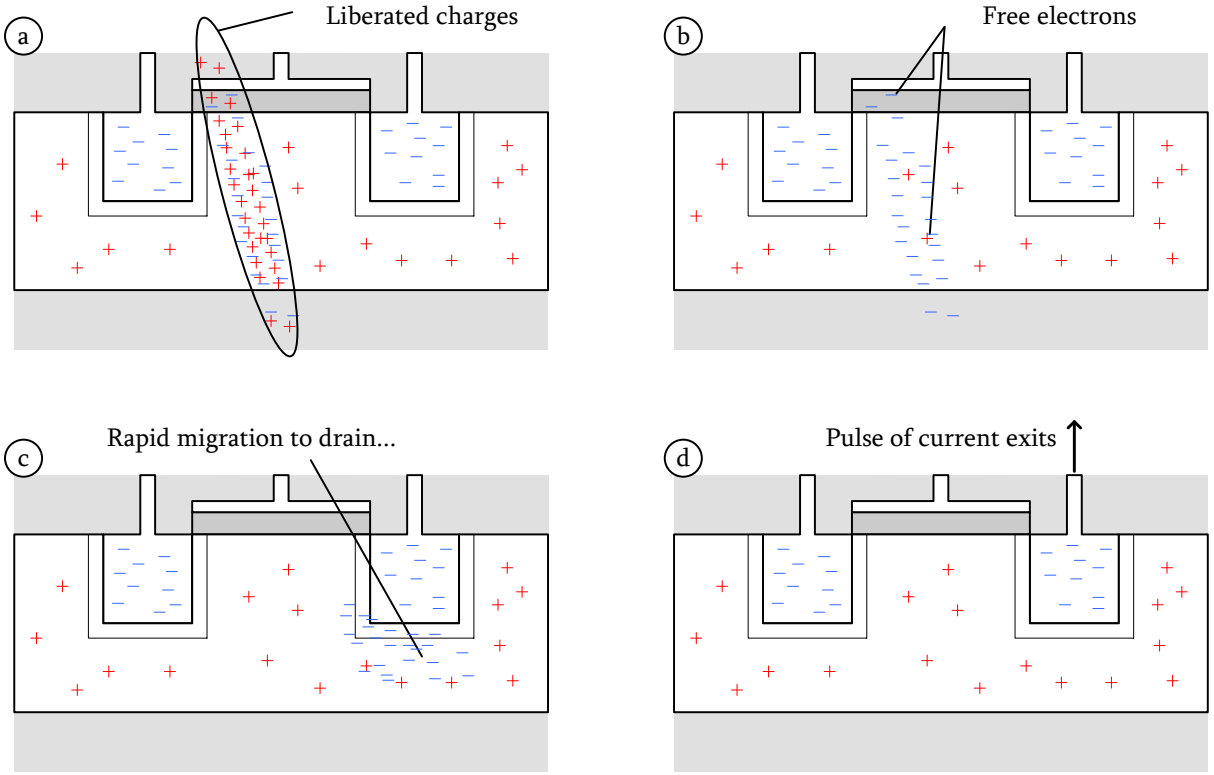

Fig. 3: SEE process (bias not shown, for simplicity)

Figure 3 considers an incident particle acting on a semiconductor, as described in the TID case. However, consider the behaviour of electrons, not holes:

(a) a charged particle passes through a semiconductor and interacts;

(b) electrons are generated by the particle as it traverses the material;

(c) electrons are highly mobile and flow through the MOSFET, and are collected at the reverse biased junction;

(d) these electrons create a pulse of current shortly after the particle's interaction.

In almost all cases, the root cause of the SEE is the *current pulse*. It can have a variety of impacts and outcomes on the circuit. There are two typical *soft failures*.

- Single event transient (SET) – a transient is created on a signal path. This has a variety of effects depending on the path's function. One potentially significant impact is an SET on a clock line, causing set-up and hold timing to be violated.
- Single event upset (SEU) – the initial particle interaction causes a stored bit to change in value. This erroneous value generally persists until it is re-written. The effect of an SEU on the system level depends upon the location and function of the flipped bit.

Other potentially disastrous failure modes exist, particular in complementary metal oxide semiconductor (CMOS) circuitry; consider Fig. 4.

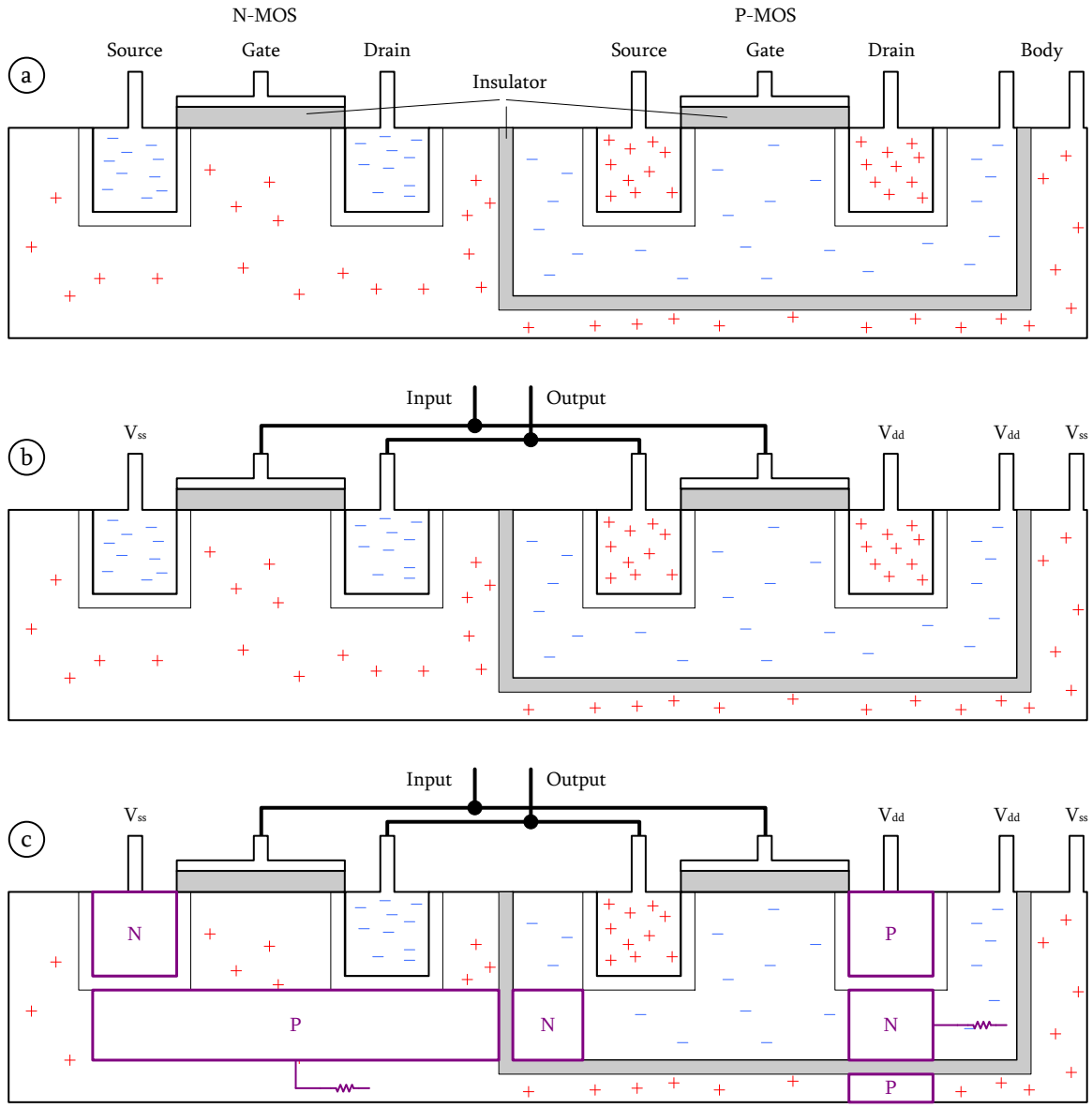

Fig. 4: CMOS transistor schematic

1. A CMOS structure is made from a pair of N-MOS and P-MOS devices;
2. A basic inverter configuration is shown, with the gates, sources, and drains connected appropriately;
3. A parasitic NPN, PNP structure exists in the CMOS device.

If a particle interaction deposits sufficient charge, then the parasitic structure can be activated, causing *hard failures*, such as the following.

- Single event latch-up (SEL) – a low-impedance short-circuit between power supply and ground is created; this requires power to be removed for the latch-up to be cleared. An SEL has the potential to be catastrophic if it is not mitigated, due to localized heating of the component in the high current state [2].
- SEE hard failures covers other effects such as single event burnout (SEB) and single event gate-rupture (SEGR).
- SEE are *prompt* (relative to displacement damage (DD) and TID), and each particle traversing the semiconductor has a certain probability of interaction. The particles of interest are *high energy hadrons* (HEH) or ions, and the critical parameter is the *cross-section*, which is the probability of an HEH-induced SEE.

1.3 Displacement damage (DD)

Displacement damage (DD) occurs when particles interact with the silicon lattice. Figure 5 shows the key process.

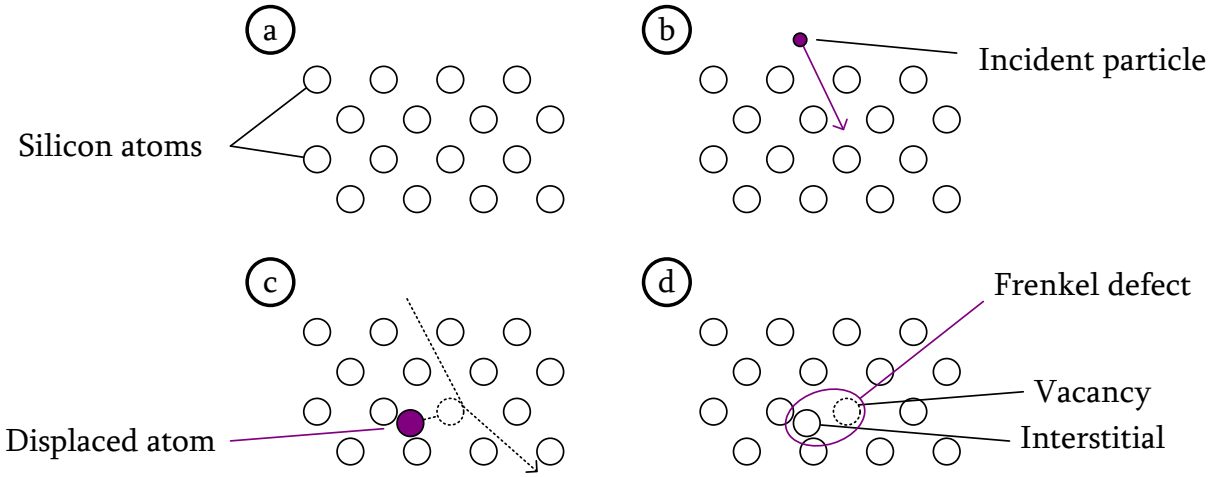

Fig. 5: DD process

In Fig. 5:

(a) an ideal silicon lattice has regularly spaced atoms;

(b) incident particles traverse the lattice;

(c) there is a probability that the particle strikes and dislodges an atom;

(d) this interaction can create *Frenkel defects* consisting of a *vacancy* and an *interstitial defect*.

Damage to the lattice is proportional to the integrated flux of particles that have passed through the atomic structure, therefore DD gradually increases over time. The effects of DD generally reduce device gain, which eventually leads to complete failure of the device. DD mainly affects bipolar technologies; CMOS technologies generally do not suffer from DD effects.

DD is a *cumulative* effect and is measured as the total number of 1 MeV equivalent neutrons that have passed through a given surface area [1 MeV eq. n/cm^2]. The term non-ionizing energy loss (NEIL) is also used.

2 Design for radiation

Dealing with radiation effects on electronic systems is a fundamental part of electronics design; at the same time, it is a tremendously complex and expensive requirement. Engineers should make every effort to first optimize the system requirements before embarking on the development of radiation-tolerant designs. Only after exhausting all alternatives should the design of a radiation-exposed system be undertaken. The main considerations to address are given below.

- Functional – is the system needed at all? Engineers should consider whether it is possible to design-out the system's function at a higher level. Are there alternative means to achieve the same goal without having a dedicated system? What are the consequences of not having this system?
- Environmental – does the system need to be here? Before undertaking a system design, exhaust all options for moving systems away from radiation, or shielding equipment from radiation. Move every element that can be moved, in order to minimize the amount of radiation-exposed elements as possible.
- Dependability – can the permitted failure rate of the system be increased? Dependability requirements should be established at an early phase. The system should have a reasonable failure rate. In addition, the permitted failure modes should be outlined. Protection-related systems may have a strict *unsafe* failure rate specification. Systems with such a requirement add further complexity to an already complex process. Engineers should make every effort to increase the permitted failure rate, and to exclude undesired failure modes.

2.1 Radiation hardened vs. radiation tolerant

Once it is decided that a radiation-exposed system must be designed, a primary factor is to determine whether a radiation-*hardened* or radiation-*tolerant* design is needed.

The principal consideration is the environment. Figure 6 shows typical values of radiation fluence and dose for sea, air, and space applications, as well as the approaches needed. The delimitation of the areas is not a fixed value, and can be debated.

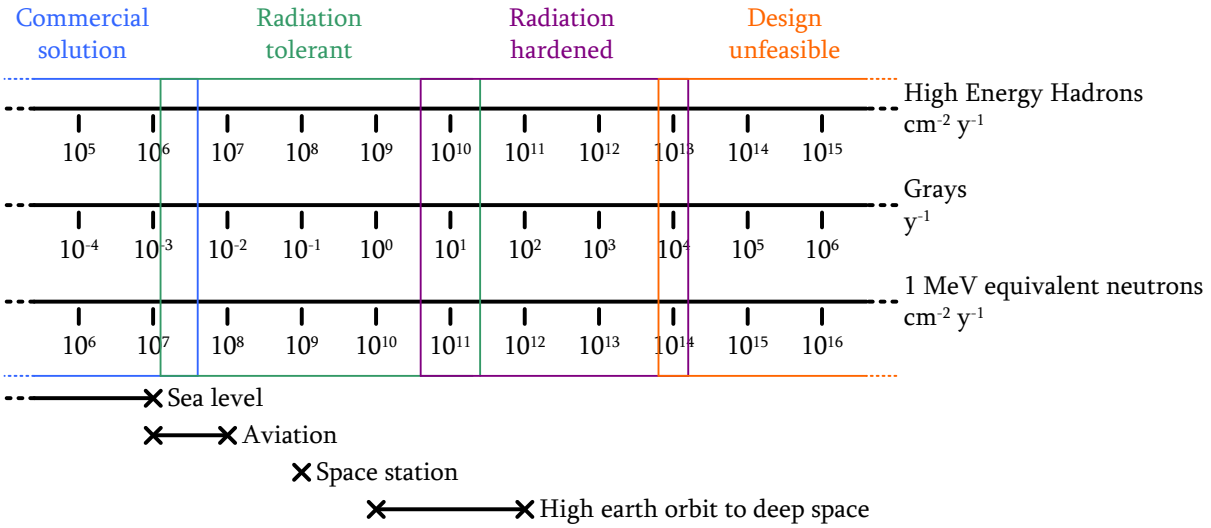

Fig. 6: Radiation exposure levels vs. engineering approach (CERN defined)

Radiation-hardened systems (as defined at CERN) exhibit no adverse effects from radiation, as they are immune to radiation-induced problems, in the environment specified, up to defined limits. These systems can make use of radiation-hardened technologies (so-called radiation-hardening-by-process) or mitigation of radiation effects at the design level (radiation-hardening-by-design). A complete, certified, radiation-hardened hardware solution can be designed. One of the key drawbacks of this approach is cost. For example, a radiation-hardened programmable logic device is 100–1000 times more expensive than a commercial device [3], and a custom-made integrated circuit can have extremely high set-up costs in the order of millions of Swiss Francs [4].

Radiation-tolerant systems (as defined at CERN) are those that can be made to function in radiation environments despite being susceptible to radiation. This is primarily done by mitigating the consequences of the effects. This paper explains the process of designing *radiation-tolerant* systems based on commercial off-the-shelf (COTS) components.

2.2 Radiation-tolerant design flow

A design flow has been created to address project risks specific to the development of radiation-tolerant COTS electronics. The design flow begins after the *requirements capture* and *engineering specification* phases. The process flows of electronics system and radiation-tolerant system development are shown in Fig. 7.

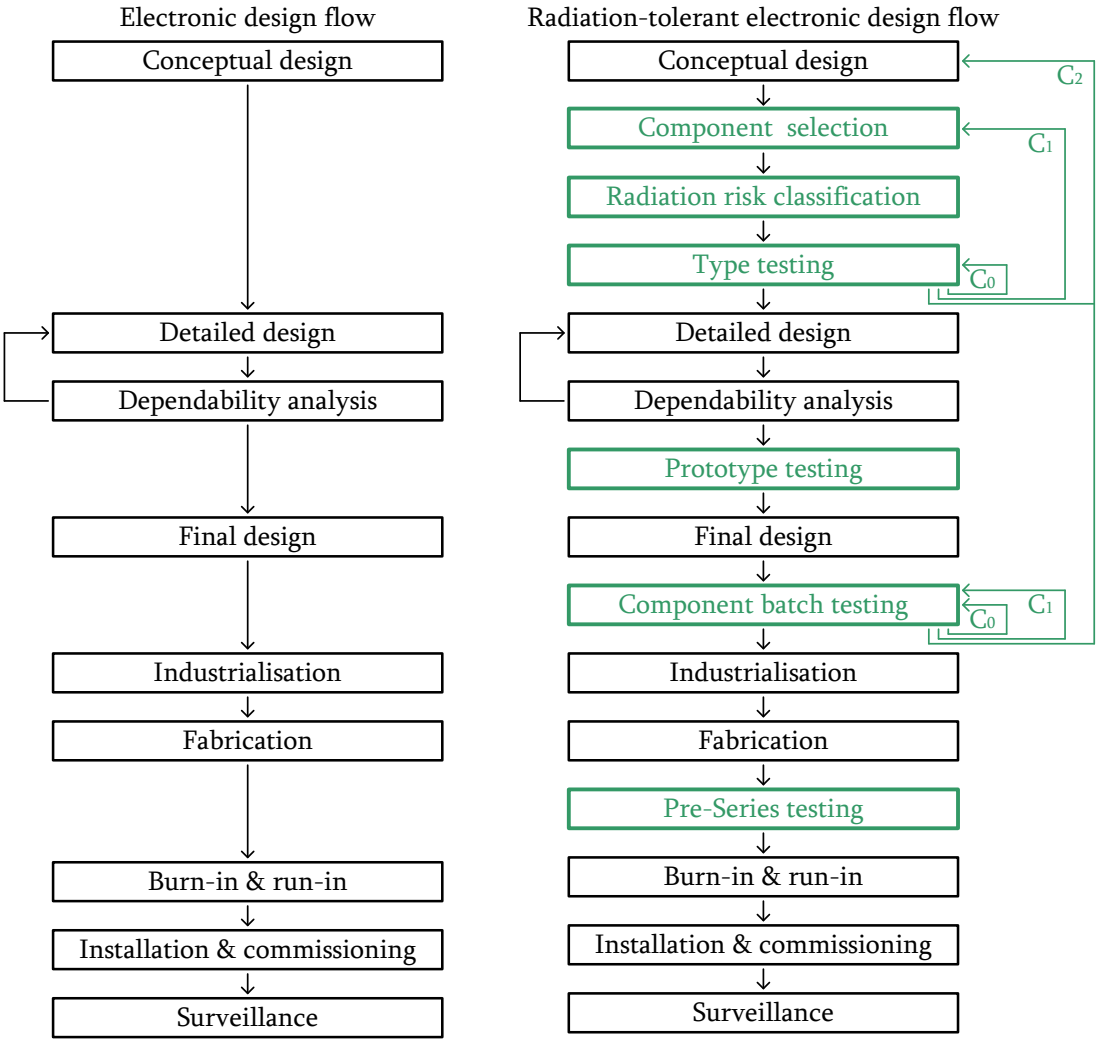

Fig. 7: Electronics design flow and radiation tolerance electronics design flow [5, 6]

The arrows in Fig. 7 show the impact of an electronic component that is not satisfactory. The arrows are marked C_0, C_1 and C_2 as a function of criticality of the unsatisfactory component in the design flow. A complete classification of components, their criticalities and different steps are described in the following paragraphs of this section. This flow can be directly compared with the Radiation Hardness Assurance of components ECSS-Q-ST-60-15C [7].

- Conceptual design – a basic design for the system is selected, with solutions proposed for the implementation of each required function from the *engineering specification*.
- Component selection – the *conceptual design* is broken into sub-systems, and a component inventory is established, with components organized by functional requirements. The component selection and creation of the bill-of-materials (BoM) are made in close collaboration with the design team. The defined functionality of the system needs to be balanced against the feasible radiation-tolerant solutions. This is an iterative process, which continues as radiation tests advance. Some components may need to be changed as results appear from testing. Radiation testing is a slow and complex process, thus minimization of component count and variation is a key requirement.
- Radiation risk classification – each component to be used is classified into one of three risk classes ($C_{0–2}$) based on a risk matrix, cross-referencing the likelihood and impact of radiation-induced failure. Three main criteria are used for the component classification:
  1. the known susceptibility of the type of component to radiation;
  2. the function of this component in the design, i.e. the impact of its failure on system reliability;
  3. the availability of alternatives for the component.

A summary is given below.

- C_0 components are those that are known to be resistant to radiation, or are easily replaced if found to be weak. In general the design of the system is not influenced by these C_0 parts. Examples: resistors, capacitors, diodes, transistors, etc.
- C_1 components are those that are potentially susceptible to radiation, in less critical parts of the system. Substitution of parts or mitigation of issues is possible with a redesign. Examples: regulators, references, drivers, level translators, memory, etc.
- C_2 components are those that are potentially susceptible to radiation, being found in more critical parts of the system. If these parts do not perform well then the basic design is compromised, and a significant rework of the *conceptual design* is needed. Substitution of parts or mitigation of issues due to C_2 parts is generally difficult. Examples: analog-to-digital converters (ADCs), programmable logic, mixed circuits, etc.
- Type testing – the selected components are subject to radiation testing to identify cross-sections and to predict component lifetimes. Various sources of radiation test data can be consulted from other institutes and organizations such as the ESA [8], NASA [9, 10] or in the IEEE NSREC data workshop proceedings. In some cases, test setup, test procedure and test parameters such as bias conditions or temperature may be similar to the project application and the test results can be directly used without a dedicated radiation characterization test. It should be noted that some of the ESA/NASA tests are performed on high-reliability electronic components, which can have different radiation tolerance to regular COTS components, even when considering the same reference numbers from the same manufacturer.

In the absence of reliable radiation results for a given component, a radiation campaign is prepared. Each individual component is tested by applying procedures that are briefly described in Ref. [11]. The higher the class of the component, the more detailed is the analysis of its response to radiation.

Several reference test standards exist for the planning and execution of the radiation tests. These are: for SEE, JEDEC Test Standard 57 [12] or ESA/SCC 25100 [13]; for TID, MIL-STD 1019.8 [14], ASTM F1892 [15] or ESA/SCC 22900 [16]. An extensive review of TID radiation hardness assurance standards can be found in Ref. [17]. The level of testing required depends upon the class of the component (Table 1).

Table 1: Radiation characterization test methodology

Class	Mixed field	Proton	Heavy ion
C_0	Mandatory		
C_1	Optional	Mandatory	
C_2	Optional	Mandatory	Mandatory

At CERN, C_0 components are tested in a mixed-field radiation environment equivalent to LHC tunnel conditions, thus giving a direct indication of the device's performance in the final application.

C_1 components are irradiated with mono-energetic protons to measure susceptibility to SEE and TID; mixed-field tests are optional proton tests that allow assessment of SEE and TID response of a component in a much shorter time. Two or more candidate parts for each C_1 position should pass *type testing*. If this cannot be ensured, it is possible that a return to *component selection* is needed to find more candidate parts.

Type-testing failure of C_2 parts is critical for the project. These are tested in exactly the same way as the C_1 components, with the addition of heavy-ion testing to assess SEL cross-section and the respective risk in the LHC radiation environment. At least one C_2 part must be found that meets system requirements. If this is not the case the *conceptual design* must be revised.

- Detailed design – the remainder of the design is established, using components that performed well in *type testing*.
- Dependability analysis – the reliability of the system hardware is predicted, using cross-sections, lifetimes and electrical characteristics. Traditional reliability engineering techniques can be used to meet system requirements.
- Prototype testing – a small number of prototypes are constructed, following the concept emerging from the dependability analysis. These are used to validate design choices, and to ensure correct integration between connecting systems and controls.
- Final design – the final design is established, which *on paper* meets all of the functional and dependability requirements of the system.
- Component batch testing – after prototype validation and definition of the final implementation, the procurement of large quantities of components begins. Each has to be qualified to confirm the results of the type testing and to assure the conformity of the component radiation response within the lot. COTS components form the main part of those used in this framework; ideally all production components should be procured from a single fabrication lot to decrease the component-to-component variability. In many cases, it is impossible to get such information concerning the number of silicon wafers from which the components were made, their lot date code, or even the lot origin. This makes lot acceptance tests complex and challenging. ESA specifications require a minimum of 11 samples to be

selected for TID characterization: ten for irradiation and one reference part. Similarly, the CERN lot acceptance test strategy requires a minimum of ten irradiated samples and one reference for each component lot. The number of samples to be tested for SEE characterization is much smaller, typically three [13].

If a C_0 component does not pass testing, another equivalent component will be purchased and lot acceptance tests will be performed. If a C_1 component does not pass the lot acceptance tests, its equivalent will be chosen from a list of preferred replacements for C_1 components prepared in advance during preparation of the BoM. As shown in Fig. 2, C_2 components are highly critical for the design, and in the case of lot non-conformity the project's conceptual design will have to be revised. For all C_2 components it is of the utmost priority to decrease the probability of lot problems.

- Industrialization and fabrication – the number of required units is produced, after industrialization, ensuring the best quality is achieved for the product being designed.
- Pre-series testing – production is usually split into pre-series and series production. A small number of parts are delivered first, which are manufactured using the industrial assembly line. Accelerated lifetime testing and dedicated irradiation testing can be carried out to ensure that industrialized fabrication yields parts that meet predictions.
- Burn-in → surveillance – the usual steps in the delivery of an engineering product.

3 Radiation testing

Radiation testing is a crucial aspect of the development of radiation-tolerant electronic systems. The three key radiation effects need to be characterized and quantified for each of the parts being used.

To determine the effects of *displacement damage*, parts are placed in the vicinity of radiation sources, typically neutrons. The parts do not need to be powered for displacement damage to occur; after irradiation parts are characterized on electrical test benches. Dedicated irradiation areas can be found in the proximity to fission reactors, such as PROSPERO [18].

SEE cross-sections and TID limits are determined by controlled exposure to radiation. This is done by building dedicated test equipment that exercises components whilst they are being irradiated. Tests and observations are carried out, looking for the malfunction characteristics of SEEs, and the end-of-life due to TID. Special care has to be taken to subject parts to a representative radiation field. The irradiation spectra have to give meaningful results considering the environment in which the system is to be used.

An example of a representative SEE and TID test area was the CERN Neutrinos to Gran Sasso (CNGS) gallery, which was operated until 2012. Proton beams from the Super Proton Synchrotron (SPS) were extracted onto a target, creating a neutrino beam. A radiation field is created by the interaction of the proton beam with the target, so components could be tested in the immediate vicinity (Fig. 8).

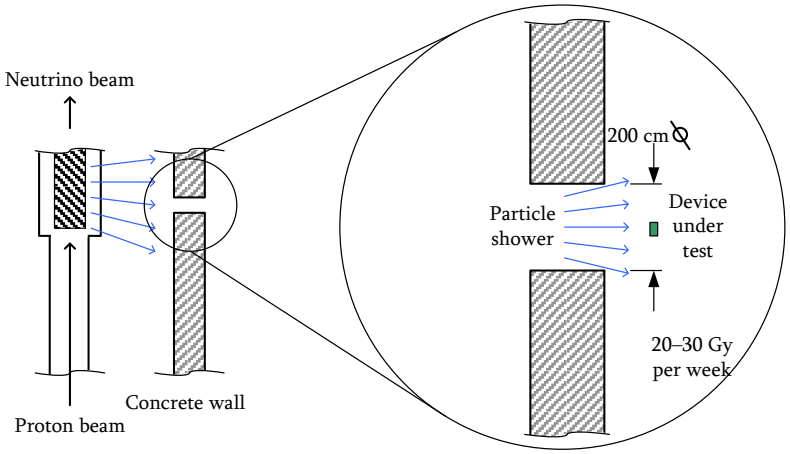

Fig. 8: Plan view of the CNGS installation [19]

A typical test apparatus placed in this location includes devices under test, which are surveyed and characterized. The conclusions from such tests are the device *failure modes*, and *failure mode ratios*. This is an exhaustive list of errors that have been observed, grouped by failure mode. The ratios of each type of error are also determined. In addition the TID limit is determined, giving the effective device lifetime in this particular radiation field. A drawback of these tests is limited beam availability and long irradiation time due to the low fluences that can be obtained [18]. At CERN a new facility, called CHARM, is under construction to overcome these limitations [20, 21]. CHARM is intended to provide:

- mixed-field particle spectra representative of the LHC tunnel, space, and/or ground level;
- a large testing volume to allow the testing of several cubic metres of equipment;
- high beam availability and intensity higher than an operational environment as in the LHC tunnel.

4 Applying the design flow to power converter controls

The design flow outlined in the previous section is being applied to the development of the power converter controls for the LHC at CERN. The LHC has several thousand normal and superconducting magnets with associated power converters. A typical example circuit is the 13 kA dipole circuit as shown in Fig. 9.

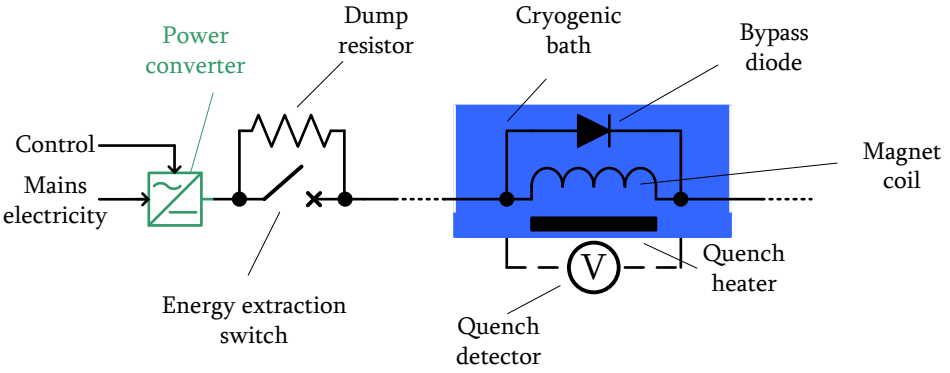

Fig. 9: Superconducting electrical circuit, with power converter

These circuits have a high stored energy, and use a system of interlocks and protection to guard against the uncontrolled release of magnet and powering energy. The power converter converts mains energy to the required magnetic field for beam operations (Table 2). The set point and operation of the power converter is managed by a power converter *controller*.

Table 2: Types of power converter in the LHC

Principal application [magnet]	**Voltage [V]**	**Current [A]**	**Quantity**
Main dipoles	13 000	190	8
Main quadrupoles	13 000	18	16
Quadrupole circuits	4 000–6 000–8 000	8	188
Warm circuits	1 000	450–950	16
Sextupole circuits	600	40	37
Octupole circuits	600	10	400
Orbit correctors	120	10	298
Orbit correctors	60	8	752

This gives a total of *over 1700* power converters used in the LHC. These are located in one of five different areas (Fig. 10), each with a different risk classification for radiation:

1. at the surface;
2. in parallel galleries;
3. in perpendicular galleries;
4. in alcoves;
5. the LHC accelerator tunnel.

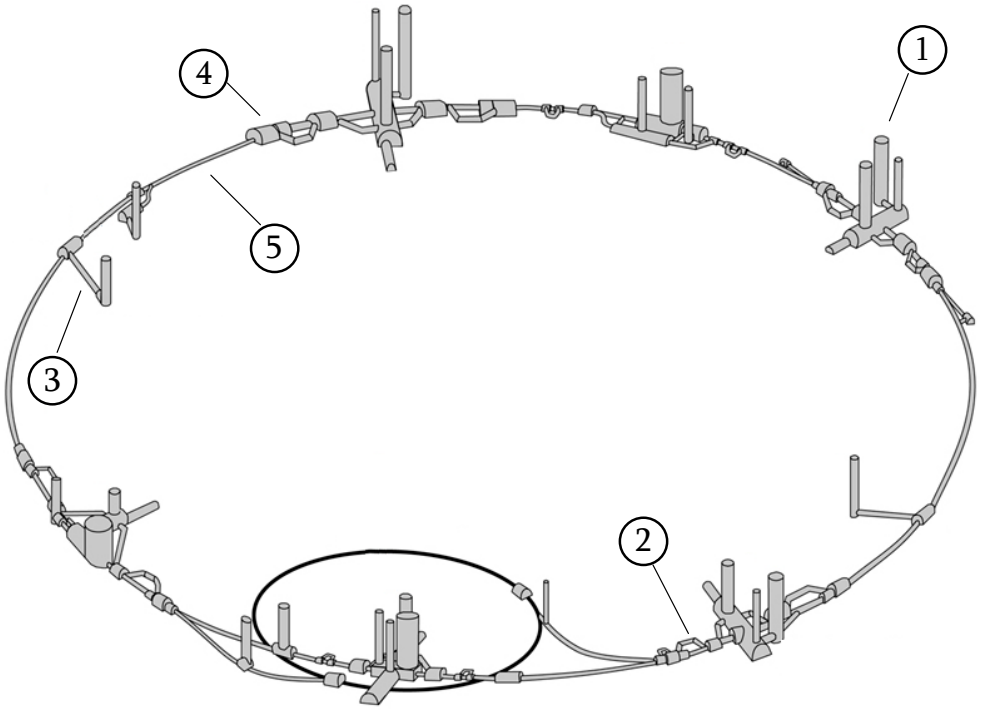

Fig. 10: Civil works with principal converter locations [22]

Perpendicular galleries, alcoves, and the accelerator tunnel each present a moderate to high level of risk concerning exposure to radiation. Of the power converter quantities shown before, *over 1000* are located in such areas (Table 3).

Table 3: **Power converters found in moderate to high radiation risk areas [23]**

Principal application [magnet]	Voltage [V]	Current [A]	Perpendicular	Alcove	Tunnel
Quadrupole circuits	4000–6000–8000	8	6	60	-
Sextupole circuits	600	40	-	12	-
Octupole circuits	600	10	24	104	-
Orbit correctors	120	10	15	92	-
Orbit correctors	60	8	-	-	752

Each power converter can be broken down into three distinct sections (Fig. 11).

1. a function generator controller (FGC) electronic module;
2. a voltage source (VS), consisting of power electronics and power circuits converting mains power to the current and voltage requested by the FGC;
3. current transformers (DCCT) converting the electrical output current of the converter into a digital value that is read back by the FGC.

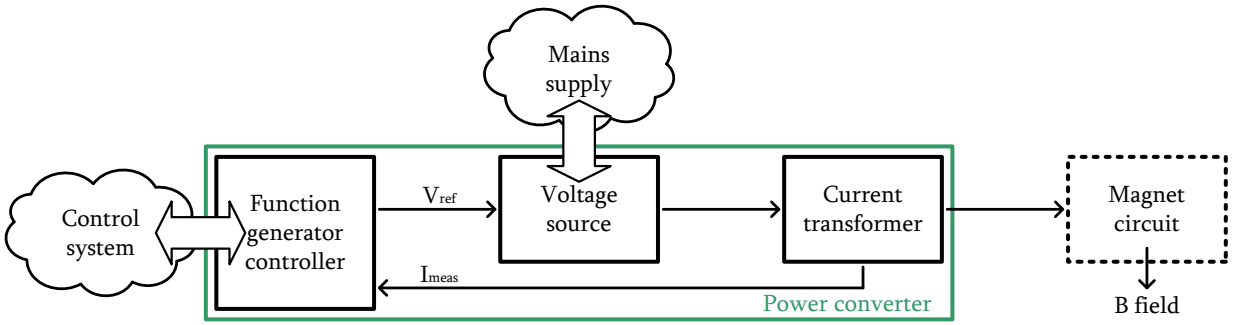

Fig. 11: Key components of a power converter

The design flow has been applied to the design and realization of the FGC that is to be used in the power converters located in moderate to high radiation risk areas, as shown in Table 3.

4.1 Function generator controller

The FGC is a purpose-built electronic module having several functions (Fig. 12). Most notably [24] it:

- implements closed-loop regulation of the magnet current, reading the measured current I_{meas} to establish the reference voltage V_{ref} needed for the field;
- controls the converter, by issuing digital commands such as ON, OFF, and RESET;
- implements low-level interlock logic as part of the interlock loops between the VS, quench detection, and powering interlock systems [25];
- allows remote control and surveillance of the converter and associated subsystems.

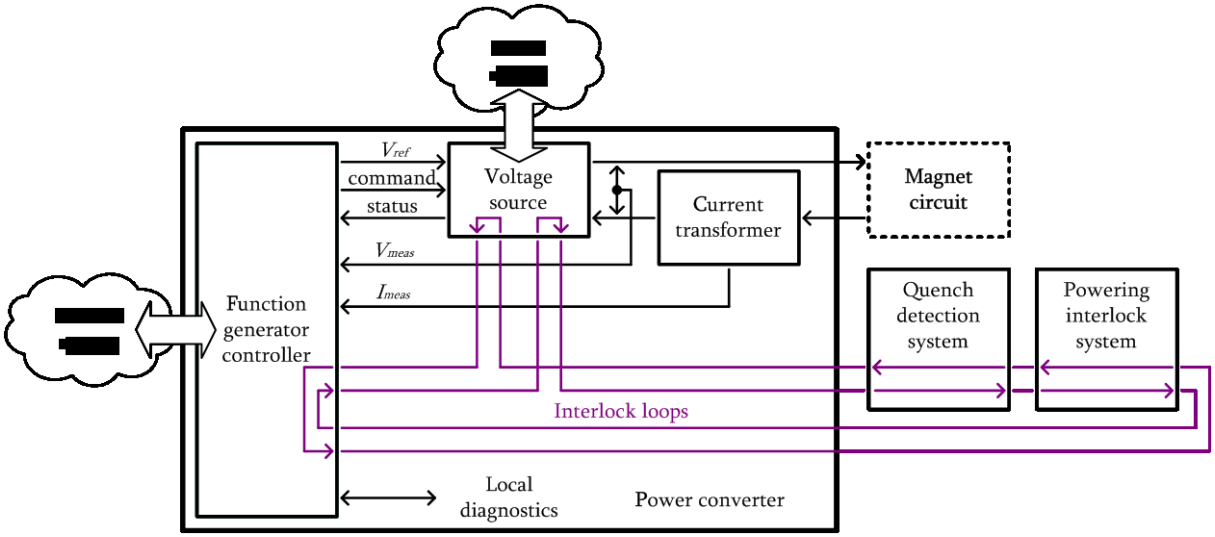

Fig. 12: Basic connectivity of an FGC

The control system of the LHC power converter controls is based on the WorldFIP fieldbus (Fig. 13), using a gateway computer with bus master to send and receive real-time commands to FGC slaves.

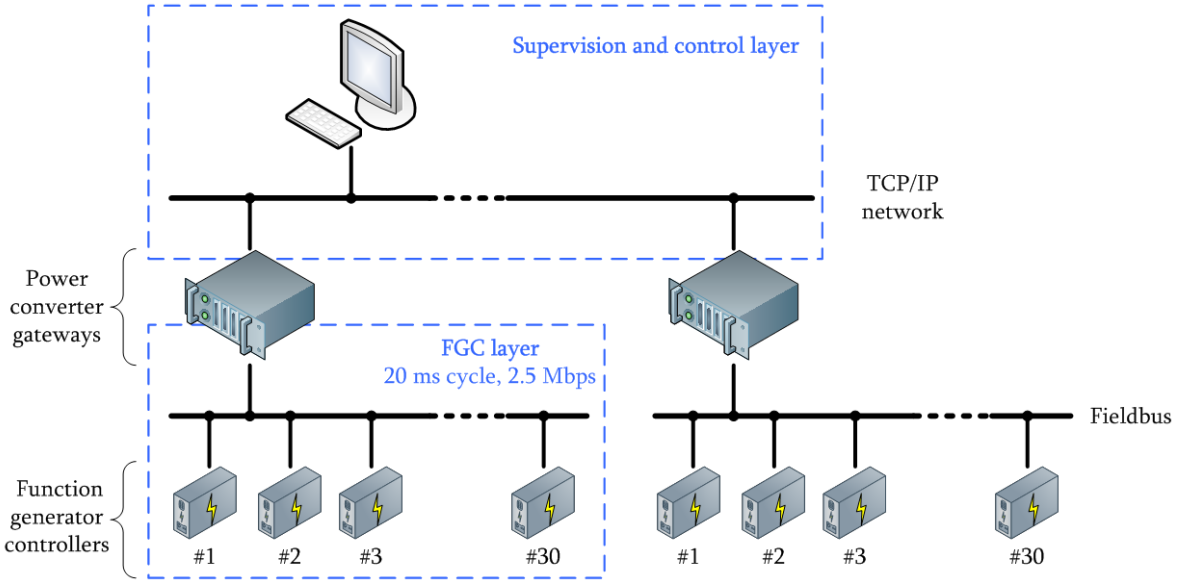

Fig. 13: Fieldbus control principle

The use of the fieldbus provides a low-bandwidth communications solution for the FGC. During each cycle only around 32 bytes can be transmitted to, and 128 bytes received from, each FGC [26].

4.2 Radiation-tolerant function generator controller

From the operational point of view, power converters are to behave in the same way regardless of whether an FGC or an FGClite controller is used. To optimize costs, the existing fieldbus infrastructure will be re-used and FGClites will be plug-compatible with FGC2. This makes significant savings but means that fundamental changes to the FGC philosophy are not possible. Effort has been put into the optimization of software, programmable logic, and hardware partitions to minimize the complexity of the FGClites, whilst meeting system-level requirements.

In FGC2, the current reference as a function of time is stored locally in each FGC. A function table and regulation circuit use circuit settings specific to the magnet circuit being powered to drive the voltage reference point (Fig. 14).

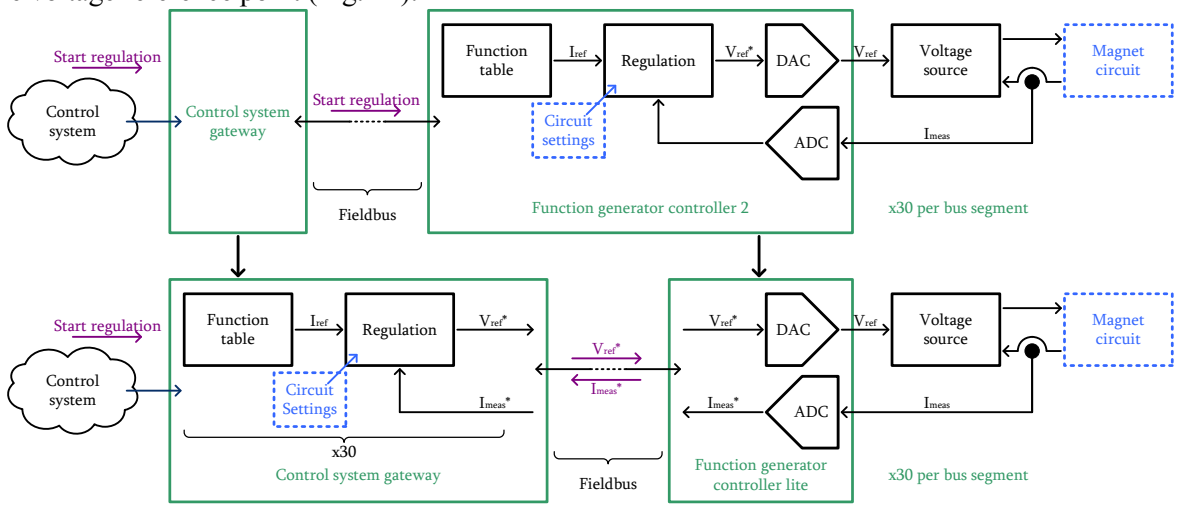

Fig. 14: Closed loop control architecture changes [26]

The gateway sends simple commands such as *start regulation* to each FGC. The most significant hardware change for the FGClites is the relocation of the digital signal processor (DSP) into the gateway, with the FGClite acting as a remote input/output module.

The gateway complexity is significantly increased as it is required to implement the regulation calculations for all FGClites connected on the same fieldbus segment. This increases the latency of the regulation loop due to the transmission of information back and forth on the fieldbus, which requires the regulation algorithms to be adjusted. Additionally, FGC2 was capable of working independently of the fieldbus for short periods, whereas the FGClites will be completely dependent on the fieldbus for correct operation.

4.3 Software and programmable logic partitioning

FGC2 depends on both software and programmable logic to achieve its functional requirements. Embedded software is used both for closed-loop signal processing and converter supervision. In the FGC2, eleven programmable logic devices are used for sub-functions such as timer circuits, access to coefficients, and digital multiplexing, amongst others (Fig. 15).

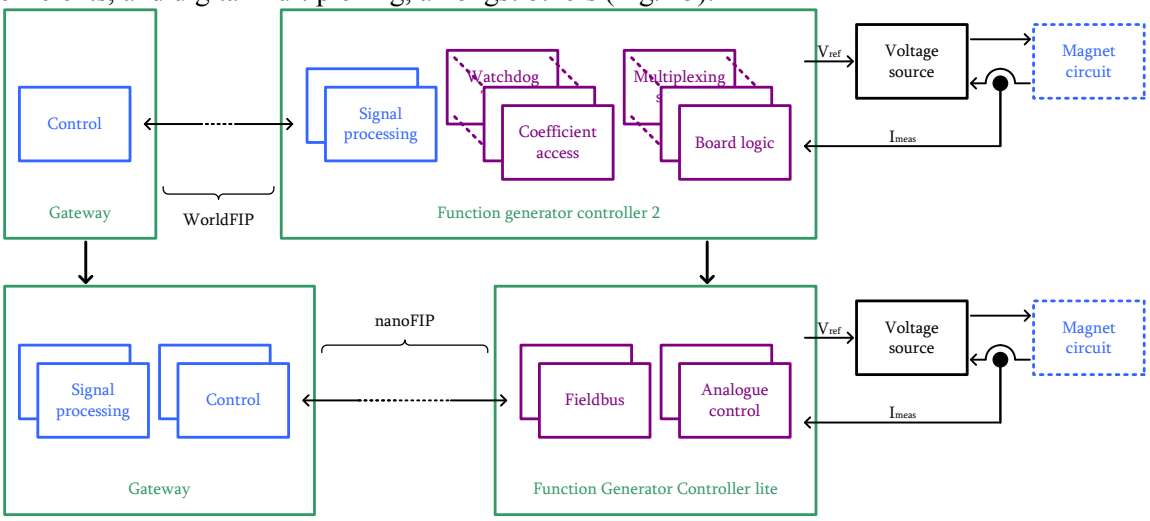

Fig. 15: Architecture changes

FGClites are to have no locally executed software as the signal processing functions are to be moved to the gateway. The remaining supervision requirements, as well as FGC2 functions implemented in programmable logic, are to be implemented in three flash-based field programmable gate arrays (FPGAs) having functionality described in VHSIC hardware description language (VHDL).

The obsolete WorldFIP chipset is also to be replaced by CERN nanoFIP, which also uses a flash FPGA. NanoFIP exploits the WorldFIP electrical standard but a simple transmission protocol between gateway and power converter [27].

4.4 Predicted reliability and lifetime

Failures of the power converter hardware can be split into two categories: basic failures corresponding to the bathtub curve and those related to radiation damage.

4.5 Basic failures

The first source of failure is expected to follow the typical hazard function for the failure of non-complex electronic systems, the so-called bathtub curve, made up of three sections.

- *Early-life* failures are caused by latent defects and are avoided by processes such as stress screening and running-in.

  The *useful-life* failure rate is one of the biggest concerns for the success of the FGClite project in meeting its reliability goal. Failures of this nature can occur at any moment in time and are not correlated. This is to be minimized by following design practices promoting reliability, such as over-specification and redundancy. The base failure rate of the FGClites will be determined using a combination of past experience and military handbooks.

- *Wear-out* failures are due to the gradual wear-and-tear of electronic systems in use. In the FGClites these are to be minimized by following the most appropriate maintenance plan, either preventive or reliability centred maintenance (RCM).

4.6 Radiation-induced failures

The second source of failure is that related to radiation. Radiation-induced damage manifests itself in two manners: cumulative and prompt. Cumulative or total dose effects reduce the effective system lifetime by advancing the wear-out phase, and SEEs increase the random-in-time failure rate of the system across its whole lifetime.

First prompt effects, such as SEU or SEL, can cause the system to malfunction, having the effect of increasing the random-in-time failure rate of the FGClites. The predicted number of failures per year can be seen as a function of the fluence of particles in the areas in which the FGC is installed, and the cross-section of each FGClite. Figure 16 shows the characteristics for a subset of converters with an LS1–LS2 estimated fluence of 9×10^9 high energy hadrons (HEH) per square centimetre per year in tunnel installations [28].

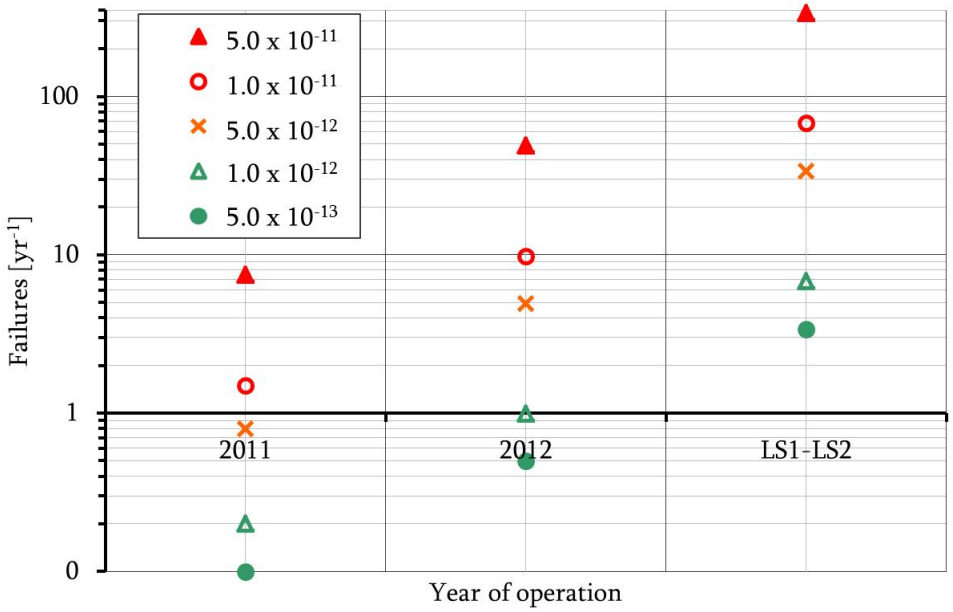

Fig. 16: Cross-section and predicted failure rate for LHC operational phases

4.7 Requirements

There are two key requirements: *lifetime*, and *reliability*.

- Lifetime: the FGClites must be designed to outlast the LHC. Current planning extends into the 2030s, so an FGClite installed in 2015 would need >25 years' lifetime. In addition to the electrical requirement, radiation dictates that every component in the FGClites must remain within specification after absorbing around 200 Gy.
- Reliability: power converters have a direct influence on the availability of the LHC machine. the LHC is expected to run for 200 days every year, with two ten-hour fills, and two recovery periods of two hours every day [29]. This gives 400 LHC missions per year. No more than 10% of these should be aborted due to the failure of power converters; this means that each power converter must have an MTBF in excess of 400 000 hours.

This can be split between electrical and radiation-induced failures. Electrical MTBF is therefore required to be similar to the existing controllers, with a maximum of 10 radiation-induced failures per year of operation for all installed systems. This means the SEE cross-section of the FGClites is required to be equal to 3×10^{-12} cm^2 or lower.

Combining these requirements means that all FGClites in operation are expected to fail less than 10 times per year due to radiation-induced errors, and less than 30 times due to electrical effects, meeting the combined requirement of less than 40 failures per year.

4.8 FGClite project risks

FGClites are required to be installed in the LHC at the end of 2015. The most significant risk to the successful completion of the project concerns class C_2 components: optimization of component selection has yielded only three C_2 parts:

- the ADC used to determine I_{meas};
- the mixed analog–digital IC used for the fieldbus interface;
- the flash-FPGA used throughout the design.

Early efforts focused on the *type testing* and *component batch testing* of these parts to determine their suitability for the FGClites.

The quality of statistics is critical for reliability calculations, as they drive both the mitigation techniques and overall FGClite reliability. Of particular importance is the predicted HEH fluence in the LHC tunnel. In this context there is a risk of over-engineering the FGClites by taking an excessively pessimistic view: layers of redundancy and power-cycling options could be in excess of the project needs, reducing overall reliability.

The shift away from software towards programmable logic has many implications, ranging from the skills required from the project team, to quality assurance of the FGClites. Reliability calculations explained in this paper assume a non-complex system, free from systematic faults. The programmable logic engineering must be of the highest quality, matching that used elsewhere at CERN, following guidelines for dependable VHDL design that have been developed in the course of other systems' developments at CERN [26].

5 Conclusions

This paper has explained the principal effects of radiation on electronic components, and has described the principal steps needed to design a radiation-tolerant system. The paper included a worked example showing how radiation-tolerant power converter controls are being developed.

Acknowledgements

This paper has been written in collaboration between the power conversion group of the CERN technology department (TE/EPC) and the CERN Radiation Effects to Electronics working group (R2E). The authors wish to express their gratitude to the numerous individuals who have helped to define this procedure, and who are active in the execution of the FGClite project.

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Passive Power Filters

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Abstract
Power converters require passive low-pass filters which are capable of reducing voltage ripples effectively. In contrast to signal filters, the components of power filters must carry large currents or withstand large voltages, respectively. In this paper, three different suitable filter structures for d.c./d.c. power converters with inductive load are introduced. The formulas needed to calculate the filter components are derived step by step and practical examples are given. The behaviour of the three discussed filters is compared by means of the examples. Practical aspects for the realization of power filters are also discussed.

Keywords
Buck converter; filter damping; filter optimization; transfer function.

1 Introduction

Switched mode d.c./d.c. power converters very often have the structure shown in Fig. 1.

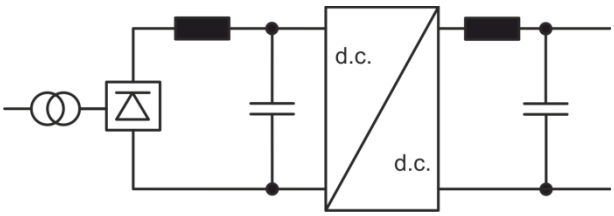


Fig. 1: General structure of a switched mode converter

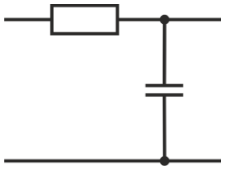
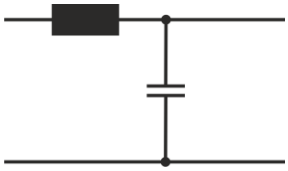
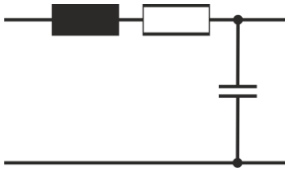
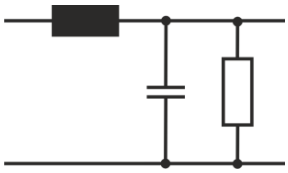
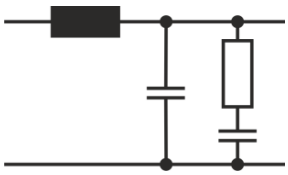
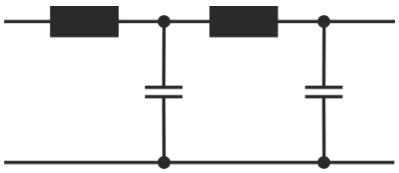
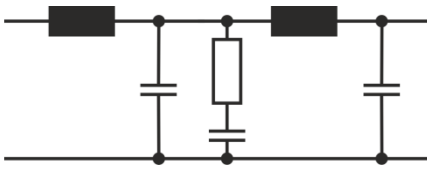
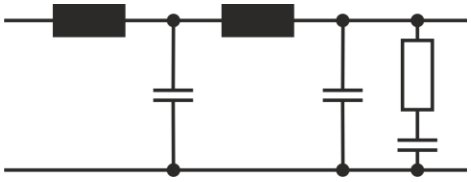
The input transformer and rectifier form a non-controlled d.c.-link voltage with a rather large voltage ripple. An input low-pass filter is needed to reduce this voltage ripple. This filter deals with voltage ripples of typically six times the mains frequency and higher-order harmonics of that. Therefore the components must be designed for frequencies up to a few kilohertz. The capacitor also acts as a voltage source for the d.c./d.c. converter and therefore has to carry large currents at high frequencies. Such input filters require rather large components, the requirements regarding high-frequency behaviour are moderate.

Usually, an output filter is also required to filter the output voltage ripple. An inductive load acts itself as a very effective filter for the current. However, without the output filter the cabling between the converter and the load would carry large a.c. voltages with large voltage slopes. That can cause large electro-magnetic interferences and the cables would need to be shielded. The fundamental frequency of the voltage ripple is equal to the switching frequency of the converter or a multiple of that. High-stability converters for accelerator applications must have a high closed-loop bandwidth in order to react to errors quickly enough. The output filter limits the closed-loop bandwidth; its cut-off frequency must therefore be as high as possible. On the other hand, the cut-off frequency must be well below the switching frequency to reduce the ripple voltage effectively. This leads to converters with rather high switching frequencies of several tens of kilohertz combined with high-order output filters. The filter components must therefore be designed for frequencies up to a few hundred kilohertz.

http://dx.doi.org/10.5170/CERN-2015-003.265

Various structures for passive low-pass filters are listed and evaluated in Table 1 for their suitability for power converters.

Table 1: Suitable filter structures

	For signal filters simple *RC* circuits are commonly used. They offer an attenuation of only 20 dB/decade. The full current flows through the resistor, which causes high losses. Not suitable!
	With an *LC* structure we get 40 dB/decade, but there is a large resonance! Not suitable!
	Series damping in order to overcome the resonance problem: the full current flows through the resistor. If the parasitic resistance of the inductor is large enough, this might be ok. Usually not suitable!
	Parallel damping in order to overcome the resonance problem: the full voltage is across the resistor, which causes high losses. Not suitable!
	Parallel *RC* damping in order to overcome the resonance problem: the resonance can be damped effectively and the losses are reasonable. Suitable; see Section 2.
	Two *LC* stages offer an attenuation of 80 dB/decade, but there is again the resonance problem. Not suitable!
	Parallel *RC* damping in the first stage in order to overcome the resonance problem: losses are moderate. Suitable, but not optimal; see Section 3.1.
	Parallel *RC* damping in the second stage in order to overcome the resonance problem: losses are low. Suitable; see Section 3.2.

2 Design of a second-order low-pass filter

In this section a low-pass filter according to Fig. 2 is outlined.

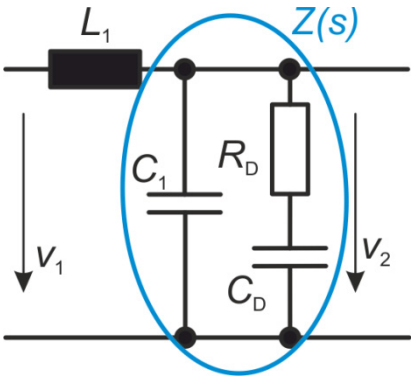


Fig. 2: Second-order low-pass filter

The complex impedance $Z(s)$ is

$$Z(s) = \frac{1}{C_1 s + \dfrac{1}{R_\mathrm{D} + \dfrac{1}{C_\mathrm{D} s}}} = \frac{1}{C_1 s + \dfrac{C_\mathrm{D} s}{R_\mathrm{D} C_\mathrm{D} s + 1}} = \frac{R_\mathrm{D} C_\mathrm{D} s + 1}{C_1 R_\mathrm{D} C_\mathrm{D} s^2 + (C_1 + C_\mathrm{D}) s}. \tag{1}$$

The transfer function of the entire filter is then

$$G(s) = \frac{v_2(s)}{v_1(s)} = \frac{Z(s)}{L_1 s + Z(s)} = \frac{\dfrac{R_\mathrm{D} C_\mathrm{D} s + 1}{C_1 R_\mathrm{D} C_\mathrm{D} s^2 + (C_1 + C_\mathrm{D}) s}}{L_1 s + \dfrac{R_\mathrm{D} C_\mathrm{D} s + 1}{C_1 R_\mathrm{D} C_\mathrm{D} s^2 + (C_1 + C_\mathrm{D}) s}}$$

$$= \frac{R_\mathrm{D} C_\mathrm{D} s + 1}{L_1 C_1 R_\mathrm{D} C_\mathrm{D}\, s^3 + L_1 (C_1 + C_\mathrm{D}) s^2 + R_\mathrm{D} C_\mathrm{D} s + 1}. \tag{2}$$

Note that the s terms in the numerator and in the denominator are equal. Therefore we can write Eq. (2) as

$$G(s) = \frac{k_1 s + 1}{k_3 s^3 + k_2 s^2 + k_1 s + 1} \tag{3a}$$

$$\text{with} \quad k_1 = R_\mathrm{D} C_\mathrm{D}, \tag{3b}$$

$$k_2 = L_1 (C_1 + C_\mathrm{D}), \tag{3c}$$

$$k_3 = L_1 C_1 R_\mathrm{D} C_\mathrm{D}. \tag{3d}$$

$G(s)$ can be expressed as the combination of a third-order PT (time-delay element) in the denominator and a first-order PD (proportional plus derivative element) in the numerator. Let us have a closer look at the third-order PT. This can be split into one second-order and one first-order PT, both connected in series. It can be expressed in its normalized form as

$$G_\mathrm{PT}(s) = \frac{1}{\left(1 + a_1 \dfrac{s}{\omega_0}\right) \cdot \left(1 + a_2 \dfrac{s}{\omega_0} + b_2 \dfrac{s^2}{{\omega_0}^2}\right)}. \tag{4}$$

The transfer function of such a combination of first- and second-order PTs can be optimized according to different methods [1], which results in particular values for a_i and b_i. The commonly used optimization methods with their corresponding coefficients are given in Table 2.

Table 2: Coefficients for a third-order PT for different optimization methods

Method	a_1	a_2	b_2
Butterworth	1.0000	1.0000	1.0000
Bessel	0.7560	0.9996	0.4772
Critical damping	0.5098	1.0197	0.2599

By expanding Eq. (4) we get

$$G_{\mathrm{PT}}(s) = \frac{1}{1 + \frac{a_2}{\omega_0}s + \frac{b_2}{{\omega_0}^2}s^2 + \frac{a_1}{\omega_0}s + \frac{a_1 a_2}{{\omega_0}^2}s^2 + \frac{a_1 b_2}{{\omega_0}^3}s^3}$$

$$= \frac{1}{\frac{a_1 b_2}{{\omega_0}^3}s^3 + \frac{(a_1 a_2 + b_2)}{{\omega_0}^2}s^2 + \frac{(a_1 + a_2)}{\omega_0}s + 1}. \tag{5}$$

By comparing the coefficients with Eq. (3a), we get

$$k_1 = R_{\mathrm{D}} C_{\mathrm{D}} = \frac{a_1 + a_2}{\omega_0}, \tag{6a}$$

$$k_2 = L_1 (C_1 + C_{\mathrm{D}}) = \frac{a_1 a_2 + b_2}{{\omega_0}^2}, \tag{6b}$$

$$k_3 = L_1 C_1 R_{\mathrm{D}} C_{\mathrm{D}} = \frac{a_1 b_2}{{\omega_0}^3}. \tag{6c}$$

For a given optimization method, the three independent Eqs. (6a)–(6c) contain five unknowns (L_1, C_1, R_{D}, C_{D}, and ω_0). Therefore, we have the choice to select two of them and the remaining three depend on that selection.

Selection of the cut-off angular frequency ω_0: for a given angular frequency ω_{B} well in the blocking area of the filter ($\omega_{\mathrm{B}} >> \omega_0$) we can define the desired attenuation G_{B}. In the blocking area the highest-order terms of both the numerator and the denominator in Eq. (2) dominate; therefore it can be simplified to

$$G_{\mathrm{B}} = \frac{R_{\mathrm{D}} C_{\mathrm{D}} s}{L_1 C_1 R_{\mathrm{D}} C_{\mathrm{D}} s^3} = \frac{\frac{a_1 + a_2}{\omega_0}s}{\frac{a_1 b_2}{{\omega_0}^3}s^3} = \frac{a_1 + a_2}{a_1 b_2} \cdot \frac{{\omega_0}^2}{s^2} = \frac{a_1 + a_2}{a_1 b_2} \cdot \frac{{\omega_0}^2}{{\omega_{\mathrm{B}}}^2},$$

$$\omega_0 = \omega_{\mathrm{B}} \cdot \sqrt{\frac{G_{\mathrm{B}} \cdot a_1 b_2}{a_1 + a_2}}. \tag{7}$$

Selection of C_1: if C_1 serves also as a commutation capacitor of a converter, it carries large a.c. currents. Therefore its capacitance must often be selected according to the current capability, in order to limit the temperature rise and to prevent early aging.

Selection of L_1: the inductance L_1 should be optimized for a reasonable ripple current. For cost reasons L_1 should be as low as possible, but a too low inductance results in an excessive ripple current. As an example, Fig. 3 shows the inductor ripple current for a buck converter.

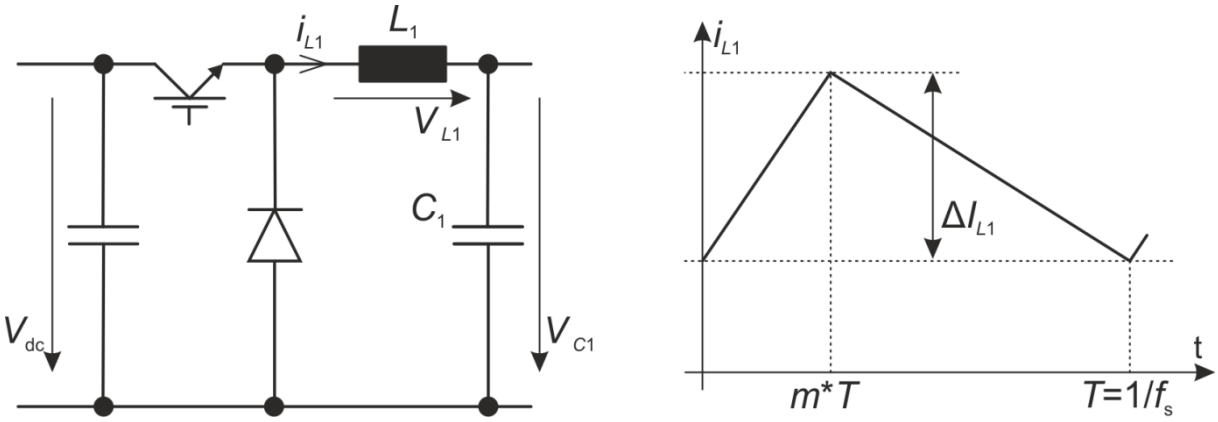


Fig. 3: Ripple current in the inductor L_1 of a buck converter

If m is the duty cycle of the switch, the d.c. voltage across C_1 is $m*V_{dc}$. When the switch is on, the current in L_1 increases and the peak–peak ripple current ΔI_{L1} can be calculated as

$$V_{L1} = L_1 \cdot \frac{\mathrm{d}i_{L1}}{\mathrm{d}t} = V_{\mathrm{dc}} - V_{C1} = V_{\mathrm{dc}} \cdot (1 - m)\,,$$

$$\Delta I_{L1} = m \cdot T \cdot \frac{\mathrm{d}i_{L1}}{\mathrm{d}t} = m \cdot \frac{1}{f_{\mathrm{s}}} \cdot \frac{V_{\mathrm{dc}} \cdot (1 - m)}{L_1} = \frac{V_{\mathrm{dc}} \cdot (1 - m) \cdot m}{f_{\mathrm{s}} \cdot L_1}\,.$$

The function $(1 - m)*m$ has its maximum of 0.25 at $m = 0.5$. Therefore, L_1 can be calculated as:

$$L_1 = \frac{V_{\mathrm{dc}} \cdot 0.25}{f_{\mathrm{s}} \cdot \Delta I_{L1}} \tag{8a}$$

Figure 4 illustrates an alternative approach to determine L_1 for sinusoidal ripple currents and voltages.

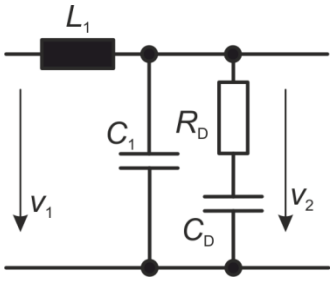


Fig. 4: Ripple current in the inductor L_1 for sinusoidal ripple currents and voltages

The filter eliminates the voltage ripple of v_1 nearly entirely, so the voltage ripple in v_2 is much smaller. Therefore, the a.c. ripple of v_1 (with frequency f_1) is also present across L_1 and generates a ripple current in L_1:

$$I_{L1\_\mathrm{ripple\_peak\_peak}} = \frac{v_{1\_\mathrm{ripple\_peak\_peak}}}{2 \cdot \pi \cdot f_1 \cdot L_1}\,,$$

$$L_1 = \frac{v_{1\_\mathrm{ripple\_peak\_peak}}}{2 \cdot \pi \cdot f_1 \cdot I_{L1\_\mathrm{ripple\_peak\_peak}}}\,. \tag{8b}$$

As mentioned before, we have the choice to preselect two of the three parameters C_1, L_1, and ω_0. By substituting Eq. (6a) into Eq. (6c) we get an equation that can be solved for the remaining parameter:

$$C_1 = \frac{a_1 b_2}{L_1 {\omega_0}^2 (a_1 + a_2)}, \tag{9a}$$

$$L_1 = \frac{a_1 b_2}{C_1 {\omega_0}^2 (a_1 + a_2)}, \tag{9b}$$

$$\omega_0 = \sqrt{\frac{a_1 b_2}{L_1 C_1 (a_1 + a_2)}}. \tag{9c}$$

By solving Eq. (6b) for C_D we get

$$C_\mathrm{D} = \frac{a_1 a_2 + b_2}{L_1 {\omega_0}^2} - C_1. \tag{10}$$

By solving Eq. (6a) for R_D we get

$$R_\mathrm{D} = \frac{a_1 + a_2}{C_\mathrm{D} \omega_0}. \tag{11}$$

Example 1: Design a second-order filter, which will be placed between a diode rectifier and a buck converter according to Fig. 5 and will reduce the 300 Hz ripple voltage from the rectifier bridge. The d.c.-link voltage is 200 V and the ripple current in L_1 must not exceed 50 A peak to peak. The design of the buck converter has shown that C_1 needs to be 22 mF to get a reasonable capacitor current. Make the design for all three given optimization methods and compare the results.

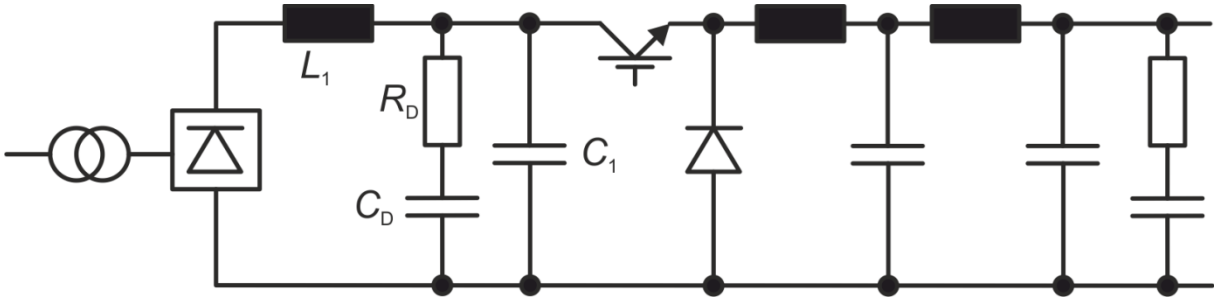


Fig. 5: Input filter for a buck converter

The diode rectifier produces a 300 Hz voltage ripple of approximately 13% of 200 V, i.e., 26 V peak to peak. To keep it simple, we consider this ripple to be sinusoidal. That means we can determine L_1 according to Eq. (8b) as follows:

$$L_1 = \frac{v_{1\_\mathrm{ripple\_peak\_peak}}}{2 \cdot \pi \cdot f_1 \cdot I_{L1\_\mathrm{ripple\_peak\_peak}}} = \frac{26\ \mathrm{V\ peak\ to\ peak}}{2 \cdot \pi \cdot 300\ \mathrm{s^{-1}} \cdot 50\ \mathrm{A\ peak\ to\ peak}} = 276\ \mu\mathrm{H}.$$

Select L_1 = 300 μH and C_1 = 22 mF and calculate the remaining filter components by using Eqs. (9c), (10), and (11). The results are listed in Table 3.

Table 3: Results for Example 1

Parameter	Butterworth	Bessel	Critical damping
ω_0	275 s^{-1}	177 s^{-1}	115 s^{-1}
f_0	44 Hz	28 Hz	18 Hz
L_1	300 μH	300 μH	300 μH
C_1	22 mF	22 mF	22 mF
C_D	66 mF	110 mF	176 mF
R_D	0.11 Ω	0.09 Ω	0.08 Ω

Figure 6 shows the Bode plots of the three filter designs according to Example 1. The three designs differ only around the cut-off frequency. In the Butterworth optimization C_D is minimal but with the drawback of a high resonance gain of 4.5 dB. With critical damping, this resonance gain is reduced to 2.3 dB with the drawback of a large C_D. The Bessel optimization is between the two and could be a good compromise.

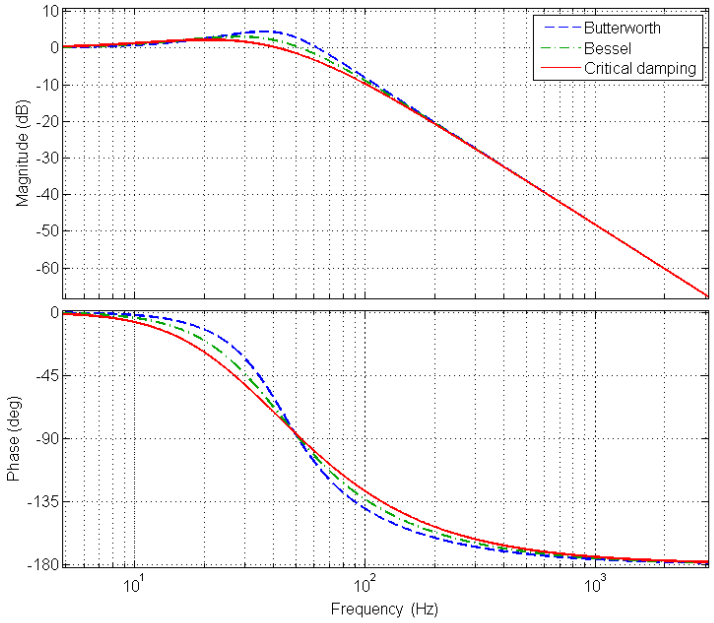


Fig. 6: Bode plots for the filter designs according to Example 1

Example 2: Design a second-order filter for a buck converter with a d.c.-link voltage of 120 V, a switching frequency of 20 kHz, and a maximum output current of 500 A; refer to Fig. 7. The ripple current in L_1 should not exceed 50 A peak to peak. The filter should have an attenuation of 0.004 at the switching frequency. Design the filter for all three optimization methods and compare the results.

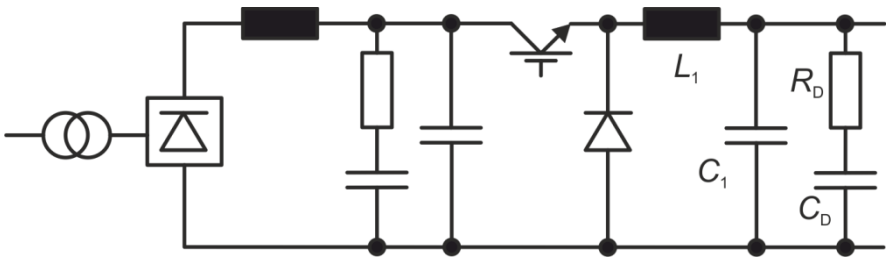


Fig. 7: Output filter for a buck converter

Select L_1 in order to meet the ripple requirement by using Eq. (8a):

$$L_1 = \frac{V_{\mathrm{dc}} \cdot 0.25}{f_{\mathrm{s}} \cdot \Delta I_{L1}} = \frac{120\ \mathrm{V} \cdot 0.25}{20\ \mathrm{kHz} \cdot 50\ \mathrm{A}} = 30\ \mu\mathrm{H}.$$

Select ω_0 in order to meet the attenuation requirement by using Eq. (7):

$$\omega_0 = \omega_{\mathrm{B}} \cdot \sqrt{\frac{G_{\mathrm{B}} \cdot a_1 b_2}{a_1 + a_2}} = 2 \cdot \pi \cdot 20\ \mathrm{kHz} \cdot \sqrt{\frac{0.004 \cdot a_1 b_2}{a_1 + a_2}}.$$

Calculate the remaining filter components by using Eqs. (9a), (10), and (11). The results are listed in Table 4.

Table 4: Results for Example 2

Parameter	Butterworth	Bessel	Critical damping
ω_0	5620 s^{-1}	3600 s^{-1}	2340 s^{-1}
f_0	890 Hz	570 Hz	370 Hz
L_1	30 μH	30 μH	30 μH
C_1	528 μF	528 μF	528 μF
C_{D}	1580 μF	2640 μF	4220 μF
R_{D}	0.22 Ω	0.18 Ω	0.15 Ω

Figure 8 shows the Bode plots of the three filter designs according to Example 2. The Bode plots are similar to the ones for Example 1 except for the frequency scaling. The attenuation at 20 kHz is –48 dB, which corresponds to a factor of 0.004, as required. The same trade-off between small capacitor values and low resonance amplitude applies; refer to Example 1.

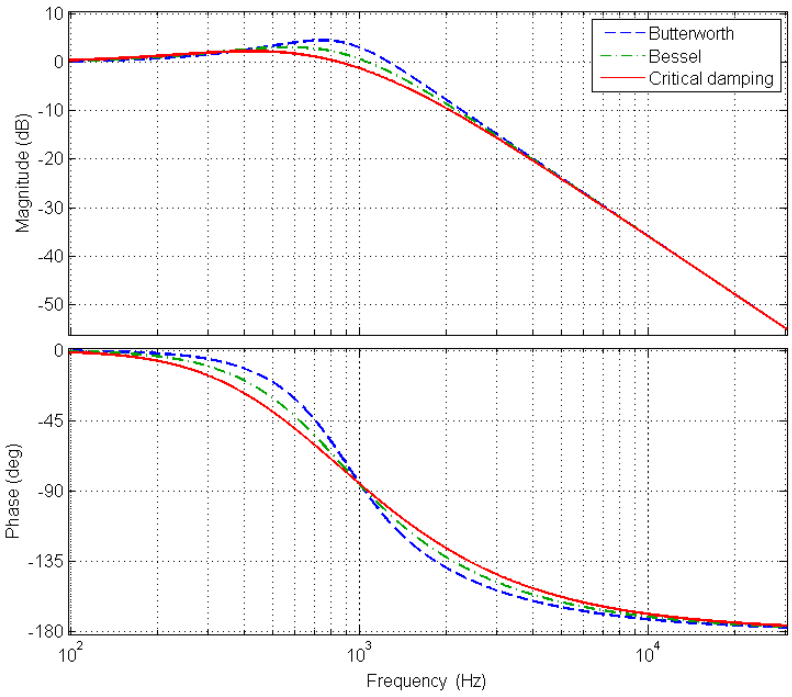


Fig. 8: Bode plots for the filter designs according to Example 2

3 Design of a fourth-order low-pass filter

For the fourth-order low-pass filter there are two alternatives. One of them has the *RC*-damping circuit in the first, the other one in the second *LC* stage. Both alternatives are outlined in detail in Sections 3.1 and 3.2, respectively, and are compared with each other in Section 4.

3.1 Fourth-order low-pass filter with damping circuit in the first *LC* stage

In this section a low-pass filter according to Fig. 9 is outlined.

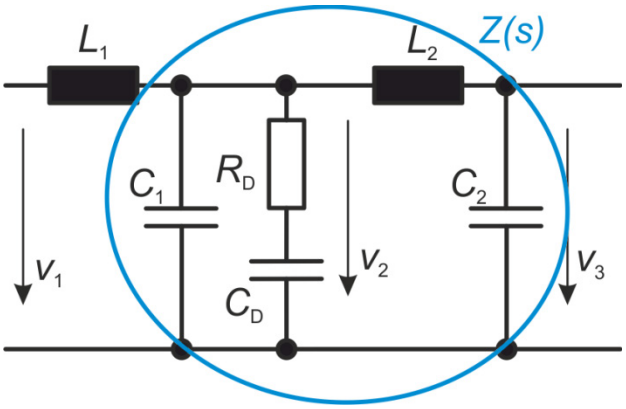


Fig. 9: Fourth-order low-pass filter with *RC* damping in the first *LC* stage

The complex impedance $Z(s)$ is

$$Z(s) = \frac{1}{C_1 s + \dfrac{1}{R_\mathrm{D} + \dfrac{1}{C_\mathrm{D} s}} + \dfrac{1}{L_2 s + \dfrac{1}{C_2 s}}} = \frac{1}{C_1 s + \dfrac{C_\mathrm{D} s}{R_\mathrm{D} C_\mathrm{D} s + 1} + \dfrac{C_2 s}{L_2 C_2 s^2 + 1}}$$

$$= \frac{(L_2 C_2 s^2 + 1) \cdot (R_\mathrm{D} C_\mathrm{D} s + 1)}{C_1 s \cdot (L_2 C_2 s^2 + 1) \cdot (R_\mathrm{D} C_\mathrm{D} s + 1) + C_\mathrm{D} s \cdot (L_2 C_2 s^2 + 1) + C_2 s \cdot (R_\mathrm{D} C_\mathrm{D} s + 1)}$$

$$= \frac{(L_2 C_2 s^2 + 1) \cdot (R_\mathrm{D} C_\mathrm{D} s + 1)}{L_2 C_1 C_2 R_\mathrm{D} C_\mathrm{D} s^4 + L_2 C_1 C_2 s^3 + C_1 R_\mathrm{D} C_\mathrm{D} s^2 + C_1 s + L_2 C_2 C_\mathrm{D} s^3 + C_\mathrm{D} s + C_2 R_\mathrm{D} C_\mathrm{D} s^2 + C_2 s};$$

$$Z(s) = \frac{(L_2 C_2 s^2 + 1) \cdot (R_\mathrm{D} C_\mathrm{D} s + 1)}{L_2 C_1 C_2 R_\mathrm{D} C_\mathrm{D} s^4 + L_2 C_2 (C_1 + C_\mathrm{D}) s^3 + R_\mathrm{D} C_\mathrm{D} (C_1 + C_2) s^2 + (C_1 + C_2 + C_\mathrm{D}) s}. \qquad (12)$$

The transfer function can be split into two partial transfer functions $G_1(s)$ and $G_2(s)$:

$$G(s) = G_1(s) \cdot G_2(s) = \frac{v_2(s)}{v_1(s)} \cdot \frac{v_3(s)}{v_2(s)} = \frac{v_3(s)}{v_1(s)};$$

$$G_1(s) = \frac{v_2(s)}{v_1(s)} = \frac{Z(s)}{L_1 s + Z(s)}$$

$$= \frac{\dfrac{(L_2 C_2 s^2 + 1) \cdot (R_\mathrm{D} C_\mathrm{D} s + 1)}{L_2 C_1 C_2 R_\mathrm{D} C_\mathrm{D} s^4 + L_2 C_2 (C_1 + C_\mathrm{D}) s^3 + R_\mathrm{D} C_\mathrm{D} (C_1 + C_2) s^2 + (C_1 + C_2 + C_\mathrm{D}) s}}{L_1 s + \dfrac{(L_2 C_2 s^2 + 1) \cdot (R_\mathrm{D} C_\mathrm{D} s + 1)}{L_2 C_1 C_2 R_\mathrm{D} C_\mathrm{D} s^4 + L_2 C_2 (C_1 + C_\mathrm{D}) s^3 + R_\mathrm{D} C_\mathrm{D} (C_1 + C_2) s^2 + (C_1 + C_2 + C_\mathrm{D}) s}}$$

$$= \frac{(L_2C_2s^2+1)\cdot(R_\mathrm{D}C_\mathrm{D}s+1)}{L_1L_2C_1C_2R_\mathrm{D}C_\mathrm{D}s^5 + L_1L_2C_2(C_1+C_\mathrm{D})s^4 + L_1R_\mathrm{D}C_\mathrm{D}(C_1+C_2)s^3+\cdots}\cdots$$

$$\cdots\frac{\cdots}{\cdots + L_1(C_1+C_2+C_\mathrm{D})s^2 + L_2C_2R_\mathrm{D}C_\mathrm{D}s^3 + L_2C_2s^2 + R_\mathrm{D}C_\mathrm{D}s+1};$$

$$G_1(s) = \frac{(L_2C_2s^2+1)\cdot(R_\mathrm{D}C_\mathrm{D}s+1)}{L_1L_2C_1C_2R_\mathrm{D}C_\mathrm{D}s^5 + L_1L_2C_2(C_1+C_\mathrm{D})s^4 + R_\mathrm{D}C_\mathrm{D}[L_1(C_1+C_2)+L_2C_2]s^3+\cdots}\cdots$$

$$\cdots\frac{\cdots}{\ldots + [L_1(C_1+C_2+C_\mathrm{D})+L_2C_2]s^2 + R_\mathrm{D}C_\mathrm{D}s+1};$$

$$G_2(s) = \frac{\frac{1}{C_2s}}{L_2s+\frac{1}{C_2s}} = \frac{1}{L_2C_2s^2+1};$$

$$G(s) = G_1(s)\cdot G_2(s);$$

$$G(s) = \frac{R_\mathrm{D}C_\mathrm{D}s+1}{L_1L_2C_1C_2R_\mathrm{D}C_\mathrm{D}s^5 + L_1L_2C_2(C_1+C_\mathrm{D})s^4 + R_\mathrm{D}C_\mathrm{D}[L_1(C_1+C_2)+L_2C_2]s^3+\cdots}\cdots \quad (13)$$

$$\cdots\frac{\cdots}{\ldots + [L_1(C_1+C_2+C_\mathrm{D})+L_2C_2]s^2 + R_\mathrm{D}C_\mathrm{D}s+1}.$$

Note that the *s* terms in the numerator and the denominator are equal. Therefore we can write Eq. (13) as follows:

$$G(s) = \frac{k_1s+1}{k_5s^5+k_4s^4+k_3s^3+k_2s^2+k_1s+1} \quad (14a)$$

$$\text{with} \quad k_1 = R_\mathrm{D}C_\mathrm{D}, \quad (14b)$$

$$k_2 = L_1(C_1+C_2+C_\mathrm{D}) + L_2C_2, \quad (14c)$$

$$k_3 = R_\mathrm{D}C_\mathrm{D}(L_1C_1+L_2C_2+L_1C_2), \quad (14d)$$

$$k_4 = L_1L_2C_2(C_1+C_\mathrm{D}), \quad (14e)$$

$$k_5 = L_1L_2C_1C_2C_\mathrm{D}R_\mathrm{D}. \quad (14f)$$

G(*s*) can be expressed as the combination of a fifth-order PT and a first-order PD. Let us have a closer look at the fifth-order PT, which is the denominator part of *G*(*s*). This can be split in two second-order PTs and one first-order PT, all connected in series. It can be expressed in its normalized form as

$$G_\mathrm{PT}(s) = \frac{1}{(1+a_1\frac{s}{\omega_0})\cdot(1+a_2\frac{s}{\omega_0}+b_2\frac{s^2}{{\omega_0}^2})\cdot(1+a_3\frac{s}{\omega_0}+b_3\frac{s^2}{{\omega_0}^2})}. \quad (15)$$

The transfer function of such a combination of first- and second-order PTs can be optimized according to different methods [1], which results in particular values for a_i and b_i. The commonly used optimization methods with their corresponding coefficients are given in Table 5.

Table 5: Coefficients for a fifth-order PT for different optimization methods

Method	a_1	a_2	b_2	a_3	b_3
Butterworth	1.0000	1.6180	1.0000	0.6180	1.0000
Bessel	0.6656	1.1402	0.4128	0.6216	0.3245
Critical damping	0.3856	0.7712	0.1487	0.7712	0.1487

By expanding Eq. (15) we get

$$G_{\mathrm{PT}}(s) = \frac{1}{(1 + \frac{a_2}{\omega_0}s + \frac{b_2}{{\omega_0}^2}s^2 + \frac{a_1}{\omega_0}s + \frac{a_1a_2}{{\omega_0}^2}s^2 + \frac{a_1b_2}{{\omega_0}^3}s^3) \cdot (1 + \frac{a_3}{\omega_0}s + \frac{b_3}{{\omega_0}^2}s^2)}$$

$$= \frac{1}{1 + \frac{a_3}{\omega_0}s + \frac{b_3}{{\omega_0}^2}s^2 + \frac{a_2}{\omega_0}s + \frac{a_2a_3}{{\omega_0}^2}s^2 + \frac{a_2b_3}{{\omega_0}^3}s^3 + \frac{b_2}{{\omega_0}^2}s^2 + \frac{a_3b_2}{{\omega_0}^3}s^3 + \cdots} \cdots$$

$$\cdots \frac{\cdots}{\cdots + \frac{b_2b_3}{{\omega_0}^4}s^4 + \frac{a_1}{\omega_0}s + \frac{a_1a_3}{{\omega_0}^2}s^2 + \frac{a_1b_3}{{\omega_0}^3}s^3 + \frac{a_1a_2}{{\omega_0}^2}s^2 + \frac{a_1a_2a_3}{{\omega_0}^3}s^3 + \cdots} \cdots$$

$$\cdots \frac{\cdots}{\cdots + \frac{a_1a_2b_3}{{\omega_0}^4}s^4 + \frac{a_1b_2}{{\omega_0}^3}s^3 + \frac{a_1a_3b_2}{{\omega_0}^4}s^4 + \frac{a_1b_2b_3}{{\omega_0}^5}s^5};$$

$$G_{PT}(s) = \frac{1}{\frac{a_1b_2b_3}{{\omega_0}^5}s^5 + \frac{(b_2b_3 + a_1a_2b_3 + a_1a_3b_2)}{{\omega_0}^4}s^4 + \cdots} \cdots \tag{16}$$

$$\cdots \frac{\cdots}{\cdots + \frac{(a_2b_3 + a_3b_2 + a_1b_3 + a_1a_2a_3 + a_1b_2)}{{\omega_0}^3}s^3 + \cdots} \cdots$$

$$\cdots \frac{\cdots}{\cdots + \frac{(b_3 + a_2a_3 + b_2 + a_1a_3 + a_1a_2)}{{\omega_0}^2}s^2 + \frac{(a_1 + a_2 + a_3)}{\omega_0}s + 1}.$$

By comparing the coefficients with Eq. (14a) we get

$$k_1 = R_{\mathrm{D}}C_{\mathrm{D}} = \frac{a_1 + a_2 + a_3}{\omega_0}; \tag{17a}$$

$$k_2 = L_1(C_1 + C_2 + C_{\mathrm{D}}) + L_2C_2 = \frac{b_3 + a_2a_3 + b_2 + a_1a_3 + a_1a_2}{{\omega_0}^2}; \tag{17b}$$

$$k_3 = R_\mathrm{D}C_\mathrm{D}(L_1C_1 + L_2C_2 + L_1C_2) = \frac{a_2b_3 + a_3b_2 + a_1b_3 + a_1a_2a_3 + a_1b_2}{{\omega_0}^3}; \tag{17c}$$

$$k_4 = L_1L_2C_2(C_1 + C_\mathrm{D}) = \frac{b_2b_3 + a_1a_2b_3 + a_1a_3b_2}{{\omega_0}^4}; \tag{17d}$$

$$k_5 = L_1L_2C_1C_2C_DR_D = \frac{a_1b_2b_3}{{\omega_0}^5}. \tag{17e}$$

For a given optimization method, the five independent Eqs. (17a)–(17e) contain seven unknowns (L_1, L_2, C_1, C_2, R_D, C_D, and ω_0). Therefore, we have the choice to select two of them and the remaining five depend on that selection; here we preselect ω_0 and L_1. Refer to Section 2 for the evaluation of L_1.

Selection of the cut-off angular frequency ω_0: For a given angular frequency ω_B well in the blocking area of the filter ($\omega_\mathrm{B} >> \omega_0$) we can define the desired attenuation G_B. In the blocking area the highest-order terms of both the numerator and the denominator in Eq. (13) dominate, therefore it can be simplified to

$$G_\mathrm{B} = \frac{R_\mathrm{D}C_\mathrm{D}s}{L_1L_2C_1C_2R_\mathrm{D}C_\mathrm{D}s^5} = \frac{\frac{a_1 + a_2 + a_3}{\omega_0}s}{\frac{a_1b_2b_3}{{\omega_0}^5}s^5} = \frac{a_1 + a_2 + a_3}{a_1b_2b_3} \cdot \frac{{\omega_0}^4}{s^4} = \frac{a_1 + a_2 + a_3}{a_1b_2b_3} \cdot \frac{{\omega_0}^4}{{\omega_B}^4},$$

$$\omega_0 = \omega_\mathrm{B} \cdot \sqrt[4]{\frac{G_\mathrm{B} \cdot a_1b_2b_3}{a_1 + a_2 + a_3}}. \tag{18}$$

The cut-off angular frequency ω_0 of the filter depends only on the required attenuation and on the selected optimization method. The equation system (17a)–(17e) has to be solved for L_2, C_1, C_2, R_D, and C_D.

By solving Eq. (17a) for C_D and substituting C_D into Eqs. (17b)–(17e) we reduce the system to four equations:

$$k_2 = L_1\left(C_1 + C_2 + \frac{k_1}{R_\mathrm{D}}\right) + L_2C_2; \tag{19a}$$

$$k_3 = k_1(L_1C_1 + L_2C_2 + L_1C_2); \tag{19b}$$

$$k_4 = L_1L_2C_2\left(C_1 + \frac{k_1}{R_\mathrm{D}}\right); \tag{19c}$$

$$k_5 = k_1L_1L_2C_1C_2\,. \tag{19d}$$

By dividing Eq. (19c) by Eq. (19d) we get

$$\frac{k_4}{k_5} = \frac{L_1L_2C_2\left(C_1 + \frac{k_1}{R_\mathrm{D}}\right)}{k_1L_1L_2C_1C_2} = \frac{\left(C_1 + \frac{k_1}{R_\mathrm{D}}\right)}{k_1C_1} = \frac{1}{k_1} + \frac{1}{C_1R_\mathrm{D}},$$

$$k_1k_4R_\mathrm{D}C_1 - k_5R_\mathrm{D}C_1 = k_1k_5,$$

$$R_{\mathrm{D}} = \frac{k_1 k_5}{C_1(k_1 k_4 - k_5)}. \tag{20}$$

By substituting Eq. (20) in Eq. (19a) we reduce the system further to three equations:

$$k_2 = L_1\left(C_1 + C_2 + \frac{k_1 C_1(k_1 k_4 - k_5)}{k_1 k_5}\right) + L_2 C_2,$$

$$= L_1\left(C_2 + C_1(1 + \frac{k_1 k_4}{k_5} - 1)\right) + L_2 C_2 = L_1 C_2 + L_1 C_1 \frac{k_1 k_4}{k_5} + L_2 C_2,$$

$$= (L_1 + L_2)C_2 + L_1 C_1 \frac{k_1 k_4}{k_5}; \tag{21a}$$

$$k_3 = k_1(L_1 C_1 + L_2 C_2 + L_1 C_2)\,; \tag{21b}$$

$$k_5 = k_1 L_1 L_2 C_1 C_2\,. \tag{21c}$$

By solving Eq. (21c) for C_1 and substituting C_1 in Eqs. (21a) and (21b), we reduce the system further to two equations:

$$k_2 = (L_1 + L_2)C_2 + L_1 \cdot \frac{k_5}{k_1 L_1 L_2 C_2} \cdot \frac{k_1 k_4}{k_5} = C_2(L_1 + L_2) + \frac{k_4}{L_2 C_2}, \tag{22a}$$

$$k_3 = k_1\left(L_1 \cdot \frac{k_5}{k_1 L_1 L_2 C_2} + L_2 C_2 + L_1 C_2\right) = k_1 C_2(L_1 + L_2) + \frac{k_5}{L_2 C_2}. \tag{22b}$$

By subtracting Eq. (22b) from Eq. (22a) we get

$$k_2 - \frac{k_3}{k_1} = \frac{k_1 k_2 - k_3}{k_1} = C_2(L_1 + L_2) + \frac{k_4}{L_2 C_2} - C_2(L_1 + L_2) - \frac{k_5}{k_1 L_2 C_2} = \frac{k_1 k_4 - k_5}{k_1 L_2 C_2};$$

$$C_2 = \frac{k_1 k_4 - k_5}{L_2(k_1 k_2 - k_3)}. \tag{23}$$

By substituting Eq. (23) in Eq. (22a) we get

$$k_2 = \frac{(k_1 k_4 - k_5)\cdot(L_1 + L_2)}{L_2(k_1 k_2 - k_3)} + \frac{k_4 L_2(k_1 k_2 - k_3)}{L_2(k_1 k_4 - k_5)};$$

$$\frac{(k_1 k_4 - k_5)\cdot(L_1 + L_2)}{L_2(k_1 k_2 - k_3)} = k_2 - \frac{k_4(k_1 k_2 - k_3)}{k_1 k_4 - k_5} = \frac{k_1 k_2 k_4 - k_2 k_5 - k_1 k_2 k_4 + k_3 k_4}{k_1 k_4 - k_5}$$
$$= \frac{k_3 k_4 - k_2 k_5}{k_1 k_4 - k_5};$$

$$\frac{L_1 + L_2}{L_2} = \frac{L_1}{L_2} + 1 = \frac{(k_3 k_4 - k_2 k_5)\cdot(k_1 k_2 - k_3)}{(k_1 k_4 - k_5)^2};$$

$$L_1 = L_2\left[\frac{(k_3 k_4 - k_2 k_5)\cdot(k_1 k_2 - k_3)}{(k_1 k_4 - k_5)^2} - 1\right];$$

$$L_2 = \frac{L_1}{\frac{(k_3k_4 - k_2k_5)\cdot(k_1k_2 - k_3)}{(k_1k_4 - k_5)^2} - 1}. \tag{24}$$

Example 3: Design a fourth-order filter for a buck converter with a d.c.-link voltage of 120 V, a switching frequency of 20 kHz, and a maximum output current of 500 A; refer to Fig. 10. The ripple current in L_1 should not exceed 50 A peak to peak. The filter should have an attenuation of 0.004 at the switching frequency. Design the filter for all three optimization methods and compare the results. In order to enable a comparison between different filter structures (refer to Section 4), the same parameters are given as in Example 2.

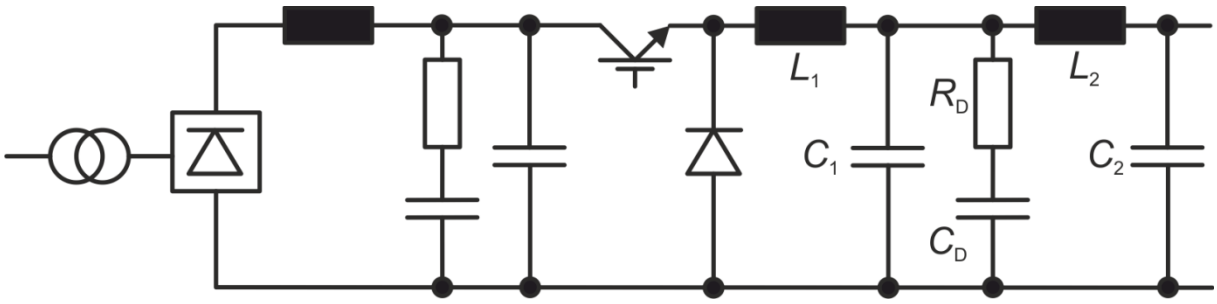


Fig. 10: Output filter for a buck converter

Select L_1 in order to meet the ripple requirement by using Eq. (8a):

$$L_1 = \frac{V_{\mathrm{dc}} \cdot 0.25}{f_{\mathrm{s}} \cdot \Delta I_{L1}} = \frac{120\ \mathrm{V} \cdot 0.25}{20\ \mathrm{kHz} \cdot 50\ \mathrm{A}} = 30\ \mu\mathrm{H}.$$

Select ω_0 in order to meet the attenuation requirement by using Eq. (18):

$$\omega_0 = \omega_{\mathrm{B}} \cdot \sqrt[4]{\frac{G_{\mathrm{B}} \cdot a_1 b_2 b_3}{a_1 + a_2 + a_3}} = 2 \cdot \pi \cdot 20\ \mathrm{kHz} \cdot \sqrt[4]{\frac{0.004 \cdot a_1 b_2 b_3}{a_1 + a_2 + a_3}}.$$

Calculate the remaining filter components by using Eqs. (24), (23), (21c), (20), and (17a) in that order. The results are listed in Table 6. Depending on the selected optimization method, L_2 is approximately either double, equal to, or half the size of L_1. This leads to a simplified design as L_1 and L_2 can be realized with either two or three identical chokes.

Table 6: Results for Example 3

Parameter	Butterworth	Bessel	Critical damping
ω_0	23,600 s^{-1}	13,800 s^{-1}	8200 s^{-1}
f_0	3.75 kHz	2.20 kHz	1.30 kHz
L_1	30 μH	30 μH	30 μH
L_2	57 μH	31 μH	17 μH
C_1	23 μF	24 μF	25 μF
C_2	26 μF	44 μF	80 μF
C_{D}	217 μF	342 μF	597 μF
R_{D}	0.63 Ω	0.51 Ω	0.40 Ω

Figure 11 shows the Bode plots of the three filter designs according to Example 3. The attenuation at 20 kHz is –48 dB, which corresponds to a factor of 0.004, as required. Compared to the second-order filter (see Fig. 8) the resonance amplitudes are slightly higher and the same trade-off between small capacitor values and low resonance amplitudes applies.

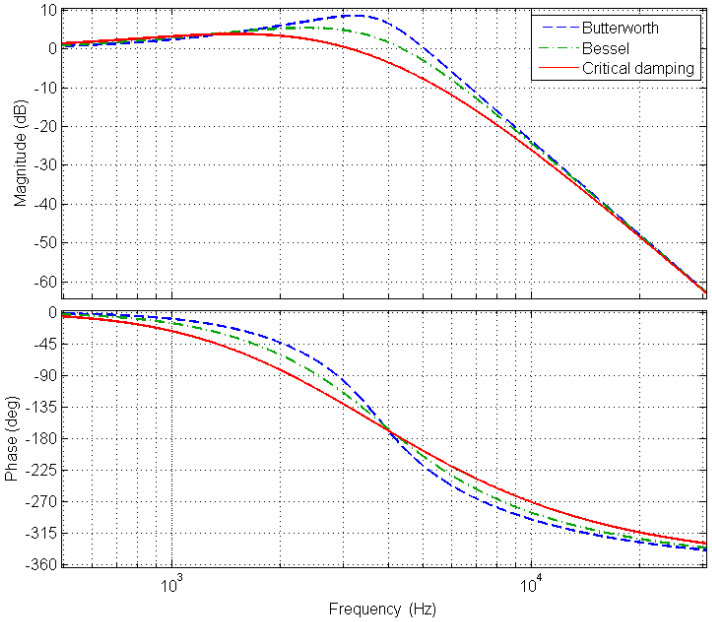


Fig. 11: Bode plots for the filter designs according to Example 3

3.2 Fourth-order low-pass filter with damping circuit in the second *LC* stage

In this section a low-pass filter according to Fig. 12 is outlined. The derivation is similar to the one in Section 3.1. For the sake of completeness it is repeated in detail.

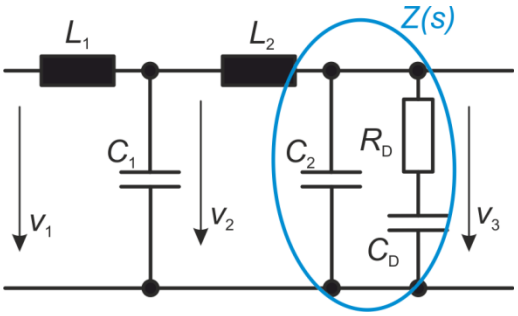


Fig. 12: Fourth-order low-pass filter with *RC* damping in the second *LC* stage

The complex impedance $Z(s)$ is given by

$$Z(s) = \frac{1}{C_2 s + \dfrac{1}{R_\mathrm{D} + \dfrac{1}{C_\mathrm{D} s}}} = \frac{1}{C_2 s + \dfrac{C_\mathrm{D} s}{R_\mathrm{D} C_\mathrm{D} s + 1}} = \frac{R_\mathrm{D} C_\mathrm{D} s + 1}{C_2 R_\mathrm{D} C_\mathrm{D} s^2 + (C_2 + C_\mathrm{D}) s}. \tag{25}$$

The transfer function can be split into two partial transfer functions $G_1(s)$ and $G_2(s)$:

$$G(s) = G_1(s) \cdot G_2(s) = \frac{v_2(s)}{v_1(s)} \cdot \frac{v_3(s)}{v_2(s)} = \frac{v_3(s)}{v_1(s)};$$

$$G_1(s) = \frac{\dfrac{1}{C_1 s + \dfrac{1}{L_2 s + Z(s)}}}{L_1 s + \dfrac{1}{C_1 s + \dfrac{1}{L_2 s + Z(s)}}} = \frac{\dfrac{L_2 s + Z(s)}{C_1 L_2 s^2 + C_1 Z(s) s + 1}}{L_1 s + \dfrac{L_2 s + Z(s)}{C_1 L_2 s^2 + C_1 Z(s) s + 1}}$$

$$= \frac{L_2 s + Z(s)}{L_1 L_2 C_1 s^3 + L_1 C_1 Z(s) s^2 + (L_1 + L_2) s + Z(s)};$$

$$G_2(s) = \frac{Z(s)}{L_2 s + Z(s)};$$

$$G(s) = G_1(s) \cdot G_2(s) = \frac{Z(s)}{L_1 L_2 C_1 s^3 + L_1 C_1 Z(s) s^2 + (L_1 + L_2) s + Z(s)}$$

$$= \frac{\dfrac{R_\mathrm{D} C_\mathrm{D} s + 1}{C_2 R_\mathrm{D} C_\mathrm{D} s^2 + (C_2 + C_\mathrm{D}) s}}{L_1 L_2 C_1 s^3 + \dfrac{L_1 C_1 R_\mathrm{D} C_\mathrm{D} s + L_1 C_1}{C_2 R_\mathrm{D} C_\mathrm{D} s^2 + (C_2 + C_\mathrm{D}) s} s^2 + (L_1 + L_2) s + \dfrac{R_\mathrm{D} C_\mathrm{D} s + 1}{C_2 R_\mathrm{D} C_\mathrm{D} s^2 + (C_2 + C_\mathrm{D}) s}}$$

$$= \frac{R_\mathrm{D} C_\mathrm{D} s + 1}{L_1 L_2 C_1 C_2 R_\mathrm{D} C_\mathrm{D} s^5 + (C_2 + C_\mathrm{D}) L_1 L_2 C_1 s^4 + L_1 C_1 R_\mathrm{D} C_\mathrm{D} s^3 + L_1 C_1 s^2 + \cdots} \cdots \quad (26)$$

$$\cdots \frac{\cdots}{\cdots + (L_1 + L_2) C_2 R_\mathrm{D} C_\mathrm{D} s^3 + (L_1 + L_2)(C_2 + C_\mathrm{D}) s^2 + R_\mathrm{D} C_\mathrm{D} s + 1};$$

$$G(s) = \frac{R_\mathrm{D} C_\mathrm{D} s + 1}{L_1 L_2 C_1 C_2 R_\mathrm{D} C_\mathrm{D} s^5 + (C_2 + C_\mathrm{D}) L_1 L_2 C_1 s^4 + \cdots} \cdots$$

$$\cdots \frac{\cdots}{\cdots + [L_1 C_1 R_\mathrm{D} C_\mathrm{D} + (L_1 + L_2) C_2 R_\mathrm{D} C_\mathrm{D}] s^3 + [L_1 C_1 + (L_1 + L_2)(C_2 + C_\mathrm{D})] s^2 + R_\mathrm{D} C_\mathrm{D} s + 1}.$$

Note that the *s* terms in the numerator and the denominator are equal. Therefore we can write Eq. (26) as

$$G(s) = \frac{k_1 s + 1}{k_5 s^5 + k_4 s^4 + k_3 s^3 + k_2 s^2 + k_1 s + 1}, \quad (27a)$$

$$\text{with} \quad k_1 = R_\mathrm{D} C_\mathrm{D}; \quad (27b)$$

$$k_2 = L_1 (C_1 + C_2 + C_\mathrm{D}) + L_2 (C_2 + C_\mathrm{D}); \quad (27c)$$

$$k_3 = R_\mathrm{D} C_\mathrm{D} (L_1 C_1 + L_2 C_2 + L_1 C_2); \quad (27d)$$

$$k_4 = L_1 L_2 C_1 (C_2 + C_\mathrm{D}); \quad (27e)$$

$$k_5 = L_1 L_2 C_1 C_2 C_\mathrm{D} R_\mathrm{D}. \quad (27f)$$

G(*s*) can be expressed as the combination of a fifth-order PT and a first-order PD. Let us take a closer look at the fifth-order PT, which is the denominator part of *G*(*s*). This can be split in two

second-order PTs and one first-order PT, all connected in series. It can be expressed in its normalized form as

$$G_{\mathrm{PT}}(s) = \frac{1}{(1 + a_1 \frac{s}{\omega_0}) \cdot (1 + a_2 \frac{s}{\omega_0} + b_2 \frac{s^2}{{\omega_0}^2}) \cdot (1 + a_3 \frac{s}{\omega_0} + b_3 \frac{s^2}{{\omega_0}^2})}. \tag{28}$$

The transfer function of such a combination of first- and second-order PTs can be optimized according to different methods [1], which results in particular values for a_i and b_i. The commonly used optimization methods with their corresponding coefficients are given in Table 7.

Table 7: Coefficients for a fifth-order PT for different optimization methods

Method	a_1	a_2	b_2	a_3	b_3
Butterworth	1.0000	1.6180	1.0000	0.6180	1.0000
Bessel	0.6656	1.1402	0.4128	0.6216	0.3245
Critical damping	0.3856	0.7712	0.1487	0.7712	0.1487

By expanding Eq. (28) we get

$$G_{\mathrm{PT}}(s) = \frac{1}{(1 + \frac{a_2}{\omega_0} s + \frac{b_2}{{\omega_0}^2} s^2 + \frac{a_1}{\omega_0} s + \frac{a_1 a_2}{{\omega_0}^2} s^2 + \frac{a_1 b_2}{{\omega_0}^3} s^3) \cdot (1 + \frac{a_3}{\omega_0} s + \frac{b_3}{{\omega_0}^2} s^2)}$$

$$= \frac{1}{1 + \frac{a_3}{\omega_0} s + \frac{b_3}{{\omega_0}^2} s^2 + \frac{a_2}{\omega_0} s + \frac{a_2 a_3}{{\omega_0}^2} s^2 + \frac{a_2 b_3}{{\omega_0}^3} s^3 + \frac{b_2}{{\omega_0}^2} s^2 + \frac{a_3 b_2}{{\omega_0}^3} s^3 + \cdots} \cdots$$

$$\cdots \frac{\cdots}{\cdots + \frac{b_2 b_3}{{\omega_0}^4} s^4 + \frac{a_1}{\omega_0} s + \frac{a_1 a_3}{{\omega_0}^2} s^2 + \frac{a_1 b_3}{{\omega_0}^3} s^3 + \frac{a_1 a_2}{{\omega_0}^2} s^2 + \frac{a_1 a_2 a_3}{{\omega_0}^3} s^3 + \cdots} \cdots$$

$$\cdots \frac{\cdots}{\cdots + \frac{a_1 a_2 b_3}{{\omega_0}^4} s^4 + \frac{a_1 b_2}{{\omega_0}^3} s^3 + \frac{a_1 a_3 b_2}{{\omega_0}^4} s^4 + \frac{a_1 b_2 b_3}{{\omega_0}^5} s^5};$$

$$G_{\mathrm{PT}}(s) = \frac{1}{\frac{a_1 b_2 b_3}{{\omega_0}^5} s^5 + \frac{(b_2 b_3 + a_1 a_2 b_3 + a_1 a_3 b_2)}{{\omega_0}^4} s^4 + \cdots} \cdots \tag{29}$$

$$\cdots \frac{\cdots}{\cdots + \frac{(a_2 b_3 + a_3 b_2 + a_1 b_3 + a_1 a_2 a_3 + a_1 b_2)}{{\omega_0}^3} s^3 + \cdots} \cdots$$

$$\cdots \frac{\cdots}{\cdots + \frac{(b_3 + a_2 a_3 + b_2 + a_1 a_3 + a_1 a_2)}{{\omega_0}^2} s^2 + \frac{(a_1 + a_2 + a_3)}{\omega_0} s + 1}.$$

By comparing the coefficients with Eq. (27a) we get

$$k_1 = R_\mathrm{D} C_\mathrm{D} = \frac{a_1 + a_2 + a_3}{\omega_0}; \tag{30a}$$

$$k_2 = L_1(C_1 + C_2 + C_\mathrm{D}) + L_2(C_2 + C_\mathrm{D}) = \frac{b_3 + a_2 a_3 + b_2 + a_1 a_3 + a_1 a_2}{{\omega_0}^2}; \tag{30b}$$

$$k_3 = R_\mathrm{D} C_\mathrm{D}(L_1 C_1 + L_2 C_2 + L_1 C_2) = \frac{a_2 b_3 + a_3 b_2 + a_1 b_3 + a_1 a_2 a_3 + a_1 b_2}{{\omega_0}^3}; \tag{30c}$$

$$k_4 = L_1 L_2 C_1 (C_2 + C_\mathrm{D}) = \frac{b_2 b_3 + a_1 a_2 b_3 + a_1 a_3 b_2}{{\omega_0}^4}; \tag{30d}$$

$$k_5 = L_1 L_2 C_1 C_2 C_\mathrm{D} R_\mathrm{D} = \frac{a_1 b_2 b_3}{{\omega_0}^5}. \tag{30e}$$

For a given optimization method, the five independent Eqs. (30a)–(30e) contain seven unknowns (L_1, L_2, C_1, C_2, R_D, C_D, and ω_0). Therefore we have the choice to select two of them and the remaining five depend on that selection; here we preselect ω_0 and L_1. Refer to Section 2 for the evaluation of L_1.

Selection of the cut-off angular frequency ω_0: For a given angular frequency ω_B well in the blocking area of the filter ($\omega_\mathrm{B} >> \omega_0$) we can define the desired attenuation G_B. In the blocking area the highest-order terms of both the numerator and the denominator in Eq. (26) dominate, therefore it can be simplified to

$$G_\mathrm{B} = \frac{R_\mathrm{D} C_\mathrm{D} s}{L_1 L_2 C_1 C_2 R_\mathrm{D} C_\mathrm{D} s^5} = \frac{\frac{a_1 + a_2 + a_3}{\omega_0} s}{\frac{a_1 b_2 b_3}{{\omega_0}^5} s^5} = \frac{a_1 + a_2 + a_3}{a_1 b_2 b_3} \cdot \frac{{\omega_0}^4}{s^4} = \frac{a_1 + a_2 + a_3}{a_1 b_2 b_3} \cdot \frac{{\omega_0}^4}{{\omega_B}^4};$$

$$\omega_0 = \omega_B \cdot \sqrt[4]{\frac{G_\mathrm{B} \cdot a_1 b_2 b_3}{a_1 + a_2 + a_3}}. \tag{31}$$

The cut-off angular frequency ω_0 of the filter depends only on the required attenuation and on the selected optimization method. The equation system (30a)–(30e) has to be solved for L_2, C_1, C_2, R_D, and C_D.

By solving Eq. (30a) for C_D and substituting C_D in Eqs. (30b)–(30e) we reduce the system to four equations:

$$k_2 = L_1\left(C_1 + C_2 + \frac{k_1}{R_\mathrm{D}}\right) + L_2\left(C_2 + \frac{k_1}{R_\mathrm{D}}\right); \tag{32a}$$

$$k_3 = k_1(L_1 C_1 + L_2 C_2 + L_1 C_2); \tag{32b}$$

$$k_4 = L_1 L_2 C_1\left(C_2 + \frac{k_1}{R_\mathrm{D}}\right); \tag{32c}$$

$$k_5 = k_1 L_1 L_2 C_1 C_2. \tag{32d}$$

By dividing Eq. (32c) by Eq. (32d) we get:

$$\frac{k_4}{k_5} = \frac{L_1 L_2 C_1 \left(C_2 + \frac{k_1}{R_\mathrm{D}}\right)}{k_1 L_1 L_2 C_1 C_2} = \frac{\left(C_2 + \frac{k_1}{R_\mathrm{D}}\right)}{k_1 C_2};$$

$$k_1 k_4 C_2 - k_5 C_2 = \frac{k_1 k_5}{R_\mathrm{D}};$$

$$R_\mathrm{D} = \frac{k_1 k_5}{C_2 (k_1 k_4 - k_5)}. \tag{33}$$

By substituting Eq. (33) in Eq. (32a) we reduce the system further to three equations:

$$k_2 = L_1 \left(C_1 + C_2 + \frac{k_1 C_2 (k_1 k_4 - k_5)}{k_1 k_5}\right) + L_2 \left(C_2 + \frac{k_1 C_2 (k_1 k_4 - k_5)}{k_1 k_5}\right)$$

$$= L_1 \left(C_1 + C_2 (1 + \frac{k_1 k_4}{k_5} - 1)\right) + L_2 \left(C_2 (1 + \frac{k_1 k_4}{k_5} - 1)\right) = L_1 C_1 + \frac{k_1 k_4}{k_5} L_1 C_2 + \frac{k_1 k_4}{k_5} L_2 C_2$$

$$= L_1 C_1 + C_2 (L_1 + L_2) \frac{k_1 k_4}{k_5}; \tag{34a}$$

$$k_3 = k_1 (L_1 C_1 + L_2 C_2 + L_1 C_2); \tag{34b}$$

$$k_5 = k_1 L_1 L_2 C_1 C_2. \tag{34c}$$

By solving Eq. (34c) for C_1 and substituting C_1 in Eqs. (34a) and (34b) we reduce the system further to two equations:

$$k_2 = \frac{k_5}{k_1 L_2 C_2} + C_2 (L_1 + L_2) \frac{k_1 k_4}{k_5}; \tag{35a}$$

$$\frac{k_3}{k_1} = \frac{k_5}{k_1 L_2 C_2} + C_2 (L_1 + L_2). \tag{35b}$$

By subtracting Eq. (35b) from Eq. (35a) we get

$$k_2 - \frac{k_3}{k_1} = C_2 (L_1 + L_2) \left(\frac{k_1 k_4}{k_5} - 1\right) = \frac{k_1 k_2 - k_3}{k_1} = \frac{k_1 k_4 - k_5}{k_5} C_2 (L_1 + L_2);$$

$$C_2 = \frac{k_5 (k_1 k_2 - k_3)}{k_1 (k_1 k_4 - k_5)(L_1 + L_2)}. \tag{36}$$

By substituting Eq. (36) in Eq. (35a) we get

$$k_2 = \frac{k_5 k_1 (k_1 k_4 - k_5)(L_1 + L_2)}{k_1 k_5 (k_1 k_2 - k_3) L_2} + \frac{k_1 k_4 k_5 (k_1 k_2 - k_3)(L_1 + L_2)}{k_1 k_5 (k_1 k_4 - k_5)(L_1 + L_2)}$$

$$= \frac{(k_1 k_4 - k_5)(L_1 + L_2)}{(k_1 k_2 - k_3) L_2} + \frac{k_4 (k_1 k_2 - k_3)}{(k_1 k_4 - k_5)};$$

$$\frac{(k_1k_4-k_5)(L_1+L_2)}{(k_1k_2-k_3)L_2}=k_2-\frac{k_4(k_1k_2-k_3)}{k_1k_4-k_5}=\frac{k_1k_2k_4-k_2k_5-k_1k_2k_4+k_3k_4}{k_1k_4-k_5}$$
$$=\frac{k_3k_4-k_2k_5}{k_1k_4-k_5};$$

$$\frac{L_1+L_2}{L_2}=\frac{L_1}{L_2}+1=\frac{(k_3k_4-k_2k_5)(k_1k_2-k_3)}{(k_1k_4-k_5)^2};$$

$$L_1=L_2\left[\frac{(k_3k_4-k_2k_5)(k_1k_2-k_3)}{(k_1k_4-k_5)^2}-1\right];$$

$$L_2=\frac{L_1}{\frac{(k_3k_4-k_2k_5)(k_1k_2-k_3)}{(k_1k_4-k_5)^2}-1}. \tag{37}$$

Example 4: Design a fourth-order filter for a buck converter with a d.c.-link voltage of 120 V, a switching frequency of 20 kHz, and a maximum output current of 500 A; refer to Fig. 13. The ripple current in L_1 should not exceed 50 A peak to peak. The filter should have an attenuation of 0.004 at the switching frequency. Design the filter for all three optimization methods and compare the results. In order to enable a comparison between different filter structures (refer to Section 4), the same parameters are given as in Examples 2 and 3.

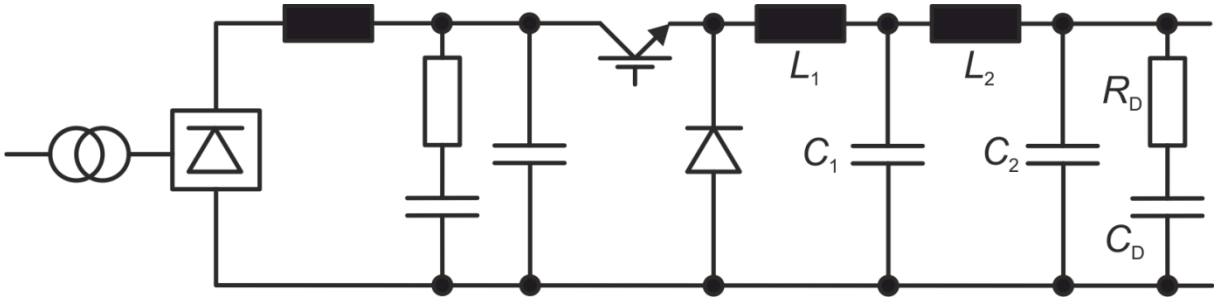


Fig. 13: Output filter for a buck converter

Select L_1 in order to meet the ripple requirement by using Eq. (8a):

$$L_1=\frac{V_{\mathrm{dc}}\cdot 0.25}{f_{\mathrm{s}}\cdot\Delta I_{L1}}=\frac{120\ \mathrm{V}\cdot 0.25}{20\ \mathrm{kHz}\cdot 50\ \mathrm{A}}=30\ \mu\mathrm{H}.$$

Select ω_0 in order to meet the attenuation requirement by using Eq. (31)

$$\omega_0=\omega_{\mathrm{B}}\cdot\sqrt[4]{\frac{G_{\mathrm{B}}\cdot a_1b_2b_3}{a_1+a_2+a_3}}=2\cdot\pi\cdot 20\ \mathrm{kHz}\cdot\sqrt[4]{\frac{0.004\cdot a_1b_2b_3}{a_1+a_2+a_3}}.$$

Calculate the remaining filter components by using Eqs. (37), (36), (34c), (33) and (30a) in that order. The results are listed in Table 8. Depending on the selected optimization method, L_2 is approximately either double, equal to, or half the size of L_1. This leads to a simplified design as L_1 and L_2 can be realized with either two or three identical chokes.

Table 8: Results for Example 4

Parameter	Butterworth	Bessel	Critical damping
ω_0	23,600 s^{-1}	13,800 s^{-1}	8200 s^{-1}
f_0	3.75 kHz	2.20 kHz	1.30 kHz
L_1	30 μH	30 μH	30 μH
L_2	57 μH	31 μH	17 μH
C_1	74 μF	90 μF	124 μF
C_2	7.9 μF	12 μF	16 μF
C_D	75 μF	168 μF	382 μF
R_D	1.83 Ω	1.05 Ω	0.62 Ω

Figure 14 shows the Bode plots of the three filter designs according to Example 4. They are exactly the same as for Example 3. The attenuation at 20 kHz is –48 dB, which corresponds to a factor of 0.004 as required. Compared to the second-order filter (see Fig. 8) the resonance amplitudes are slightly higher and the same trade-off between small capacitor values and low resonance amplitudes applies.

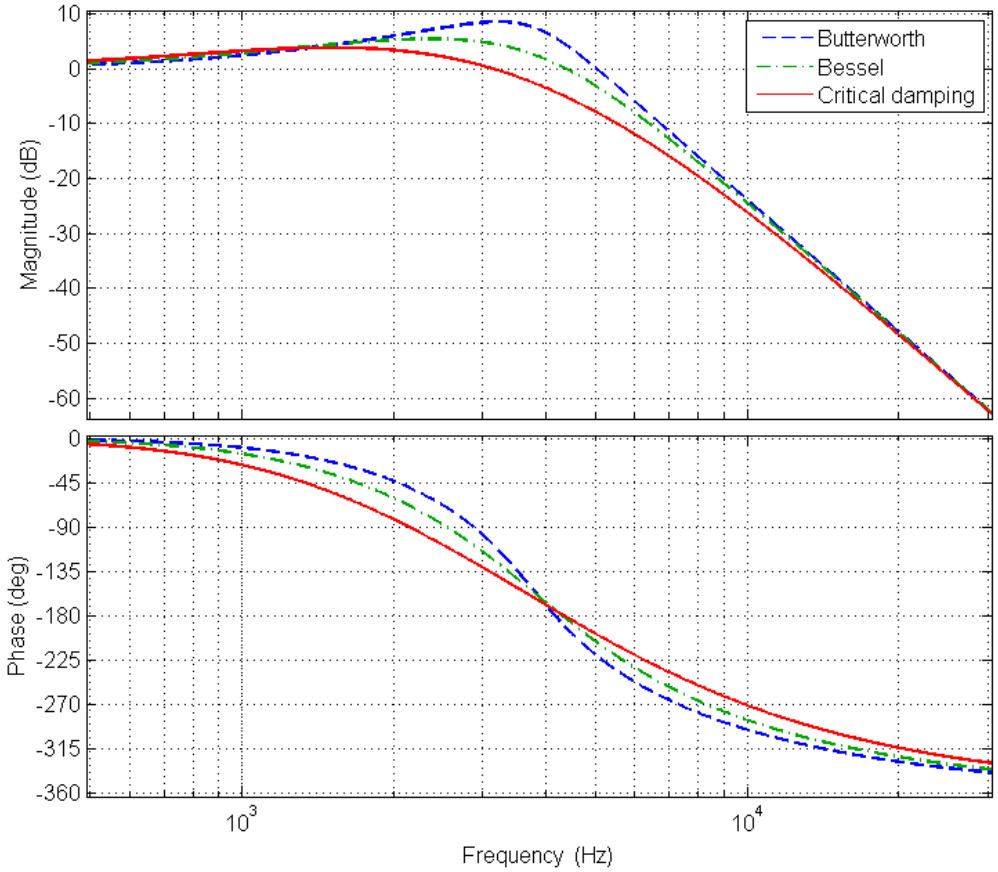


Fig. 14: Bode plots for the filter designs according to Example 4

4 Comparison of different filter designs

In Examples 2–4 we have designed three filters with different structures but with the same performance (attenuation factor of 0.004 at 20 kHz). This allows a direct comparison of the three filter structures. Table 9 summarizes the results for the Bessel optimization.

Table 9: Results for Bessel optimization Examples 2–4

Parameter	**Example 2**	**Example 2** $L_1 = 100\ \mu H$	**Example 2** $L_1 = 100\ \mu H$ $G_B = 0.01$	**Example 3**	**Example 4**
L_1	30 μH	100 μH	100 μH	30 μH	30 μH
L_2				31 μH	31 μH
C_1	528 μF	158 μF	63 μF	24 μF	90 μF
C_2				44 μF	12 μF
C_D	2640 μF	790 μF	320 μF	342 μF	168 μF
$C_1 + C_2 + C_D$	3168 μF	948 μF	383 μF	410 μF	270 μF
R_D	0.18 Ω	0.62 Ω	0.98 Ω	0.51 Ω	1.05 Ω
f_0	570 Hz	570 Hz	910 Hz	2200 Hz	2200 Hz
Losses in C_D	0.26 W	0.076 W	0.30 W	37 W	0.042 W

In Example 2 (second-order filter) the total installed capacitance ($C_1 + C_2 + C_D$) becomes huge and the resulting cut-off frequency is low compared to Examples 3 and 4 (see Table 9). In order to achieve comparable capacitances for Example 2, two alternative filters have been calculated. The first alternative has a larger inductance L_1, which reduces the total capacitance remarkably. The transfer function stays the same (same Bode plot, see Fig. 15). The selection of L_1 allows an optimization of the components in terms of space required, weight, costs, etc., but in general it is much cheaper to store energy in capacitors than in inductors. The second alternative also has a larger inductance L_1 and additionally the attenuation factor was relaxed to 0.01 (instead of 0.004). This modification reduces the total capacitance further and the cut-off frequency becomes higher. However, the drawback is a higher output voltage ripple.

Examples 3 and 4 are both fourth-order filters and they have the same transfer function (see the Bode plot in Fig. 15). The only difference is the placement of the damping circuit. Example 4 (damping circuit in second *LC* stage) is the preferred solution for two reasons: first, the total capacitance is remarkably smaller, which is a space and cost factor. Second, the power dissipation in R_D is three orders of magnitude smaller! Although losses of 37 W might still be acceptable, it requires a larger element, which needs to be cooled sufficiently.

At first glance, the fourth-order filter is more complex, and therefore it is often considered as non-practical. However, the comparison in Table 9 reveals several advantages. High precision power converters need high bandwidth in order to react rapidly to errors. The closed-loop bandwidth is limited by the output filter cut-off frequency (see the Bode plot in Fig. 15). Therefore, higher-order filters, as presented in Example 4, are the preferred choice. If we compare Example 2 with $L_1 = 100\ \mu H$ with Example 4, there is in total 1.6 times more inductance and 3.5 times more capacitance needed to obtain the same attenuation.

Figure 15 shows the comparison of the five examples listed in Table 9. Note, that for Example 2 the two alternatives with $L_1 = 30\ \mu H$ and $L_1 = 100\ \mu H$ have the same transfer function. Also the Bode plots for Examples 3 and 4 are identical.

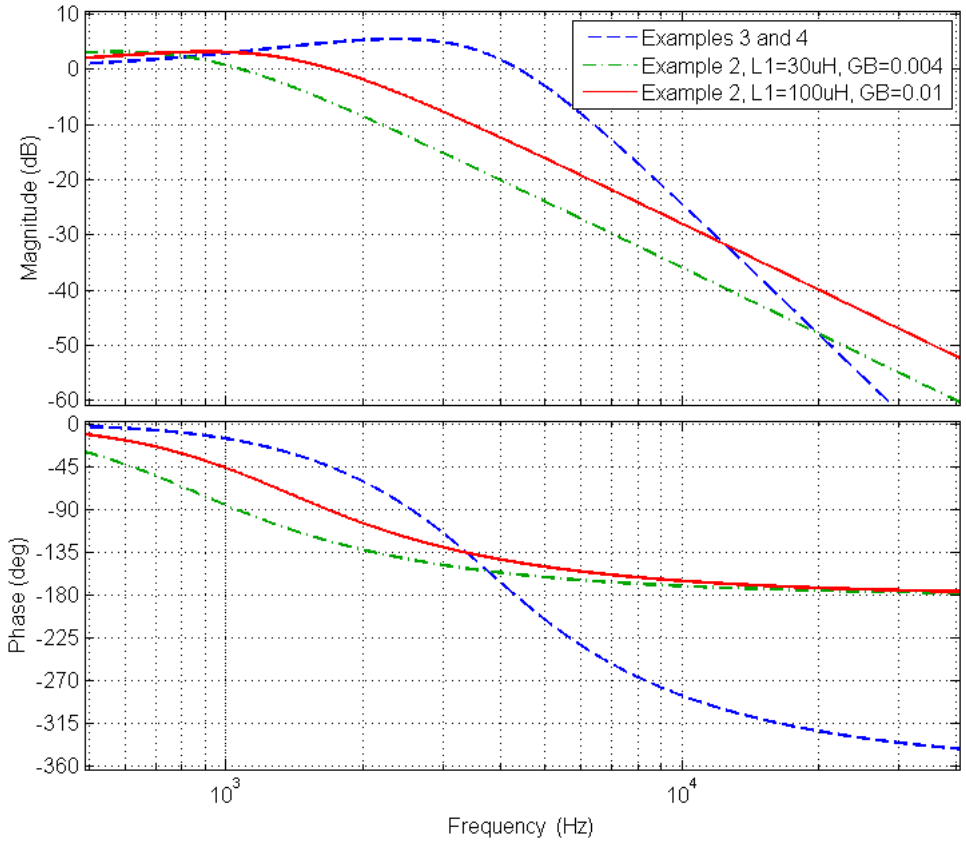


Fig. 15: Bode plots for the filter designs according to Examples 2–4 with Bessel optimization

5 Practical aspects

5.1 Load impedance

The presented calculations do not consider the load impedance. In many cases, where the load impedance is high enough and inductive (magnets), this approach is acceptable. However, if the load impedance is low and/or complex, it has an impact on the filter behaviour. In that case, the load impedance has to be considered in the calculation, or at least the complete circuit has to be analysed.

5.2 Parasitic circuit elements

The presented calculations were made considering ideal elements. In practice, this is not the case. As an example, the parasitic resistances and inductances of C_1 and C_2 in Example 4 should be estimated by considering two alternatives: a 'good' and a 'bad' design. There are two main effects to be considered: the cable that connects C_1 and C_2 to the circuit, and the ESR (equivalent series resistance) of these two capacitors. In the damping circuit these effects do not have a significant impact.

For the 'bad' design we use a 50 cm long wire with a cross-section of 16 mm^2 to connect C_1 and a 50 cm long wire with a cross-section of 2.5 mm^2 to connect C_2. Due to the skin effect, the effective cross-sections of the wires are reduced to 6.3 mm^2 for C_1 and 2.0 mm^2 for C_2. These wires add parasitic resistances and inductances of 1.40 mΩ and 0.53 μH to C_1, and 4.2 mΩ and 0.63 μH to C_2.

It is strongly recommended, that C_1 and C_2 are connected as directly as possible (using shorter connections) to the main bus bars. If we consider connections shorter by a factor of 5 (10 cm) for the 'good' design, the parasitic elements are reduced to 0.27 mΩ and 0.075 μH for C_1, and 0.83 mΩ and 0.093 μH for C_2.

The ESR values are given in the data sheets. The situation can be improved by selecting good capacitors with a small ESR and by paralleling many small capacitors rather than only a few large ones. The ESR values from a data sheet are given in Table 10 for capacitors suitable for the realization of the output filter according to Example 4 with critical damping (see Section 3.2).

Table 10: ESR of metalized film capacitors

Capacitor	ESR
1.5 μF / 250 V	6.8 mΩ
10 μF / 250 V	1.8 mΩ
20 μF / 250 V	1.9 mΩ
60 μF / 250 V	1.9 mΩ

According to Example 4 with optimization method critical damping, C_1 should be 124 μF and C_2 should be 16 μF. The filter should be realized with capacitors from Table 10.

For the 'bad' design, we use two 60 μF capacitors with a resulting ESR of 0.95 mΩ for C_1 and one 20 μF capacitor with an ESR of 1.9 mΩ for C_2. Refer also to Table 11.

For the 'good' design, we use 12 10 μF capacitors with a resulting ESR of 0.15 mΩ for C_1 and 11 1.5 μF capacitors with a resulting ESR of 0.62 mΩ for C_2. Refer also to Table 11.

Figure 16 shows the fourth-order filter as outlined in Section 3.2 expanded with the parasitic elements.

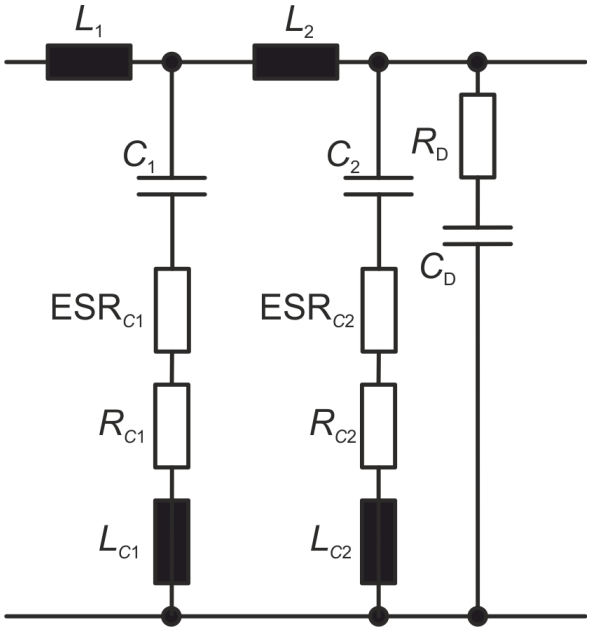


Fig. 16: Fourth-order filter with parasitic elements

The corresponding element values are listed in Table 11 for three different designs called 'ideal', 'good', and 'bad'. The main filter elements are rounded to practically realizable values.

Table 11: Filter components including parasitic elements

Parameter	Design 'ideal'	Design 'bad'	Design 'good'
L_1	30 μH	30 μH	30 μH
L_2	17 μH	15 μH	15 μH
C_1	124 μF	120 μF	120 μF
ESR_{C1}	0 mΩ	0.95 mΩ	0.15 mΩ
R_{C1}	0 mΩ	1.40 mΩ	0.27 mΩ
L_{C1}	0 μH	0.53 μH	0.075 μH
C_2	16 μF	20 μF	16.5 μF
ESR_{C2}	0 mΩ	1.90 mΩ	0.62 mΩ
R_{C2}	0 mΩ	4.20 mΩ	0.83 mΩ
L_{C2}	0 μH	0.63 μH	0.093 μH
C_D	382 μF	360 μF	360 μF
R_D	0.62 Ω	0.60 Ω	0.60 Ω

Figure 17 shows the Bode plots for the three designs listed in Table 11. For the 'bad' design, there is a steep phase shift right at the switching frequency, and the higher harmonics of the switching frequency are suppressed much less than in the ideal design. For the 'good' design in principle the same occurs, but at higher frequencies and at a much lower amplitude level.

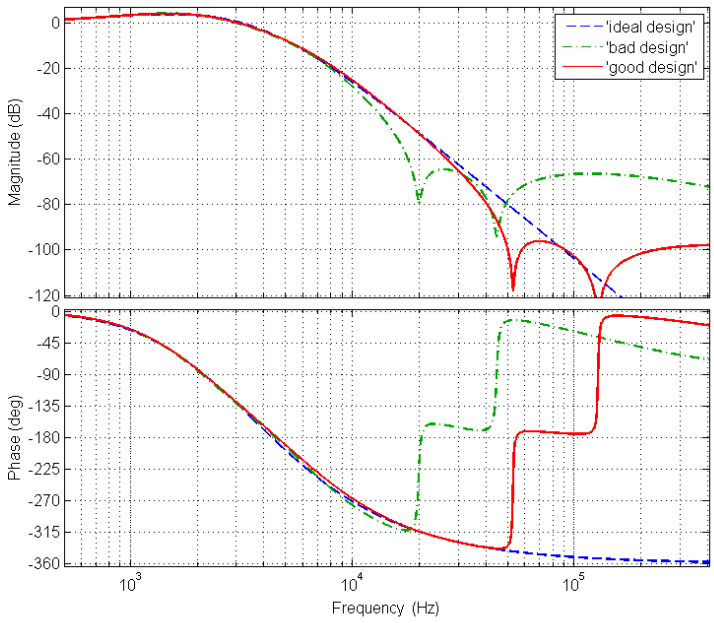


Fig. 17: Bode plots for the filter designs with parasitic elements

References

[1] U. Tietze and Ch. Schenk, *Halbleiter Schaltungstechnik*, 12th ed. (Springer, Berlin, Heidelberg, New York, 2002), p. 815.

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Risk and Machine Protection for Stored Magnetic and Beam Energies

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Abstract
Risk is a fundamental consideration when designing electronic systems. For most systems a view of risk can assist in setting design objectives, whereas both a qualitative and quantitative understanding of risk is mandatory when considering protection systems. This paper gives an overview of the risks due to stored magnetic and beam energies in high-energy physics, and shows how a risk-based approach can be used to design new systems mitigating these risks, using a lifecycle inspired by IEC 61508. Designing new systems in high-energy physics can be challenging as new and novel techniques are difficult to quantify and predict. This paper shows how the same lifecycle approach can be used in reverse to analyse existing systems, following their operation and first experiences.

Keywords
Risk; machine protection; safety; accelerators; IEC 61508.

1 Introduction

Modern high-energy physics (HEP) machines run with large stored energies. These pose a risk: if energies are released in an uncontrolled manner, there is the potential for damage to accelerator components and an impact on operational availability, as machines have to be stopped and repaired before operations can continue. Risks due to stored energies are studied, and ultimately mitigated by dedicated machine protection systems (MPS). Risk-based approaches should be part of every engineer's toolbox: this is particularly important in the development of systems related to protection. This paper outlines the fundamentals of machine protection, giving an overview of the approaches used in the powering and protection of HEP machines.

1.1 The Large Hadron Collider

The Large Hadron Collider (LHC) is the world's most powerful particle accelerator and one of the world's largest and most complicated machines, having been conceived and designed over the course of the last 30 years. This machine represents the cutting edge of accelerator technology. Figure 1 shows a simplified schematic of the LHC, where two counter-rotating beams (Beam-1 and Beam-2) are injected and brought into collision at dedicated experiments located at four of the eight insertion regions (IR) of the machine.

Beams are transferred to the LHC from the Super Proton Synchrotron (SPS), which is the final machine in a complex of accelerators that prepare LHC beams. It takes 12 injections of beam from the SPS to completely fill each of the LHC's two rings. Once filled, the LHC accelerates the beams by means of a radio-frequency (RF) system. The dipole magnetic field is increased in step with the increase in beam energy, ensuring that each circulating beam maintains a consistent beam orbit. Once physics energy is reached, the beams are squeezed and brought into collision. Experiments then gather data, before the machine is emptied, and the process restarted. This process is referred to as the LHC *machine cycle* and is shown in more detail in Fig. 2.

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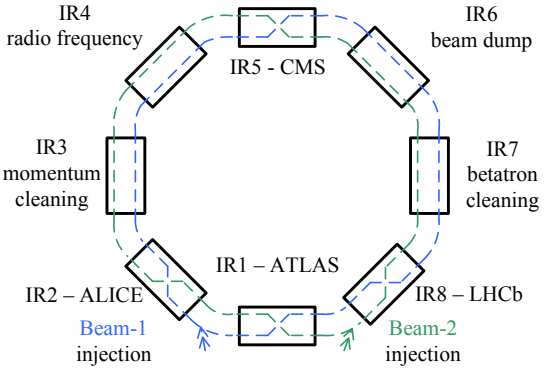

Fig. 1: LHC schematic and insertion regions

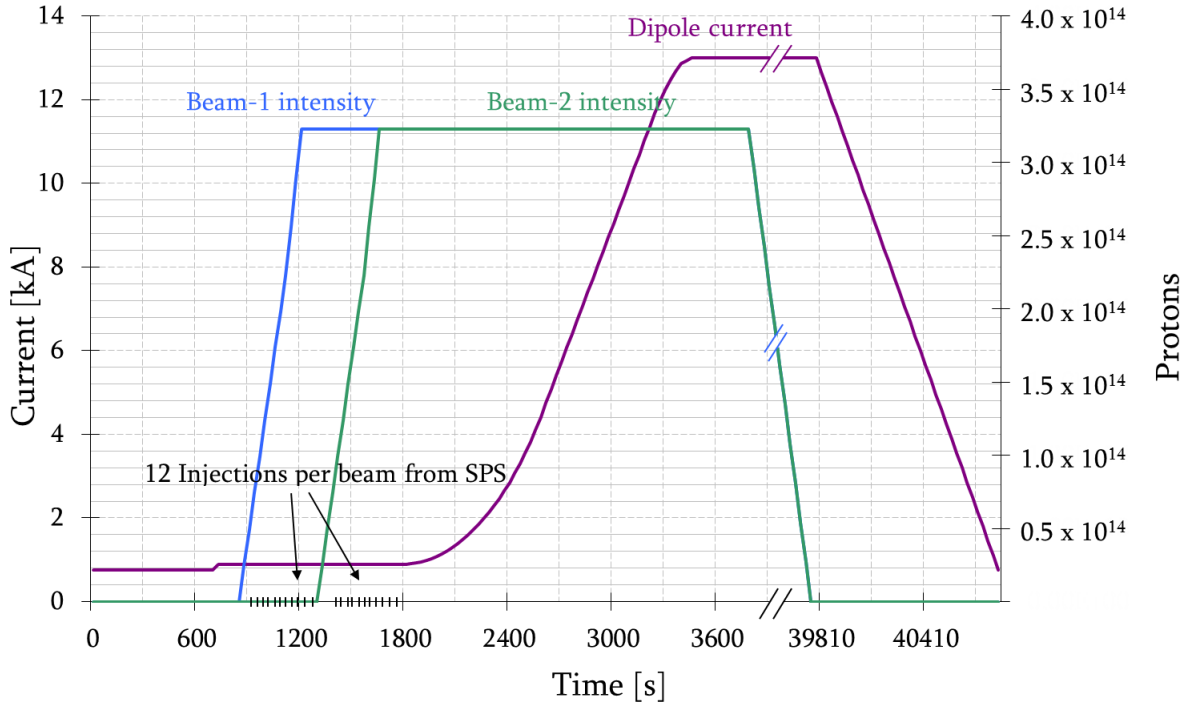

Fig. 2: LHC cycle with main dipole current and approximated beam intensities

2 Risks due to stored energies

The two principal sources of energy in large physics machines are the powering circuits, in the form of stored magnetic energy, and the beam.

The LHC is designed to provide a centre-of-mass collision energy of 14 TeV (10^{12} eV). This gives around 360 MJ stored beam energy per beam, over 100 times larger than any other machine. To circulate the 7 TeV beams in the 27 km circumference of the machine, magnetic fields of 8.3 T are needed. These fields require superconducting dipole magnets operating at 13 kA, at only around 2°C above absolute zero (about −271°C). At nominal current, around 10 GJ is stored as magnetic energy in the whole magnet powering system. Figure 3 compares the stored magnet and beam energies in the LHC with those of other HEP machines.

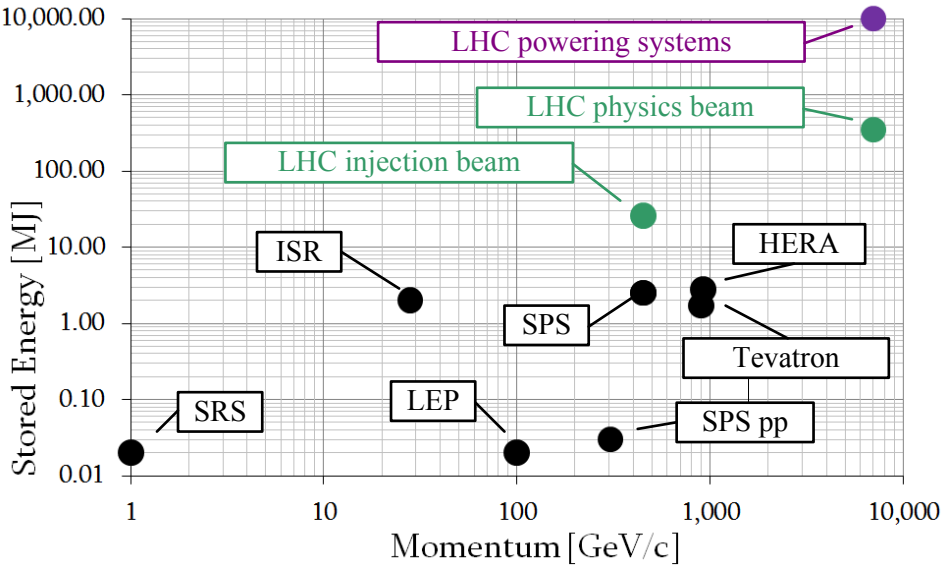

Fig. 3: Comparative energy levels in the LHC and other HEP machines [1]

With these parameters, there is a high chance of particle impacts causing a magnet to quench, where superconductor becomes resistive, and action must be taken to prevent damage to the magnets. Losing excessive beam energy in a part of the machine can cause other kinds of damage, such as rupturing the machine vacuum [2]. Table 1 shows the percentages of prompt beam energy losses considered as *quench* and *damage* limits of the LHC.

Table 1: Quench and damage levels due to prompt beam energy loss [3]

Energy [GeV]	Beam energy loss [%]	Consequences
450	0.000 8	Quench
450	0.5	Damage
7000	0.000 0005	Quench
7000	0.005	Damage

In the best case, damage events would result in repairs and downtime; in the worst case there are potential failures that could result in the closure of the laboratory for significant periods of time. One incident regarding an uncontrolled loss of energy from the magnetic circuits has already occurred, and it resulted in CERN's accelerators being closed for over a year to make repairs and to design mitigations. Table 1 represents the key design challenge of machine protection.

At the same time, machines such as the LHC must operate. The performance should be taken as close to operational limits as permitted, whilst at the same time being protected. To accomplish these goals, machine protection systems (MPS) are designed and implemented.

3 Machine protection systems (MPS)

At CERN, an MPS has been developed to bring the risks of running the LHC down to an acceptable level. The development process has followed a deep-thinking academic approach as machine protection is not a legal requirement of the LHC project and the MPS is not a safety system, although the two are closely related. In the LHC, the safety system is the LHC Access System, ensuring the collective protection of the personnel against electrical and radiological hazards arising from the LHC accelerator [4].

The MPS is split into two sections, to address the two different classes of risk:

- beam-related machine protection – protecting the LHC against damage due to the accidental release of beam energy, caused by losing beam particles;
- powering machine protection – protecting the LHC against damage due to the accidental release of energy stored in the magnet powering circuits.

Figure 4 shows the relationship between these different systems. In order to correctly protect people and the environment from the risk of operation, the safety system does not require the correct function of the MPS. However, without the MPS, an activation of the safety system would put the LHC machine at risk, as the safety actuators are designed to sacrifice the machine in order to protect the personnel.

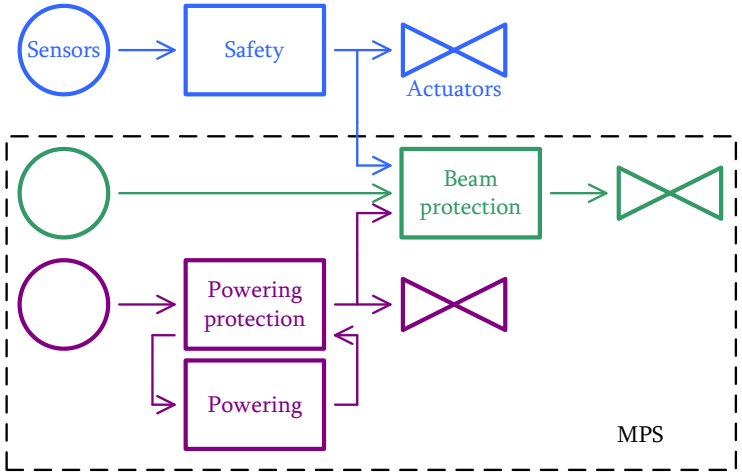

Fig. 4: Safety and machine protection system relations

MPS are conceived on the basis of two principles:

- machine safety – the machine must be protected from damage, and should be prevented from unduly wearing out its components;
- machine availability – the machine must provide beams for physics applications.

The *machine safety to availability balance* is a crucial concern in MPS development. A machine that is entirely safe may have low availability, as increasing safety can mean reducing tolerance to non-nominal situations. On the other hand, if the tolerance to non-nominal situations is increased, the safety is generally reduced, whilst the availability is increased.

3.1 Non-nominal energy release

Damage to the machine related to energy is triggered by non-nominal energy release: energy releases that cannot be corrected for by using feedback systems or passive protection. Therefore the MPS is based on a combination of two phases.

- *Prevent* non-nominal energy release – intervene in a failure chain that may lead to a non-nominal release. It is known that following the failure of certain components, without intervention, energy release will eventually occur.
- *Protect* equipment from the consequences of non-nominal energy release – intervene if non-nominal energy release occurs, by mitigating the consequences of the release.

3.2 Beam energy protections

In the case of non-nominal beam energy loss, the protection phase intervention is performed in three steps, by three types of subsystem, as shown in Fig. 5.

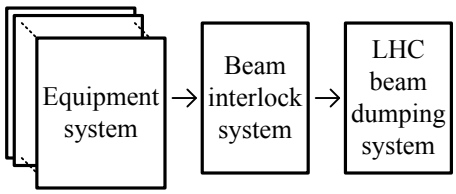

Fig. 5: Principal components of the beam-related MPS

- *Equipment systems* are designed to detect non-nominal beam conditions and send beam abort requests to the *Beam Interlock System*;
- The *beam interlock system* transmits the beam abort request to the *LHC beam dumping system*;
- The *LHC beam dumping system* carries out the controlled abort of LHC beam operation, and the dissipation of stored beam energy.

Some failure modes mean that a failure can lead to a dangerous situation in just a few turns of the machine [5]. To protect the LHC from these fast failure modes, the beam-related protection intervention must take place within *several hundred microseconds.*

3.3 Powering protection

At design values, the stored energy of all LHC magnet circuits is almost 10 GJ. Powering systems are divided into eight principal subsectors to bring the energy stored in each powering circuit to levels similar to that of other machines [6]. A combination of three key systems performs the intervention in the protection phase intervention as shown in Fig. 6.

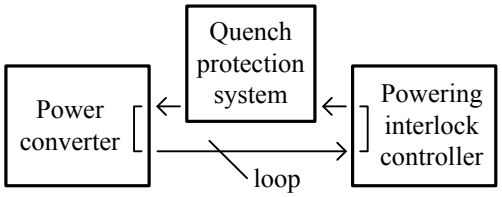

Fig. 6: Principal components of the magnet powering-related MPS

- A *quench protection system* detects non-nominal magnet conditions, opens energy extraction switches, and transmits a powering abort request to the power converters.
- The *power converter* stops supplying power to affected circuits.
- In addition, a *powering interlock controller* links related powering circuits, and other subsystems having an influence on LHC magnet powering.

For magnet powering system protection, an intervention must take place within *several milliseconds*.

3.4 Protection, safety and control interactions

The safety system is the access system. If intrusion of personnel into the machine environment is detected during operation the access system automatically moves beam stoppers into the LHC beam lines [4]. If circulating LHC beam were to hit these beam stoppers, there would be significant beam losses and the LHC would be damaged. Therefore the access system is connected to both the LHC

beam dumping system, and the beam interlock system. If the access system is triggered, the beam-related MPS protects the LHC from the dangers posed by the beam stoppers.

Three of CERN's central systems are also shown in Fig. 7. The *control system* provides general supervision and an overview of all accelerator subsystems. The *timing system* synchronizes all of the accelerator subsystems. Also shown is the safe machine parameters (SMP) system, which is closely related to the MPS. SMP controls the MPS mode; it ensures a consistent configuration of the most critical MPS subsystems. For example, the beam energy losses quench and damage thresholds change as a function of beam energy, as shown in Table 1. SMP broadcasts machine energy throughout the complex, where it is received by, amongst others, the beam loss monitor (BLM) system, and is used to determine whether beam losses are putting the machine at risk.

Interconnections between safety, beam-related machine protection and power protection systems are shown in Fig. 7.

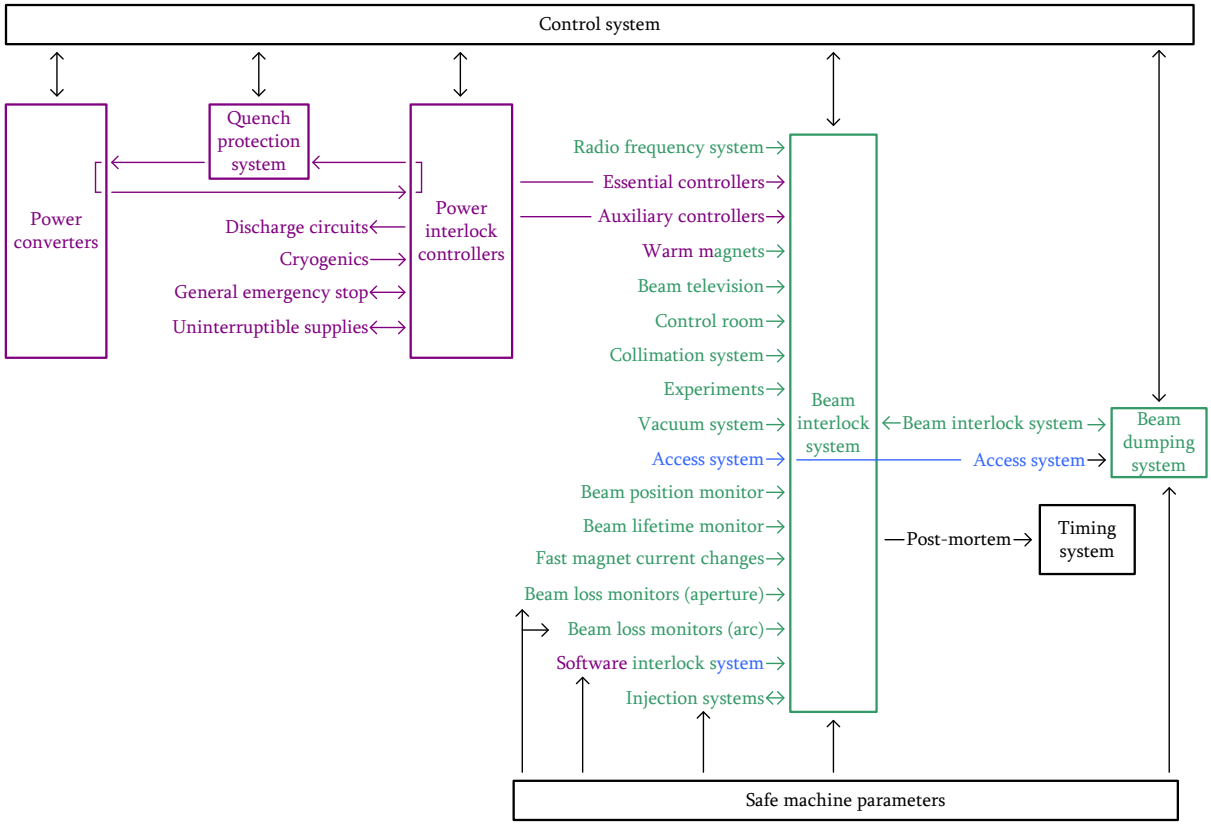

Fig. 7: Combined view of safety, protection, and control system interconnections

4 Protection system lifecycle: Designing new systems

In order to ensure that risks are mitigated a complete development process needs to be put into place. This ensures that correct decisions are taken at all points during system development. Considering this, the domain of machine protection shares several similarities with the domain of system safety, where MPS is the equivalent to a safety system.

Several industry standards exist, each ensuring that the process of developing safety systems can be proven, and that safety cases can be made. The central standard upon which most modern standards are based is IEC 61508 *Functional Safety of Electrical, Electronic & Programmable Electronic Safety Related Systems* [7], as shown in Fig. 8. IEC 61508 has been used as a basis from which to create the protection system lifecycle, which is outlined in this chapter.

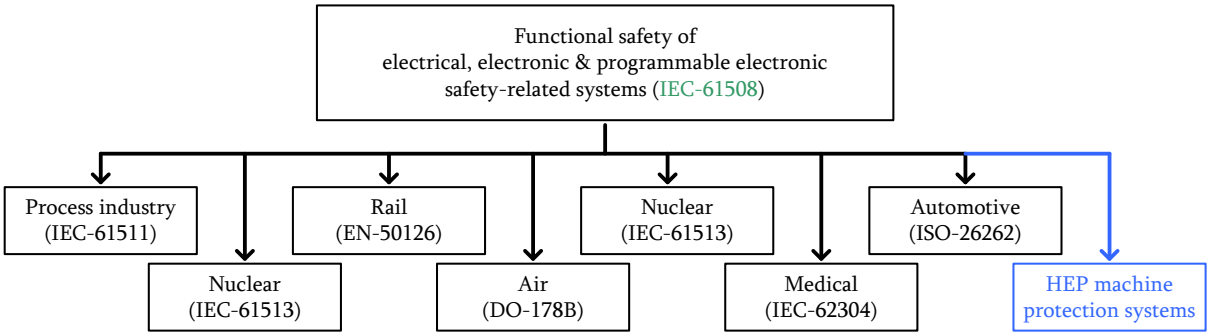

Fig. 8: IEC 61508 as a template for other safety standards [8]

With some appropriate conditioning and interpretation, many system-safety techniques, principles, tools, and guidelines can be applied to machine protection. The key steps in the protection system lifecycle are shown in Fig. 9. This is tailored to CERN's academic, non-legal environment, giving a less-rigorous framework than IEC 61508, while establishing best practices and the requirements for MPS development. This process has to be carried out within an organizational structure that is adapted to the role of machine protection. Appendix A outlines the structure currently in place at CERN.

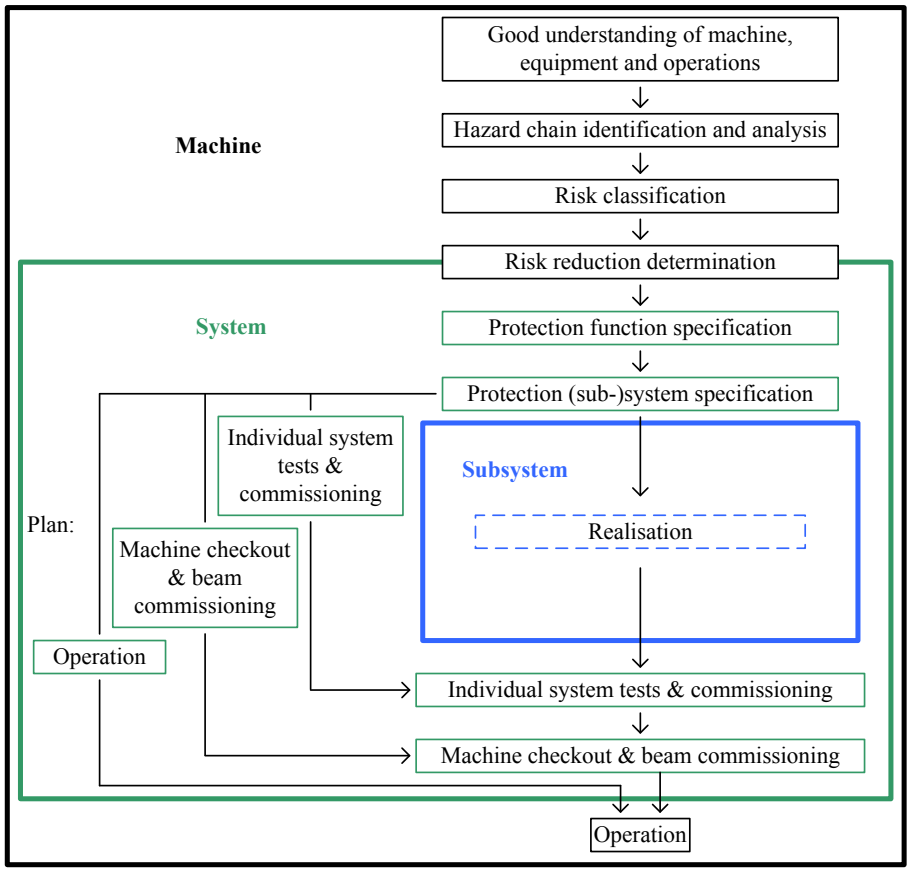

Fig. 9: Protection system lifecycle [7]

The first steps of the lifecycle are outlined below, with key information captured while following the process (Fig. 10). This begins with an understanding of risk, and ends with subsystem specifications. The principle is that for each risk identified, it can be proven that adequate mitigation is in place, and that the quality of mitigation is proportional to the risk being mitigated.

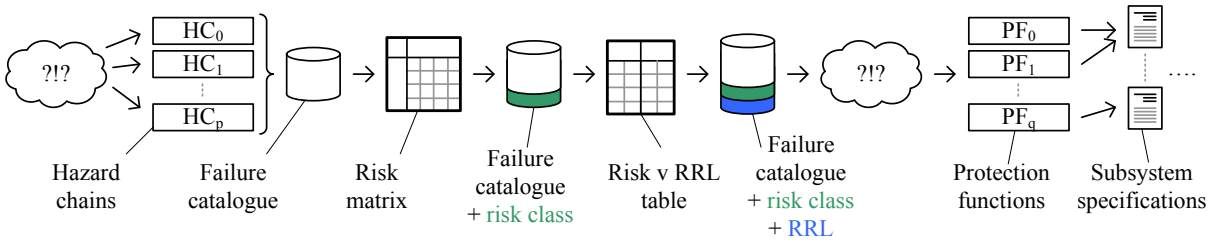

Fig. 10: Key data for each step of the protection system lifecycle [7]

4.1 Hazard identification and analysis

The first step is to identify *hazard chains*, which link failures to damage through a series of events and/or conditions. The granularity of these depends on the functions being studied, and the types of systems involved in the chain. This step results in the creation of a *failure catalogue*, containing all of the hazard chains that link failures, non-nominal energy deposition, and damage. The template for a failure chain is shown in Fig. 11, with an example explained on the right-hand side.

For each chain, two time constants should be recorded:

– ΔT_n, the time between the failure occurring at the start of the chain and the first non-nominal energy deposition taking place;

– ΔT_d, the time between the first non-nominal energy deposition and damage occurring.

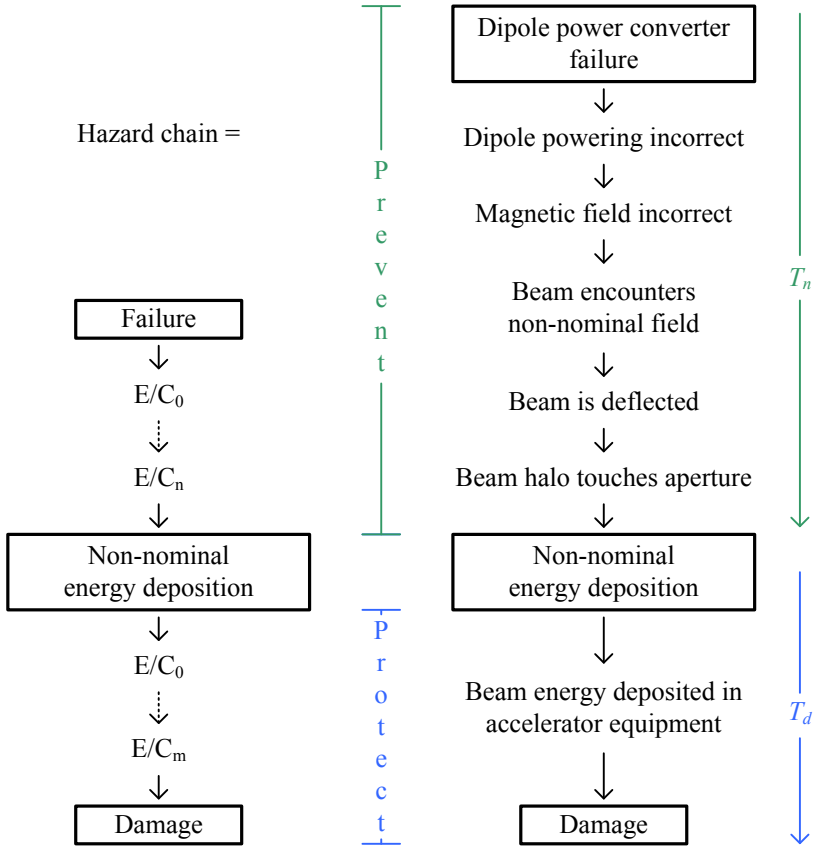

Fig. 11: Hazard chains, prevent, protect and time definitions [7]

Chains that have a small total time (T_n + T_d) between initial failure and damage can be more difficult to mitigate: less time is available to observe and take action; whereas chains that take a longer overall time to evolve may be more readily observed, and more easily mitigated.

The ratio between T_n and T_d is also important. Failures may take a longer time to lead to non-nominal loss, but then quickly lead to damage, or vice versa. In these cases mitigations must focus on different aspects of the chain, either prevention or protection.

In the example given above, several chains will be created, each for a different magnet failure and magnet families, each having different times between energy deposition and damage.

4.2 Risk classification and risk matrix

Risk is defined as a product of *probability* and *impact* [8]. The higher the product, the higher the risk. A *risk matrix* is a visual means of representing this. On one axis is indicated *probability*, and on the other axis is *impact*, with coordinate points representing the individual risks. A typical matrix, with a risk plotted, is shown in Fig. 12.

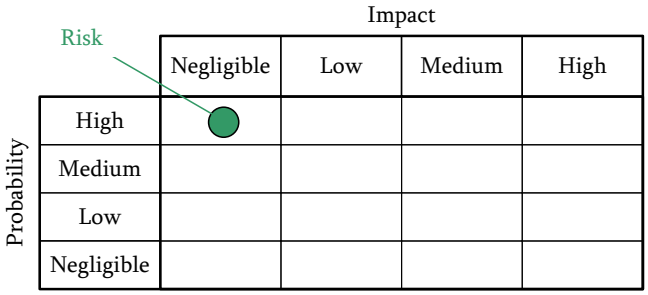

Fig. 12: Risk matrix

The matrix in Fig. 12 is qualitative; this should be converted into a quantitative matrix by appropriate experts. The definition of impact in the case of HEP could be a quantity such as *repair time*, *number of magnets damaged*, or *cost to repair*. In addition to the definition of the axes, the relative risk level for each area should also be qualified, by splitting the matrix into zones of equivalent risk. The typical approach is to choose four or five levels of risk. An example is shown in Fig. 13.

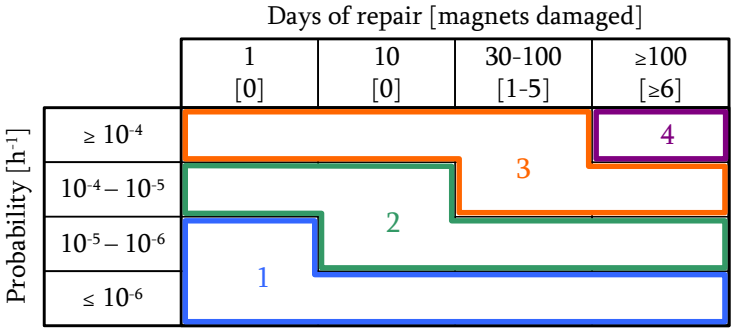

Fig. 13: Risk matrix with defined impact and risk levels

A risk level 1 is generally considered ‘as low as reasonably possible’ (ALARP). When a risk has this level, no mitigation is needed: the risk is accepted. The process of conversion from qualitative to quantitative, and the definition of boundaries, is subjective. There is no standard risk matrix: what is considered as ALARP for one organization or machine may be unacceptable to another.

Each of the hazard chains previously identified should have the associated risk plotted and classified using the risk matrix.

4.3 Risk reduction level (RRL)

For each of the risks plotted, a risk reduction level (RRL) is required to bring the risk to the ALARP level: higher risks require a larger RRL (Fig. 14). These RRL are added to the failure catalogue.

Original	Desired	RRL
4	1	3
3	1	2
2	1	1

Fig. 14: Risk reduction level definitions

4.4 Protection function specifications

For each hazard chain and associated risk, mitigations must be identified.

The first step is to determine whether there is a means to remove the hazard chain and risk entirely. It may be possible to change the machine architecture to render some chains impossible. If the risk cannot be removed, then *protection functions* should be conceived. These are to intervene in the chains, achieving the required risk reduction levels. A single chain may have several related functions; similarly, a single function may be used to intervene in several chains. If a single chain is broken in multiple places by multiple functions, then the required RRL is shared between the functions.

Functions that affect the HC before non-nominal energy losses occur are *prevention* mechanisms, whereas functions that intervene after non-nominal energy loss, but before damage, are *protection* mechanisms.

4.5 Protection integrity level (PIL) specifications

The protection functions are collected, and gathered into technical solutions, which are then assigned to systems. A single system may implement several functions, and a single function may be used to break several hazard chains.

In Fig. 15, hazard chain 1 (HC_1) *orbit feedback failure* has three protection functions that intervene to prevent damage. All three functions would have to fail for damage to result. The overall risk is 3, the overall RRL is therefore 2. PF_1, PF_2, and PF_3 must combine to reach this level. However, in hazard chain 2 (HC_2) *training quench*, only PF_3 interrupts the chain. In this case the risk is 4, giving a RRL of 3. Therefore PF_3 *extract energy from powering systems* has to meet the most strenuous requirement of RRL of 3. This is assignment of the so-called *protection integrity level* specification for the protection function.

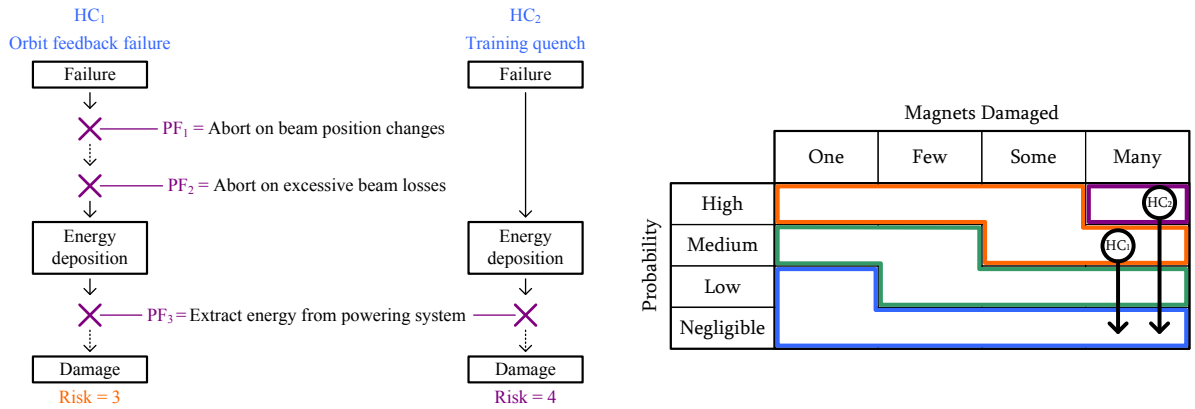

Fig. 15: An example of hazard chains and protection functions, with risks and risk matrix

4.6 Meeting specifications

The specified protection function has to be realised, and the specified PIL has to be demonstrated; in addition, the subsystem must meet the time constraints T_n and T_d as determined above. The development of high-dependability systems to meet protection requirements forms the central topic of several Ph.D. theses undertaken at CERN, see Appendix B for more information.

4.7 Operation and ongoing assurance

The steps following this are installation, testing, commissioning, and finally the handover of the system to operations.

A vital aspect to consider is that the ongoing operation of the machines should always be comparing the observed failure modes and failure rates against what was expected in the hazard chain and risk analysis. For this reason a failure catalogue should be maintained, and each activation of the MPS should be checked to ensure that the MPS is reacting correctly, and that no unforeseen hazard chains occur. If new chains are discovered, the risk analysis is repeated, to build adequate mitigation [9].

5 Protection system lifecycle in reverse: Analysing existing systems

The risk-based approach can also be used to *analyse* existing systems and functions. This chapter presents a case study where risk-based analysis is used to consider the existing powering protection in the LHC. The key elements of this discussion are shown in Fig. 16:

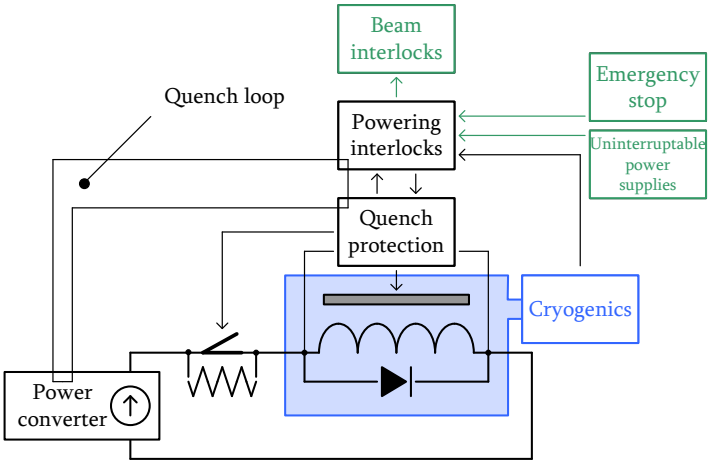

Fig. 16: Elements of a superconducting power system with protection

Appendix C gives a detailed description of powering circuit elements. Note that Fig. 16 is a simplification, For example, in the LHC dipole magnet system, 154 dipole magnets are powered in series and it contains two energy extraction systems, one at each end of the circuit.

5.1 Non-nominal energy deposition scenario

This case study considers the following electrical scenario, similar to the LHC. In this case seven magnets are connected in three electrical circuits, sharing a cryogenic bath. Consider a non-nominal energy deposition occurring in the central magnet (Fig. 17).

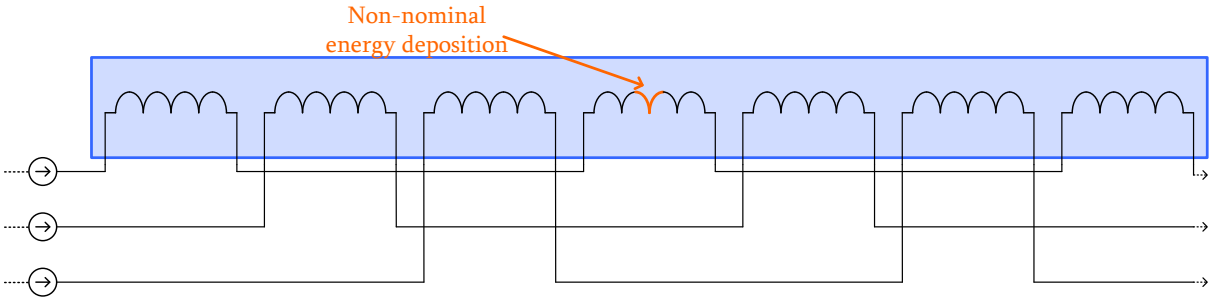

Fig. 17: Non-nominal energy deposition scenario

A hazard chain and risk matrix can be constructed using the same approach. In this case, to aid in the discussion, the definition of *probability* and *consequence*, as well as the four *risk classes*, is intentionally vague. The resulting chain and the risk matrix are shown in Fig. 18.

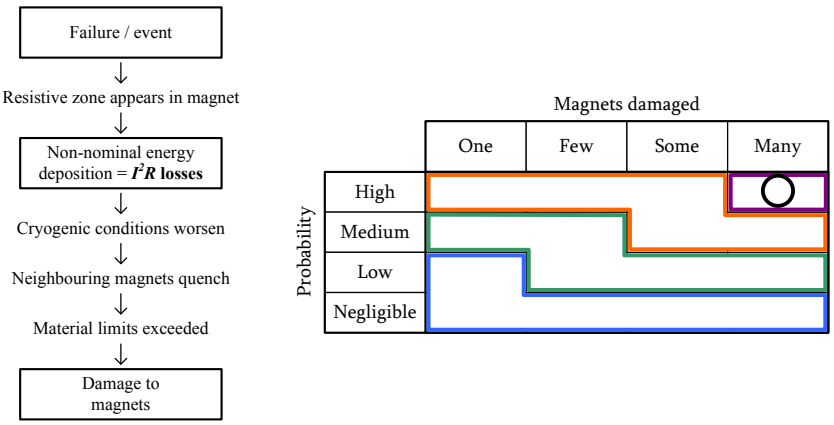

Fig. 18: Scenario hazard chain with unmitigated risk

There are four functions in place, breaking the hazard chain (Fig. 19).

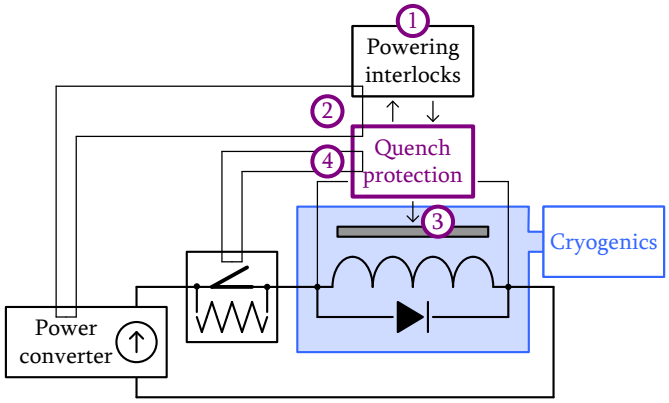

Fig. 19: Protection functions in a superconducting circuit scenario

- PF_1 – link-related circuits. The quench protection system informs the powering interlock controller of the detection of quench. The powering interlock carries out actions on neighbouring circuits to prevent non-nominal energy deposition in them, which could occur due to quench propagation.
- PF_2 – switch off power converter. The power converter is switched off, and no further energy is added to the magnet circuit. The power converter can only slowly extract circuit energy, pushing it back onto the mains supply over the course of several minutes.

– PF_3 – propagate the quench. The quench protection system activates a quench heater, which increases the quenched zone in the magnet, increasing the resistive area, and reducing the power density.

– PF_4 – extract energy from the magnetic circuit. The quench protection system triggers the opening of the bypass switch where the stored energy of the magnet circuit is removed as heat by including a purpose-built dump resistor in the electrical circuit.

PF_1 interrupts the chain in the prevent phase. The other three functions work in the protect phase. On the risk diagram the first function causes the risk to move to the left; as the impact of the failure is reduced, the other protection functions work together to move the risk down, reducing the risk probability (Fig. 20). Hence, the fully mitigated risk, with all protection functions, is in the acceptable region.

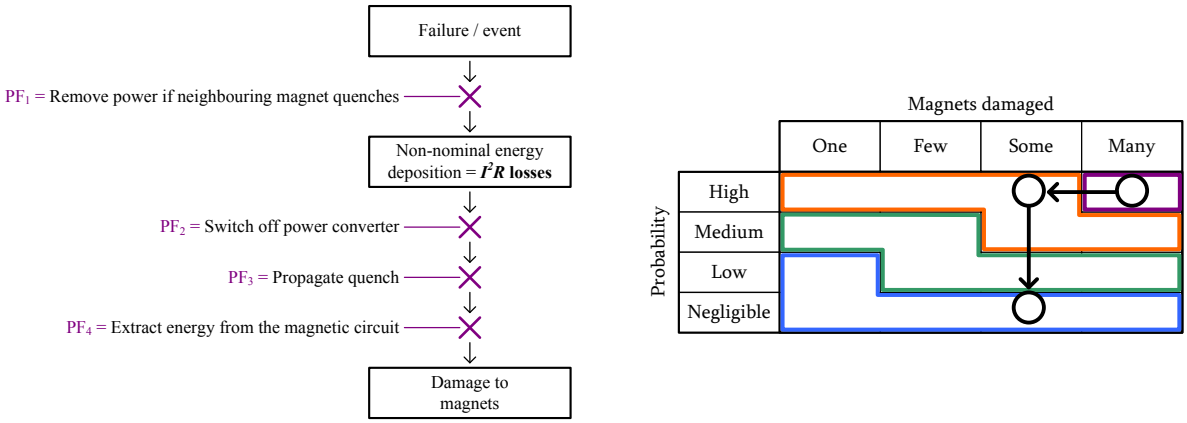

Fig. 20: Scenario hazard chain with mitigated risk

5.2 Reverse risk analysis

A reverse risk analysis of these protection functions can be carried out by determining the probability and scope of damage following malfunction. The figures in these descriptions come from system experts. The absolute values of risk associated can be debated; this is a worked example of the concept (Fig. 21).

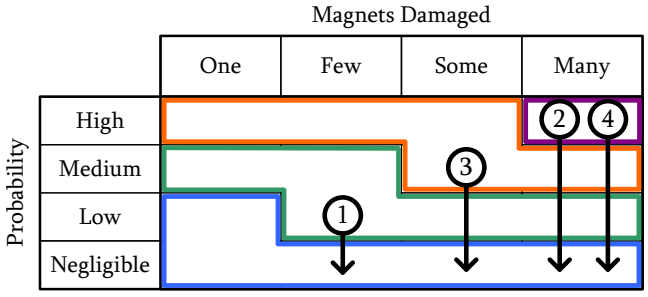

Fig. 21: Risk matrix with risk of protection function failure labelled

– PF_1 – link related circuits. If neighbouring circuits are not disabled, then the prevent phase of machine protection has been unsuccessful for those circuits; the other functions that are in place in the protect phase are still able to react. This means that there is a low probability of a few magnets being damaged.

– PF_2 – switch off power converter. If the power converter does not switch off, it will continue to add power to the quenched circuit until it can no longer maintain the output setpoint. If this occurs, there is a high probability of many magnets being damaged.

- PF_3 – propagate the quench. If the quench heater does not fire, the resistive losses in the coil will be localized to a single small area. There is a medium probability that some magnets are damaged.
- PF_4 – extract energy from the magnetic circuit. If the energy extraction fails to operate, the field decay time will be very long, vastly increasing the probability of damage o$_c$curring; this presents a high probability of many magnets being damaged.

PIL requirements for LHC powering protection systems

Working backwards from the previous risk matrix gives the RRL and consequently the PIL of the protection functions:

- PF_1 – link related circuits. Risk class 2 is therefore PIL 1.

  Quench protection system → powering interlock → powering interlock → power converter
- PF_2 – switch off power converter. Risk class 4 is therefore PIL 3.

  Quench protection system → power converter
- PF_3 – propagate the quench. Risk class 3 is therefore PIL 2.

  Quench protection system → quench heater
- PF_4 – extract energy from the magnetic circuit. Risk class 4 is therefore PIL 3.

  Quench protection system → energy extraction

5.3 Outcomes of reverse analysis

PIL figures can be compared to system knowledge, identifying elements that require further investigation or, conversely, those systems that have integrity level requirements that are too high. In these cases more methods should be found to understand how to remove the risk, or break the hazard chains more often, so sharing the integrity requirements amongst more systems and functions. This reduces the individual integrity needs of specific systems or connections.

6 Conclusions

This paper has described the principal risks in HEP powering systems, the basics of machine protection, the concepts of risk analysis, and a protection system lifecycle.

The paper has shown how the lifecycle can be used in the traditional manner, fitting the concept of IEC 61508, where a protection case is made from first ideas through to system realization. Due to the unique nature of HEP research machines, it is not always possible to be absolutely accurate in the prediction of risks and the assignment of protection functions. With this in mind, the paper concluded with a case study showing that the same lifecycle can be used in a reverse manner to allow analysis and appraisal of existing systems and functions, after machines have been operated and real information is gathered.

Risk is a critical parameter in modern engineering; it should be appreciated and understood by engineers involved in every aspect of HEP. Machine protection is driven by risk analysis. It is a discipline that continues to evolve to meet the changing demands of both the working environment and the types of machines being built. The LHC MPS is novel, being highly tailored to the machine's requirements, having an extremely fast reaction time, and a very high dependability. These are qualities that when combined, cannot be delivered by commercial systems.

Acknowledgements

This paper has been written in collaboration by the CERN Technology Department power conversion (TE/EPC) and machine protection (TE/MPE) groups. The authors wish to express their gratitude to the numerous individuals who have helped in developing this concept. In addition, the authors wish to acknowledge the contribution of the Warsaw University of Technology, in supervising and reviewing the Ph.D. written on dependable logic design, which first covered the topic of PIL.

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Appendix A: Organizational strategy

The development of the MPS is generally carried out by a wide range of experts from multiple disciplines, physicists defining particle simulations and interactions, and system-level experts, working with machine equipment. The MPS traverses organizations, and should be one of the key concerns when considering decisions related to accelerator operation.

It can be observed that organizational structures shown do not reflect a safety management scheme within a company. Structures in HEP are borne out of a confluence of deep-thinking academic and applied industrial approaches. The considerations of the MPS are multi-disciplinary. At CERN an initial machine protection working group (MPWG) was established as a forum to centralize studies, develop scenarios, and to exchange ideas related to machine protection. The MPWG was responsible for coordinating the development of the basic principles of LHC machine protection and organized the production of coherent documentation for all of the major protection systems and subsystems.

The MPWG oversaw the initial commissioning of the LHC powering systems and beam commissioning. Once machine commissioning was completed, the MPWG was renamed to the machine protection panel (MPP) to reflect the changing nature of the LHC from a machine under test to a machine for physics. In addition to this, a subset of the MPP was established, the restricted MPP (rMPP), which consolidates the opinions of the panel members and leads the decision-making processes during operational periods of the machine. Figure A.1 details the background and scale of the members of the MPP and rMPP.

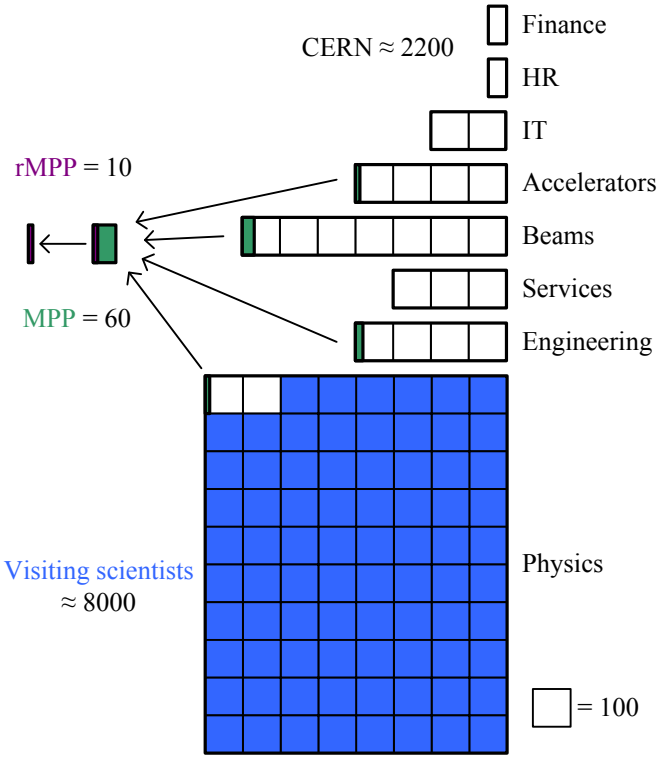

Fig. A.1: Protection expertise in CERN

From the machine point of view, the key forum for discussion is the LHC machine committee (LMC). This is an executive committee concerned with technical and performance aspects of the LHC. The LMC is responsible for the definition of operational parameters and the optimization of performance [10]. The rMPP reports on behalf of the MPP to the LMC. From this, and other reporting groups, senior management has sufficient information to take informed decisions. In this way there is

a clear chain of command concerning machine protection issues (Fig. A.2): from the frontline engineering teams, through to senior management.

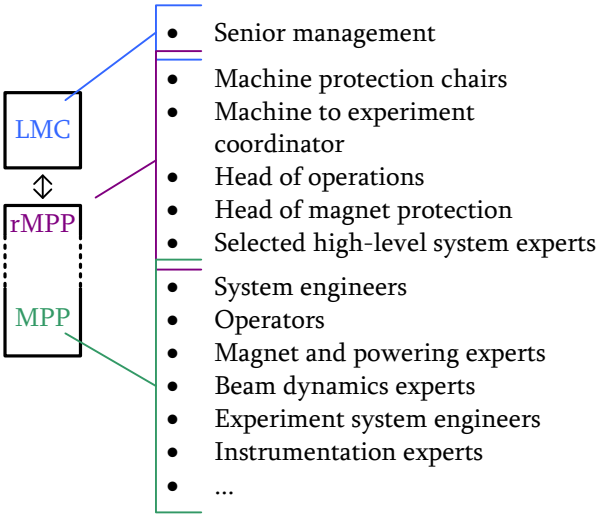

Fig. A.2: Protection chain of command

Appendix B: MPS doctoral research at CERN

MPS elements highlighted in Figure B.1 are those that have been subjects of doctoral level research.

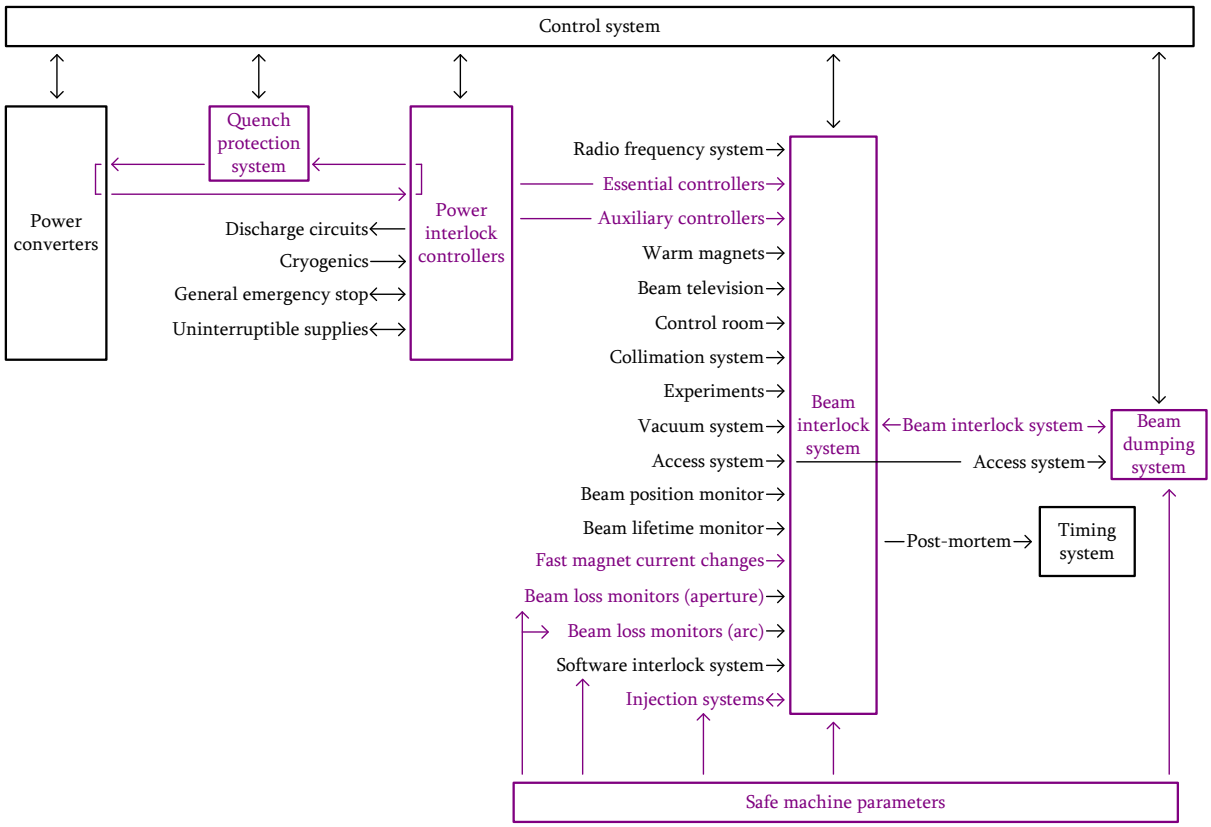

Fig. B.1: Elements of the MPS subject to Ph.D. research at CERN

– *Injection systems* – Machine protection & beam quality during the LHC injection process, V. Kain [11].

- *Quench protection system* – Reliability of the quench protection system for the LHC superconducting elements, A. Vergara [12].
- *Fast magnet current change monitor* – Redundancy of the LHC machine protection systems in case of magnet failures A. Gomez Alonso [5].
- *Beam interlock system* – A beam interlock system for CERN high energy accelerators, B. Todd [13].
- *Safe machine parameters* – Methods for the application of programmable logic devices in electronic protection systems for high energy particle accelerators, M. Kwiatkowski [7].
- *Power interlock controllers* – Powering and machine protection of the superconducting LHC accelerator, M. Zerlauth [6].
- *Beam loss monitor system* – Reliability of the beam loss monitors system for the Large Hadron Collider at CERN, G. Guaglio, and The real-time data analysis and decision system for particle flux detection in the LHC accelerator at CERN, C. Zamantzas [14].
- *Safety vs. availability* – LHC machine protection system: Method for balancing machine safety and beam availability, S. Wagner [9].

Appendix C: Elements of superconducting powering systems and protection

The key elements of the powering and protection of superconducting circuits are shown in Fig. C.1.

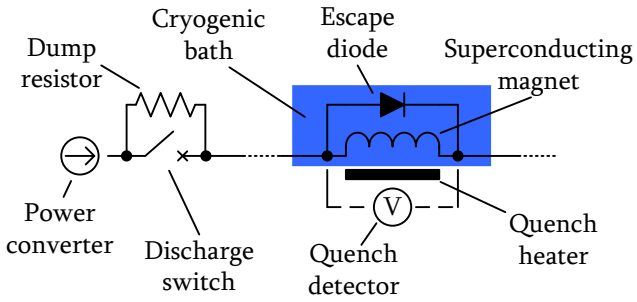

Fig. C.1: Components of a superconducting magnet and protection system

- Power converter, superconducting magnet, and cryogenic bath – these form the equipment under control. The converter regulates the magnet current required to achieve the machine beam performance requirements. The cryogenic system, of which only the bath is shown above, is responsible for maintaining the low temperatures required by the magnet in order to achieve superconductivity.
- Quench detector – this element determines the resistance of the magnet coil, by measuring the voltage drop from one end of the magnet to the other. An ideal superconductor should have no voltage drop, as it has no internal resistance. A voltage appearing over the magnet coil is an indicator that a quench is occurring, and is used to initiate the powering protection functions.
- Quench heater – once a quench is detected, heaters are used to force the quench to propagate over a large area. This reduces the power density of the quench, and decreases the chances of damage to the magnet coil.
- Escape diode – this further protects the magnet coil by providing an alternative current path around the quenching magnet coil. As the magnet quenches, the voltage drop increases, and

at one point this becomes high enough to switch on the escape diode. From this point the current bypasses the quenching magnet coil.

– Discharge switch and dump resistor – stored magnetic energy in the superconducting circuit has to be discharged after a quench has occurred. This is carried out by opening a discharge switch and adding a dump resistor in series with the magnet coil; the current in the circuit diminishes as power is lost as heat in the dump resistor.

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Thermal Design of Power Electronic Circuits

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Abstract
The heart of every switched mode converter consists of several switching semiconductor elements. Due to their non-ideal behaviour there are ON state and switching losses heating up the silicon chip. That heat must effectively be transferred to the environment in order to prevent overheating or even destruction of the element. For a cost-effective design, the semiconductors should be operated close to their thermal limits. Unfortunately the chip temperature cannot be measured directly. Therefore a detailed understanding of how losses arise, including their quantitative estimation, is required. Furthermore, the heat paths to the environment must be understood in detail. This paper describes the main issues of loss generation and its transfer to the environment and how it can be estimated by the help of datasheets and/or experiments.

Keywords
Conduction losses; switching losses; packages; thermal impedance; thermal cycling; power cycling.

1 Introduction

Figure 1 shows the structure of a typical switched mode converter—in this case a buck converter—fed by a diode rectifier with input and output filters.

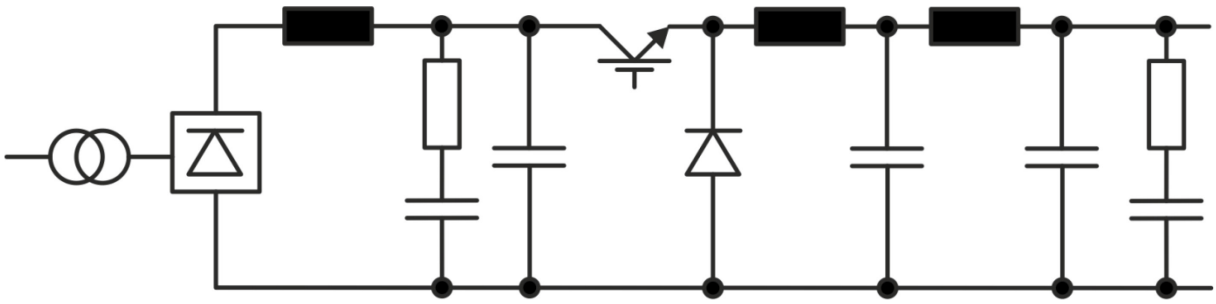

Fig. 1: Generic structure of a buck converter with diode rectifier and filters

Every component must be considered as a heat source. Also, capacitors carrying large alternating current (a.c.) heat up due to their ESR (equivalent series resistance), which can limit their lifetime, especially for electrolytic capacitors. Inductive devices like transformers and chokes have losses, and, due to their compact design, generate hot spots. Resistors are usually not critical as they are designated to dissipate power, and therefore designers are aware of their thermal behaviour.

The main heat sources are the semiconductors. They act as switching elements, i.e., they are either fully conducting or fully blocking. While the blocking losses are usually low enough to be negligible, the voltage drop in the ON state must be considered. At the transition between the ON and OFF states both the current through the semiconductor and the voltage across it are present for a short time causing switching losses.

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Special care must be taken if the chip temperature and/or the base plate temperature oscillate. This phenomenon is known by the terms ‘power cycling’ and ‘thermal cycling’. Temperature gradients cause additional mechanical stress to the soldering and welding joints inside a semiconductor module. The number of such thermal cycles is limited.

2 Heat sources

2.1 Resistors

Resistors with continuous load must be designed for a sufficient continuous heat transfer to the environment. At stable ambient temperature, a resistor’s temperature is also stable. The power ratings given in datasheets are maximum ratings for very effective cooling and maximum temperatures. It is recommended to oversize the devices considerably in order to prevent hotspots or aging problems.

A resistor with a pulsed load must be designed to absorb the energy during the pulse. As a consequence of this the temperature of the resistor rises quickly. Pulse resistors therefore have a large amount of active material, such as wires or cast iron. After the pulse, there must be enough time for the active material to cool down, before the next pulse occurs. There must be adequate overload protection, i.e., limitation of the pulse duration, limitation of the pulse repetition frequency, or even a temperature measurement of the active material.

Cables must also be treated as resistors, and they must be designed and installed to allow sufficient heat transfer to the environment. Cables with sufficient cross-section should be used. This may result in higher costs at installation, but offsets the energy saving during the increased life period due to lower temperatures. The skin effect must also be considered: the penetration depth in copper is approximately 2.1 mm at 1 kHz and approximately 0.66 mm at 10 kHz. This reduces the effective cable cross-section and can lead to overheating. Large cable bundles should be avoided, when the current density is high, and there should be sufficient air circulation.

2.2 Magnetic components

Magnetic components like chokes and transformers dissipate power in both the core and the winding. Core losses are caused by *eddy current losses* and *hysteresis losses*.

Depending on the frequency, the eddy current losses are minimized by different means. For low frequencies up to approximately 1 kHz the cores are built with core plates: the thinner the core plates, the lower the eddy currents. For higher frequencies (from 1 kHz to approximately 10 kHz) powder cores are used. These can be seen as cores with extremely thin core plates, and therefore tend to have considerably fewer eddy current losses. In the frequency range above 10 kHz ferrite is the core material of choice. Ferrite cores have a very poor electric conductivity and therefore have almost no eddy currents.

Hysteresis losses arise from the periodic reversal of magnetism, which requires energy. The energy is proportional to the area of the hysteresis curve. Transformers are designed to have a small area of the hysteresis curve in order to minimize the losses. Be aware that the core losses of a transformer are also present at zero load! The hysteresis curves of d.c. chokes (which are designed to store a lot of magnetic energy) span a large area. The ripple current in such a choke causes the core to run through only a small part of the hysteresis area. The hysteresis losses depend very much on the amplitude and the frequency of the ripple current.

Winding losses, also called Cu losses, arise from the ohmic resistance of the winding. The dissipated power is approximately proportional to I^2. The resistance of a copper winding increases approximately 0.4% per kelvin, i.e., a temperature raise of 25 K increases the winding losses by approximately 10%.

There are good reasons to keep the temperatures of both the core and the winding as low as possible, even if it costs something: winding and core losses increase with higher temperatures. Losses in general are expensive; there are not only the costs of the electric energy, but also the costs for re-cooling. Lower temperatures increase the life period. This is especially important for components which are used permanently under high load.

2.3 Semiconductors

In most power electronic applications semiconductors are either switched on or off. Therefore, we have either current through the semiconductor or voltage across it, but never both at the same time. But that is only valid in an ideal world. In reality, there are voltage drops in the ON state, which cause conduction losses. There are also leakage currents in the OFF state, but they are usually very low and therefore not considered here. At the transition between the ON and OFF states both current through the semiconductor and voltage across it are present. This leads to high power dissipation for a very short time.

In order to estimate the losses in our application, we have to consult the datasheet. In the following the losses of a buck converter according to Fig. 1 are estimated. The converter is designed for a maximum output current I_{Out} of 400 A and a maximum output voltage V_{Out} of 200 V. The d.c.-link voltage V_{dc} is 250 V. The switching frequency is 20 kHz. The combination of an IGBT (insulated-gate bipolar transistor) and a freewheeling diode is realized with a half bridge module FF600R06ME3 from Infineon. The graphs in Figs. 2–4 and Fig. 11 originate from its datasheet; see Ref. [1].

2.3.1 Conduction losses in the IGBT and the diode

During the ON state of the IGBT the output current flows through the IGBT. Its voltage drop can be derived from the output characteristic in the datasheet; see Fig. 2. The modulation index m is the ratio $V_{\mathrm{Out}}/V_{\mathrm{dc}}$, and in a buck converter this is also the time ratio ON state/switching period. The voltage drop depends on the junction temperature. We make a pessimistic estimate for the junction temperature and get V_{CE} from Fig. 2. In our example the conduction losses in the IGBT are given by

$$P_{\mathrm{cI}} = m \cdot I_{\mathrm{Out}} \cdot V_{\mathrm{CE}} = 0.8 \cdot 200\ \mathrm{A} \cdot 1.1\ \mathrm{V} = 176\ \mathrm{W}\,. \tag{1}$$

During the OFF state of the IGBT, the output current flows through the freewheeling diode. Its voltage drop can be derived from the forward characteristic figure in the datasheet; see Fig. 2. In contrary to the transistor, the diode usually has a negative temperature coefficient. Therefore we consider a rather low estimate for the junction temperature and get V_{F} from Fig. 2. In our example the conduction losses in the diode are given by

$$P_{\mathrm{cD}} = (1 - m) \cdot I_{\mathrm{Out}} \cdot V_{\mathrm{F}} = (1 - 0.8) \cdot 200\ \mathrm{A} \cdot 1.15\ \mathrm{V} = 46\ \mathrm{W}\,. \tag{2}$$

Note: If the converter operates at a low modulation index for the maximum output current, the diode has many more conduction losses!

Some manufacturers specify V_{CE} and V_{F} only at the chip level, as this is relevant to determine the losses in the silicon chip. In addition to this there is also a resistance between the silicon chip and the terminals. These losses are mainly transported to the environment through the terminals and the connected cables. They may also be considered for an overall estimate of the losses. In the datasheet [1] this resistance is called $R_{\mathrm{CC'+EE'}}$ and its value is 1.1 mΩ per switch. In our example with $I_{\mathrm{Out}} = 200$ A and $m = 0.8$ this leads to an additional voltage drop of 0.22 V in each branch and to additional losses of 35 W in the IGBT branch and 9 W in the diode branch.

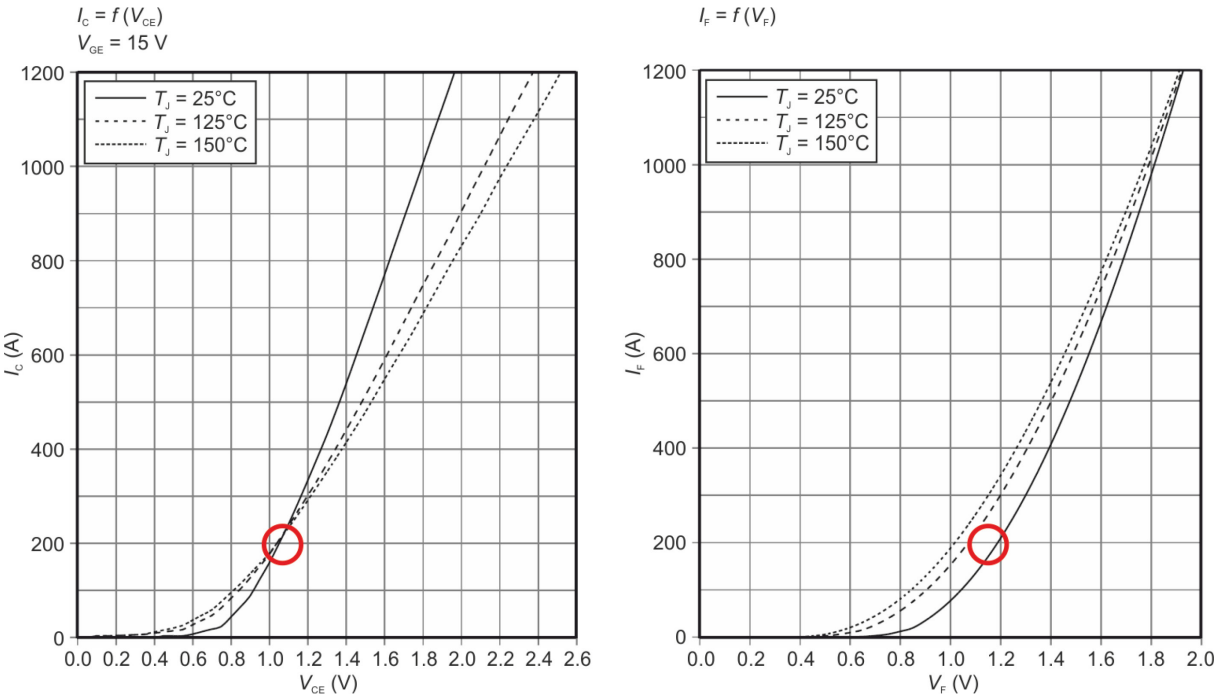

Fig. 2: Output characteristic of the IGBT for a gate-emitter voltage V_{GE} of 15 V (left) and forward characteristic of the diode (right).

2.3.2 Switching losses in the IGBT

The dissipated energy E_{on} and E_{off} at each switching is given in the datasheet. The graphs are given for discrete reference junction temperatures T_{Ref}, e.g., 125ºC or 150ºC; see Fig. 3. For a different junction temperature T_J a correction factor applies; refer to Eq. (3). Accordingly, the graphs are given for a reference blocking voltage V_{ref}, e.g., 300 V. For a different blocking voltage V_{CE}, a correction factor applies; refer to Eq. (3). The switching losses in the IGBT are given by

$$P_{sI} = f_s \cdot (E_{on} + E_{off}) \cdot \left(1 + TC\left(T_J - T_{Ref}\right)\right) \cdot (V_{CE}/V_{ref})^{KV} \ . \tag{3}$$

For transistors, $TC \sim 0.003\ \mathrm{K}^{-1}$ and $K_V \sim 1.3\text{–}1.4$; see Ref. [2], p. 287. With the values from our example with f_s = 20 kHz, $V_{CE} = V_{dc}$ = 250 V, and an estimated junction temperature T_J of 90ºC, we get

$$P_{sI} = 20{,}000\ \mathrm{s}^{-1} \cdot (5 + 8) \cdot 10^{-3}\ \mathrm{J} \cdot (1 + 0.003 \cdot (90 - 125)\ \mathrm{K}) \cdot \left(\frac{250\ \mathrm{V}}{300\ \mathrm{V}}\right)^{1.35} = 182\ \mathrm{W}.$$

Be aware that the switching losses are highly dependent on the gate resistance; see Fig. 3 (right). Hard switched converters are usually optimized for very fast switching in order to minimize the losses. However, if the switching needs to be softer, e.g., for EMC reasons (electromagnetic compatibility), this can be achieved by increasing the gate resistor. As shown in Fig. 3 on the right, this dramatically increases the switching losses.

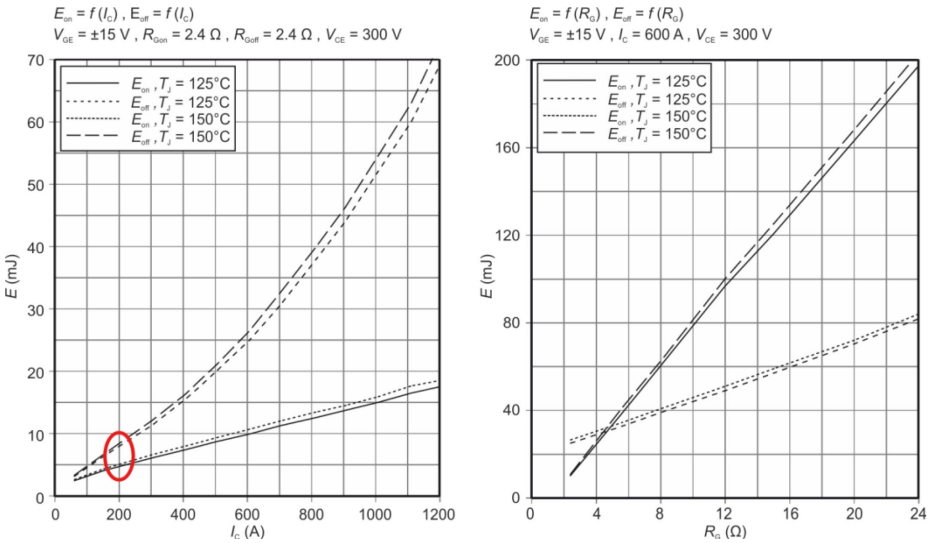

Fig. 3: Switching losses in the IGBT for a gate-emitter voltage V_{GE} of ±15 V

2.3.3 Switching losses in the diode

The dissipated energy E_{rec} at each switching OFF is given in the datasheet. The graphs are given for discrete reference junction temperatures T_{Ref}, e.g., 125ºC or 150ºC; see Fig. 4. For a different junction temperature T_J a correction factor applies; refer to Eq. (4). Accordingly, the graphs are given for a reference blocking voltage V_{ref}, e.g., 300 V. For a different blocking voltage V_{CE}, a correction factor applies; refer to Eq. (4). The switching losses in the diode are given by

$$P_{sD} = f_s \cdot E_{rec} \cdot \left(1 + TC\left(T_J - T_{Ref}\right)\right) \cdot \left(V_{CE}/V_{ref}\right)^{KV}. \tag{4}$$

For diodes, $TC \sim 0.006\ \mathrm{K}^{-1}$ and $K_V \sim 0.6$; see Ref. [2], p. 287. With the values from our example with f_s = 20 kHz, $V_{CE} = V_{dc}$ = 250 V, and an estimated junction temperature T_J of 90ºC, we get

$$P_{sD} = 20{,}000\ \mathrm{s}^{-1} \cdot 5 \cdot 10^{-3}\ \mathrm{J} \cdot (1 + 0.006 \cdot (90 - 125)\ \mathrm{K}) \cdot \left(\frac{250\ \mathrm{V}}{300\ \mathrm{V}}\right)^{0.6} = 71\ \mathrm{W}.$$

In contrary to the IGBT, a softer switching (higher gate resistance R_G) reduces the switching losses of the freewheeling diode remarkably; see Fig. 4 (right).

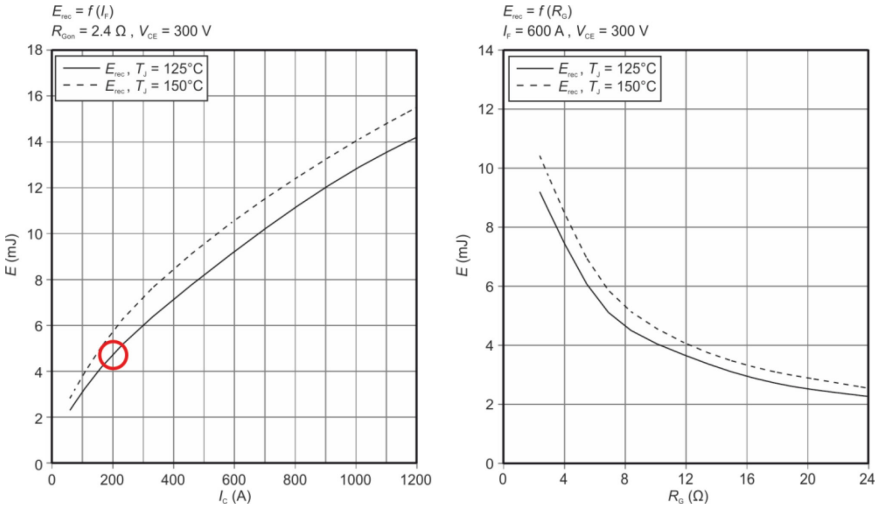

Fig. 4: Switching losses in the diode

2.3.4 Total IGBT and diode losses

Inside the module the heat is generated in two different silicon chips, the IGBT and the diode. The IGBT losses P_I and the diode losses P_D are given by

$$P_I = P_{cI} + P_{sI} = 176\ W + 182\ W = 358\ W, \quad (5)$$

$$P_D = P_{cD} + P_{sD} = 46\ W + 71\ W = 117\ W. \quad (6)$$

They are needed to determine the junction (chip) temperatures; see Section 3.2. In addition to that the module lead resistance $R_{CC'+EE'}$ causes terminal losses P_{Term}.The overall losses for the entire module P_M are given by

$$P_M = P_I + P_D + P_{Term} = 358\ W + 117\ W + 44\ W = 519\ W. \quad (7)$$

This figure is needed to determine the overall converter losses and the efficiency.

3 Heat transfer

3.1 Packages

The losses as described in Section 2 originate in the silicon chips and must be transferred to the environment by means of heat sinks. Different packaging concepts are used (see Fig. 5) depending on the power rating.

For small discrete elements mounted on a PCB, the heat flows via the electrical connections and/or the air. The tracks on the PCB can be used as heat conductors in order to spread the heat to a large area or to lead the heat to a heat sink or the housing. See Section 3.5 for a practical example. The calculation of the resulting junction temperatures is difficult, and requires a detailed thermal modelling of the entire arrangement (semiconductor and PCB) and a time-consuming finite element analysis. Therefore usually a ‘trial and error’ approach is used.

Larger discrete elements have a cooling surface, which can be soldered to a copper pad or pressed onto a heat sink. Refer to Section 3.5 for a practical example. The thermal resistance between the silicon chip and the cooling surface is given in the datasheet. Note that usually the cooling surface is connected to one of the electrical connections. If isolation is needed, it needs to be realized separately.

Large semiconductor modules have isolated cooling plates, which can be connected to ground level. Refer to the example in Section 2.3. Most of the losses produced in such elements are dissipated through this cooling plate.

Very large semiconductors are packed in press-pack housings. They have large contact surfaces, which serve as both electrical and thermal connections.

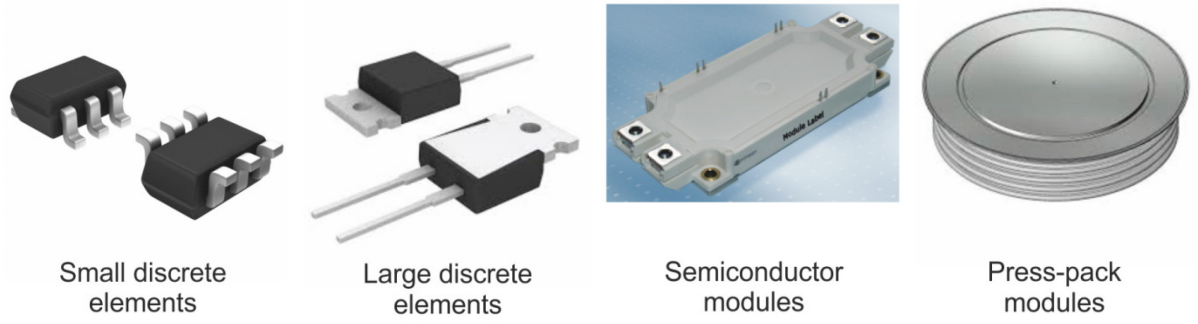

Fig. 5: Different packages for semiconductor devices

Figure 6 shows typical cross-sections of an isolated module package and a press-pack module. In the isolated module package the heat from the silicon chips must flow through the ceramic insulator and the soldering joints to the copper base. The press-pack housing does without soldering joints and ceramic insulator, and therefore has a much more effective heat transfer to the heat sink. Furthermore it can be cooled from both sides, but the two heat sinks are on different electrical potentials, usually neither of them connected to ground.

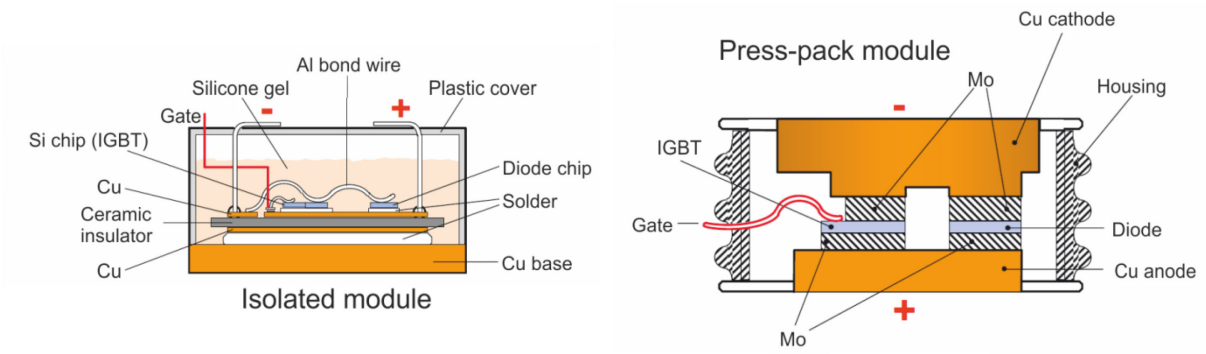

Fig. 6: Typical cross-sections for different housing concepts

3.2 Steady-state temperatures

The losses in both the IGBT and the freewheeling diode cause temperature differences in the thermal resistor network, as shown in Fig. 7. In steady state, the losses and the ambient temperature are constant. Therefore the resulting temperatures in the module are also constant.

The thermal resistances R_{thJC} (junction to case) for both the IGBT and the diode can be found in the datasheet. Note: In data sheets the Cu base of an isolated module is also called ‘case’. The thermal resistance R_{thCH} (case to heat sink) is also given in the datasheet; this depends not only on the module itself, but also on the way the element is mounted to the heat sink. The surfaces of the device and the heat sink both have a certain roughness and therefore there are inherent air gaps between the two. In order to achieve an effective heat flow, these air gaps must be filled by a Thermal Interface Material (TIM). The application notes from the semiconductor suppliers for proper mounting of the element should be consulted; an example is given in Ref. [3]. The thermal resistance of the heat sink R_{thHA} (heat sink to ambient) is either given by the manufacturer or can be determined by means of an experiment.

With this information, the corresponding temperature differences can be calculated by multiplying the power flow by the thermal resistance.

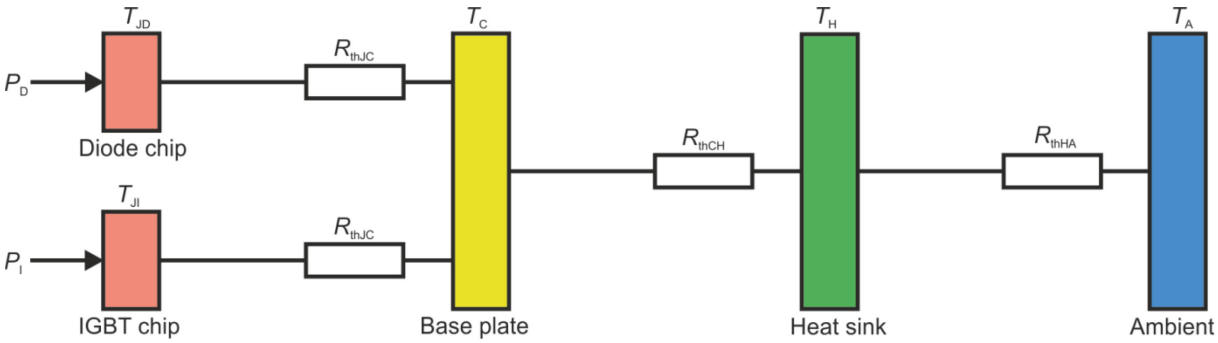

Fig. 7: Power flow from silicon to ambient

For the example in Section 2.3 we found losses of 358 W for P_I and 117 W for P_D. In the datasheet [1] we find thermal resistances of 0.09 K/W for R_{thJC} for the IGBT, 0.15 K/W for R_{thJC} for the diode, and 0.009 K/W for R_{thCH}. The thermal resistance of the heat sink R_{thHA} we assume to be 0.1 K/W. These figures are recorded in Fig. 8.

On multiplying the power flow by the corresponding thermal resistances we get the temperature differences ΔT_{JCI} (IGBT junction to case) = 32 K, ΔT_{JCD} (diode junction to case) = 18 K, ΔT_{CH} (case to heat sink) = 4 K, and ΔT_{HA} (heat sink to ambient) = 48 K. If we assume the ambient temperature to be 35ºC we get the absolute temperatures T_H (heat sink) = 83ºC, T_C (base plate) = 87ºC, T_{JD} (diode junction) = 105ºC, and T_{JI} (IGBT junction) = 119ºC. The results are summarized in Fig. 8.

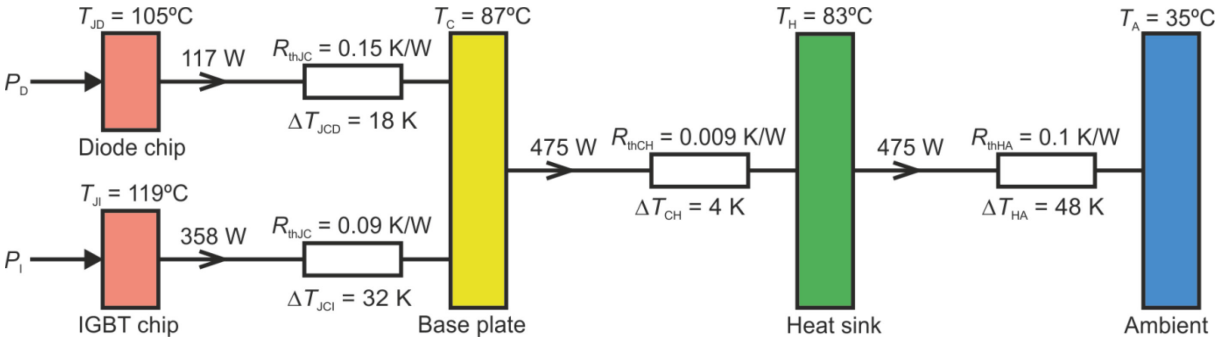

Fig. 8: Power flow for example in Section 2.3

According to the datasheet [1], the IGBT module used for our example may be operated at junction temperatures up to 150ºC. The loss calculation and the thermal calculations are not very accurate, and we also have to consider long-term drifts of the parameters involved. Therefore a safety margin of at least 25 K is necessary. Our example revealed a margin of 31 K, which is quite close to that limit. In general, lower temperatures raise the MTBF (mean time between failures) and the long-term reliability. It is left to the designer to make a reasonable trade-off between exploiting the elements and long-term reliability.

3.3 Transient thermal impedance

The loss and temperature calculations mentioned in Section 3.2 are valid for steady-state conditions only. If the losses vary with time (pulsating or oscillating), the thermal impedance has to be considered instead of the simple thermal resistance. From the thermal point of view, the arrangement shown in Fig. 6 (left) can be seen as a row of thermal capacitances (Si chip–solder–ceramic insulator–solder–Cu base) interconnected by thermal resistances. This leads to the continued fraction model, also known as the Cauer model, the T-model, or the ladder network (see Fig. 9). This model requires detailed knowledge of the material characteristics of the individual layers. However, the correct modelling of the thermal spreading is difficult.

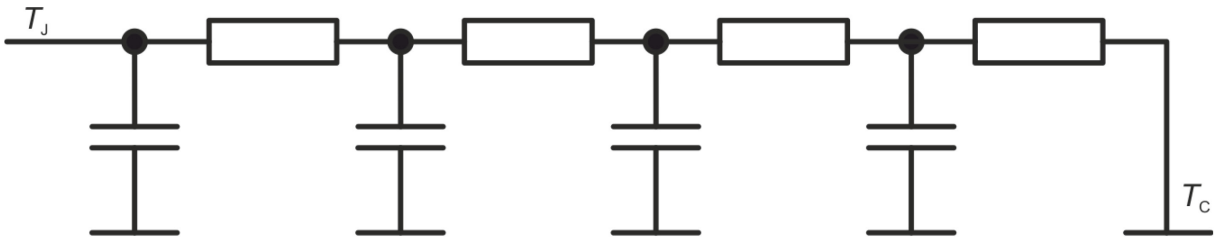

Fig. 9: Cauer model

Most manufacturers publish data for the partial fraction model, also known as Foster model or the Pi model (see Fig. 10).

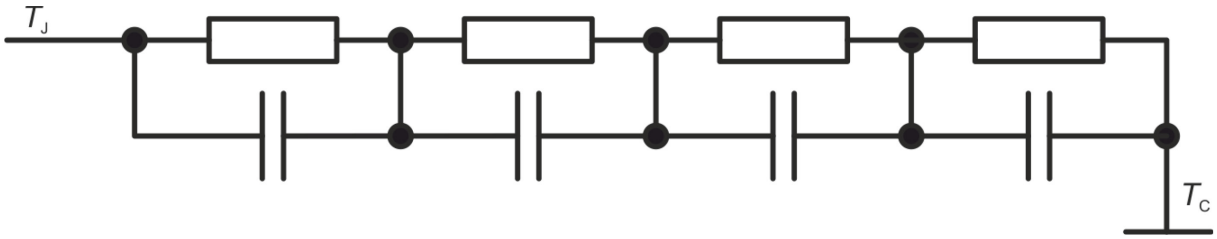

Fig. 10: Foster model

This model does not represent the layer sequence; the network nodes do not have any physical correlation. The thermal impedance

$$Z_{\mathrm{thJC}}(t) = \sum_{i=1}^{n} r_i \cdot \left(1 - \mathrm{e}^{-\frac{t}{\tau_i}}\right) \tag{8}$$

as a function of time is usually given in the datasheet; see Fig. 11 and Ref. [1]. The sum of the individual thermal resistances r_i corresponds to the steady-state thermal resistance R_{thJC}. The time constants are typically in the region of 10 to 100 ms. If the power fluctuations are faster than that, e.g., losses during one switching period, we may simplify the calculation and consider the average power only, as in Section 2.3.

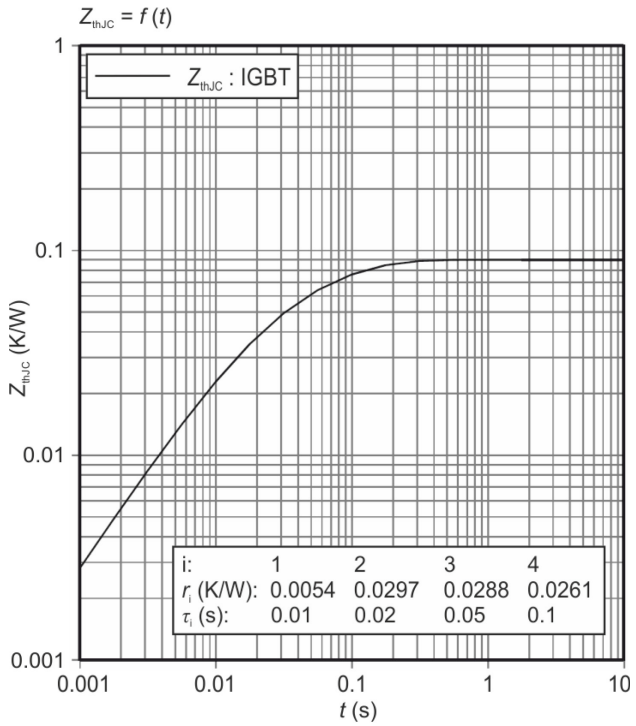

Fig. 11: Transient thermal impedance

Once the losses and the base plate temperature as a function of time are known, the junction temperature as a function of time can be determined as

$$T_{\mathrm{J}}(t) = P(t) \cdot Z_{\mathrm{thJC}}(t) + T_{\mathrm{C}}(t). \tag{9}$$

For more information about transient thermal impedance see Ref. [4]; note that Figs. 9 and 10 originate from this reference.

3.4 Temperature oscillations

When the junction and the case temperatures oscillate, material fatigue has to be considered. Problems arise from different expansion coefficients for different materials and conjoined mechanical stress; see Table 1 and Fig. 6.

Table 1: Expansion coefficients for different materials

Material	**Expansion coefficient (10^{-6}/K)**
Silicon	4.1
Copper	17
Aluminium	24
Molybdenum	5
Solder	15–30
Ceramic	5–9

3.4.1 Thermal cycling

Temperature oscillations of the base plate are referred to as ‘thermal cycling’. There is a large-area soldering joint between the ceramic insulator and the base plate, which accomplishes a good thermal conductivity. The expansion coefficients for copper and solder material match reasonably well, but the ceramic material differs by a factor of 2 or more. This causes mechanical stress to the soldering joint, which leads to accelerated aging. Finally, the thermal resistance increases, the temperature oscillations become even larger, and the device fails.

Thermal cycling problems can be avoided by using water cooling with a constant water inlet temperature, which keeps the temperature of the heat sink and the base plate nearly constant.

3.4.2 Power cycling

Temperature oscillations of the silicon chip are known as ‘power cycling’. The expansion coefficients of aluminium (bond wires) and silicon (semiconductor chip) differ by a factor of 6. When the temperature oscillates there is mechanical stress to the bond-wire welding. After some time, the bond wires start to lift off. This causes an increased voltage drop V_{CEsat} , which increases the losses. This leads to an even larger temperature oscillation, and the device finally fails.

Press-pack devices do not have bond wires for the main connections and are therefore less sensitive to power-cycling stress.

In the mid-1990s in the scope of the LESIT project, standard modules with base plates from different manufacturers were tested regarding their power-cycling capability. During the project, a large volume of data was collected. Figure 12 shows the results for different temperature oscillations at three medium temperatures T_{m}.

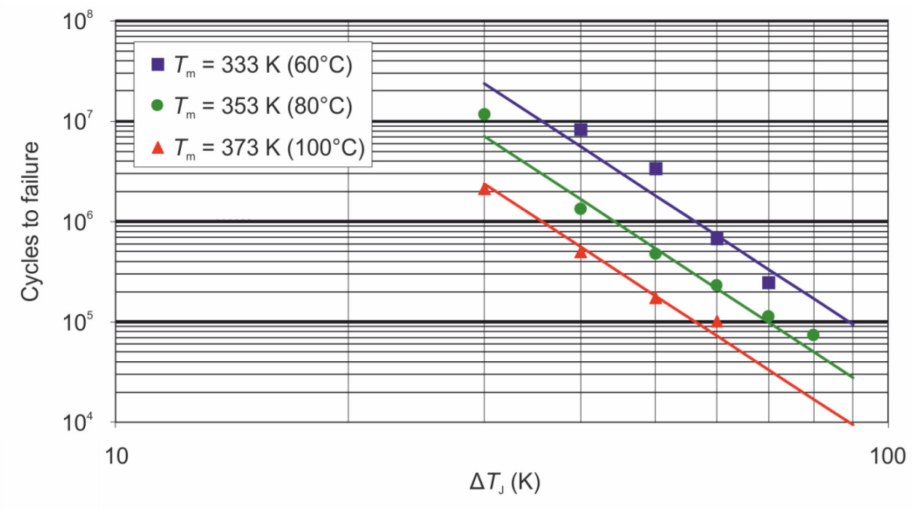

Fig. 12: Results from the LESIT project

Almost 20 years have passed, and the development of better packaging has evolved. Today there are specialized and improved devices on the market. However, for a first assessment, the LESIT figures are still valuable.

3.4.3 Practical experience with power cycling

The output current of the booster dipole power supply (PS) of the Swiss Light Source (SLS) oscillates with a 320 ms cycle time, i.e., with a frequency of 3.125 Hz, from zero to full current and back to zero. The SLS works in top-up mode, i.e., a short refilling of the storage ring takes place approximately once every 100 s. In the first 4 years of operation the booster PS was permanently on. Since then, the PS is only turned on during the refilling procedure of the storage ring, in order to save energy. During the remaining time, it is on standby. After 3.5 years in this 'energy-saving mode' we experienced two IGBT failures within a month. That was a clear sign of a systematic and reproducible aging problem, probably due to power cycling.

Measurements combined with simulations showed a temperature excursion as shown in Fig. 13. During standby, the chip temperature corresponds to the cooling-water inlet temperature, which is stabilized to 30ºC. Once every 100 s the chip temperature is raised from 30ºC to 86ºC. For approximately 5 s there is a second oscillation with a 320 ms cycle time superimposed, where the chip temperature oscillates between 68ºC and 82ºC. This raised the question: which of the two oscillations killed the IGBTs?

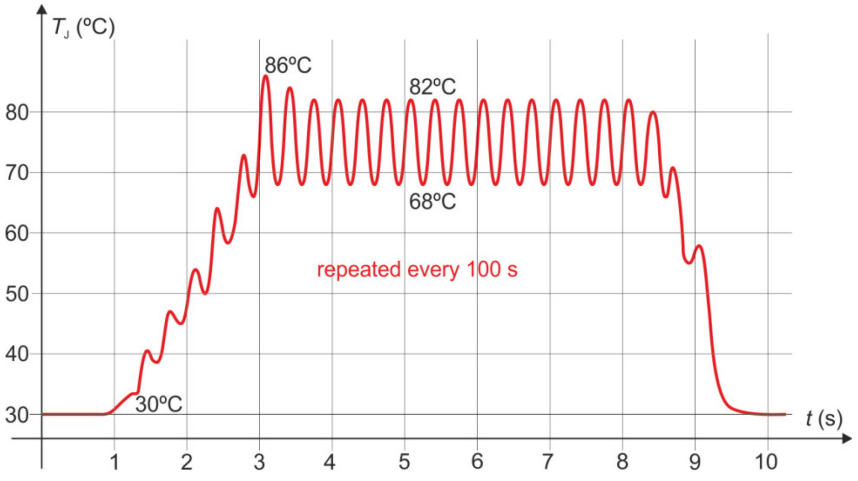

Fig. 13: Practical example of an IGBT junction temperature excursion

The 320 ms oscillation has a medium temperature of 75ºC and a peak-to-peak amplitude of 14 K. By extrapolating the LESIT results (see Fig. 14, dotted line) we can expect a lifetime of approximately 5×10^8 cycles. During the first 4 years of continuous operation (40 weeks per year) we gathered approximately 3.0×10^8 cycles. During the following 3.5 years in energy-saving mode (40 weeks per year, 16 cycles every 100 s) we gathered another 1.5×10^7 cycles, which sums to a total of 3.2×10^8 cycles. This is considerably below the expected lifetime. Furthermore, it is doubtful whether such an extreme extrapolation of the LESIT results is appropriate.

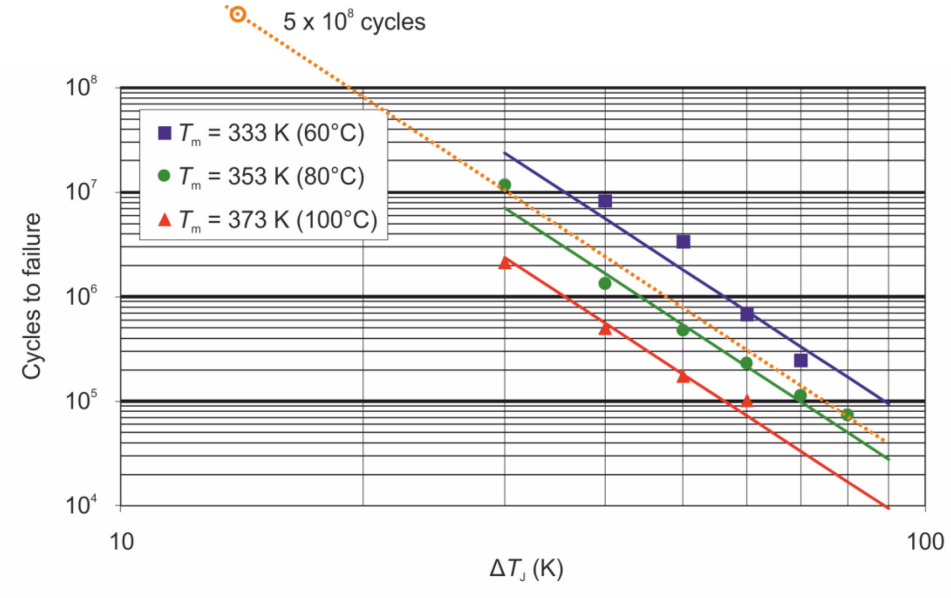

Fig. 14: Extrapolation of the LESIT results for the 320 ms cycles

The 100 s oscillation has a medium temperature of 58ºC and a peak-to-peak amplitude of 56 K. By interpolating the LESIT results (see Fig. 15, dotted line) we can expect a lifetime of approximately 1×10^6 cycles. During the first 4 years of continuous operation, there were only a few such cycles. During the following 3.5 years in energy-saving mode (40 weeks per year, one cycle every 100 s) we gathered approximately 8.5×10^5 cycles. This is very close to the expected lifetime and most likely killed the IGBTs.

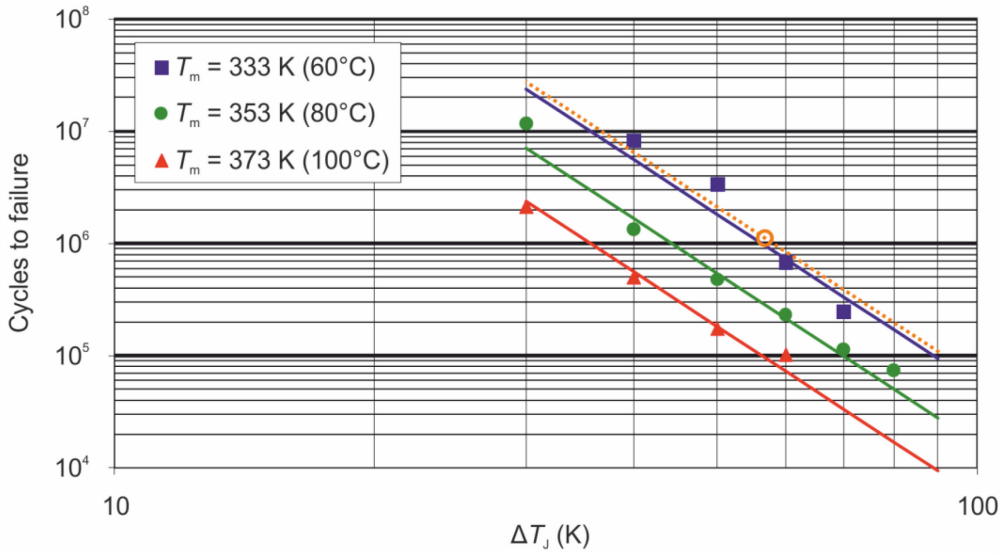

Fig. 15: Interpolation of the LESIT results for the 100 s cycles

3.5 Practical example: thermal design on a PCB

For the free electron laser SwissFEL at the Paul Scherrer Institute (PSI), a new bipolar 10 A/24 V converter has been developed, which is installed on a 100 mm × 160 mm PCB. The calculation of the resulting junction temperatures is difficult; this would require a detailed thermal modelling of the entire arrangement (semiconductor and PCB) and a time-consuming finite element analysis. Instead, we designed a first prototype, measured the temperature distribution on the board, and made improvements to the design. Figure 16 depicts a thermal image of the first prototype. It shows a very inhomogeneous board temperature with several hot spots up to 117ºC.

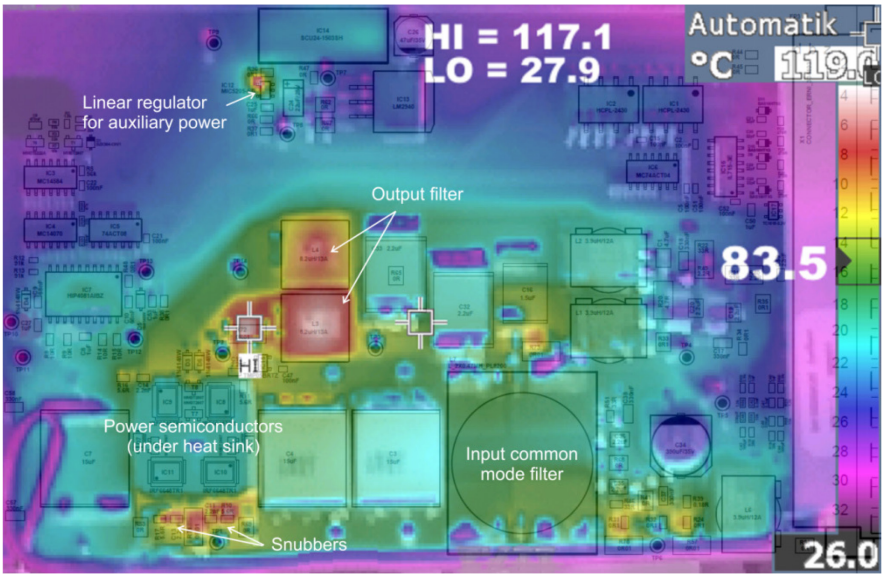

Fig. 16: Thermal image of the first prototype

For EMC reasons the entire PCB must be enclosed in a metallic housing. It was one of the main goals of the development project to design a converter that does not need any forced cooling. This requires a cooling design that uses the metallic shielding for a heat sink. In order to transfer the heat from the various hot spots on the PCB to the shielding, improvements in the design were necessary.

The thermal conductivity for materials used on a PCB differs greatly; see Table 2. The PCB core material is only about 10 times better than air, but 1000 times worse than metals. Heat-transfer foils are rather bad but unavoidable because they perform the electrical isolation. Therefore the strategy must be to conduct the heat as much as possible through metals.

Table 2: Thermal conductivity λ for different materials

Material	**Thermal conductivity λ (W/K m)**
Gold	318
Silver	429
Copper	401
Aluminium	237
Steel	50
Heat-transfer foil	2
PCB core material (FR-4)	0.3
Air	0.025

The four MOSFETs for the converter are mounted on the top side of the PCB on an area of approximately 2 cm × 2 cm = 4 cm^2. At full load the losses are approximately 10 W. The core thickness is 1.6 mm. The thermal resistance from top to bottom through the PCB core material is

$$R_{\mathrm{th}} = \frac{l}{\lambda \cdot A} = \frac{1.6 \cdot 10^{-3}\ \mathrm{m}}{0.3\ \frac{\mathrm{W}}{\mathrm{K \cdot m}} \cdot 4 \cdot 10^{-4}\ \mathrm{m^2}} = 13.3\ \mathrm{K/W}. \tag{10}$$

This causes a temperature difference from top to bottom of

$$\Delta T = R_{\mathrm{th}} \cdot P = 13.3\ \frac{\mathrm{K}}{\mathrm{W}} \cdot 10\ \mathrm{W} = 133\ \mathrm{K}. \tag{11}$$

These figures clearly show that the heat transfer through the PCB core material is not sufficient.

Vias (borings coated with copper) are used for electrical connections from one layer to another. Such vias (see Fig. 17 for the geometry) can also be used to transfer the heat from the top layer to the bottom one.

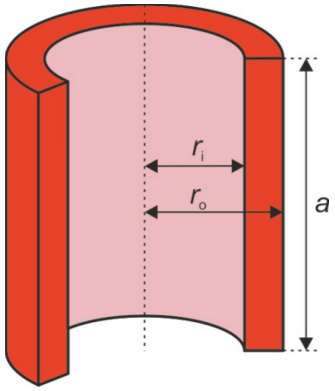

Fig. 17: Geometry of a via

The copper coating inside the boring has an outside radius r_o of 0.175 mm and an inside radius r_i of 0.15 mm. Its length a is 1.6 mm, which corresponds to the core thickness of the PCB. The effective cross-section is

$$A = (r_{\mathrm{o}}{}^2 - r_{\mathrm{i}}{}^2) \cdot \pi = (0.175^2 - 0.15^2)\ \mathrm{mm^2} \cdot \pi = 0.0255\ \mathrm{mm^2}. \tag{12}$$

The resulting thermal resistance for a single via is therefore

$$R_{\mathrm{th}} = \frac{l}{\lambda \cdot A} = \frac{1.6 \cdot 10^{-3}\ \mathrm{m}}{401\ \frac{\mathrm{W}}{\mathrm{K \cdot m}} \cdot 0.0255 \cdot 10^{-6}\ \mathrm{m^2}} = 157\ \mathrm{K/W}. \tag{13}$$

On an area of 4 cm^2 there is space for 8 × 8 = 64 parallel vias, which reduces the overall thermal resistance to 2.45 K/W. This thermal resistance is in parallel to the one of the PCB core materials, and the resulting temperature difference

$$\Delta T = R_{\mathrm{th}} \cdot P = \frac{1}{\frac{1}{13.3\ \frac{\mathrm{K}}{\mathrm{W}}} + \frac{1}{2.45\ \frac{\mathrm{K}}{\mathrm{W}}}} \cdot 10\ \mathrm{W} = 20.7\ \mathrm{K} \tag{14}$$

between the top and bottom layers is acceptable.

Originally we had only one 70 μm layer for the signal and power wiring (Fig. 18, left). In the final design (Fig. 18, right), there are 105 μm layers on the top and bottom sides and two additional

35 μm layers in between. All four layers are electrically and thermally connected together. That reduces the current density in the power wiring and allows for an effective heat spread and heat transfer from top to bottom. The overall thickness of the PCB was reduced from 1.7 mm to 1.4 mm.

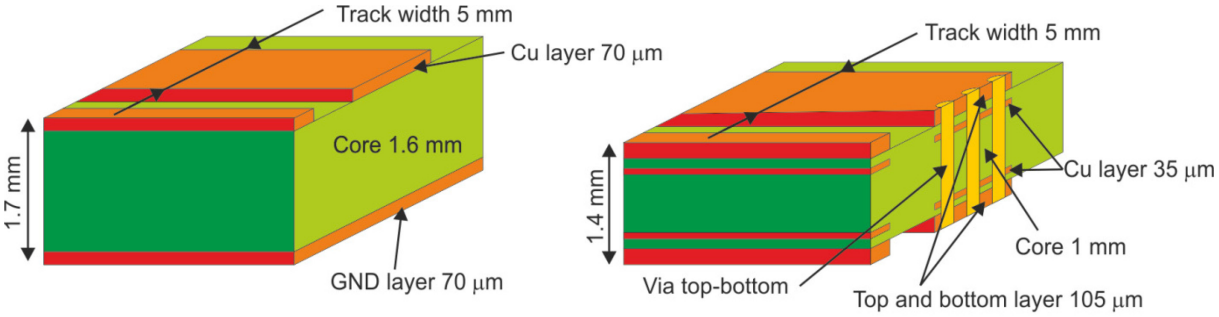

Fig. 18: Original (left) and final (right) PCB structure

Figure 19 shows the cross-section of the whole arrangement at the main heat source (the MOSFET switches) and its corresponding thermal model. The MOSFETs have cooling plates on top of them, onto which a heat sink is bolted. These cooling plates and the bottom layer of the PCB are electrically isolated by means of heat-transfer foil. The heat is transferred to the environment along three parallel paths: through the PCB and the aluminium bar, through the heat sink, and through the mounting bolt.

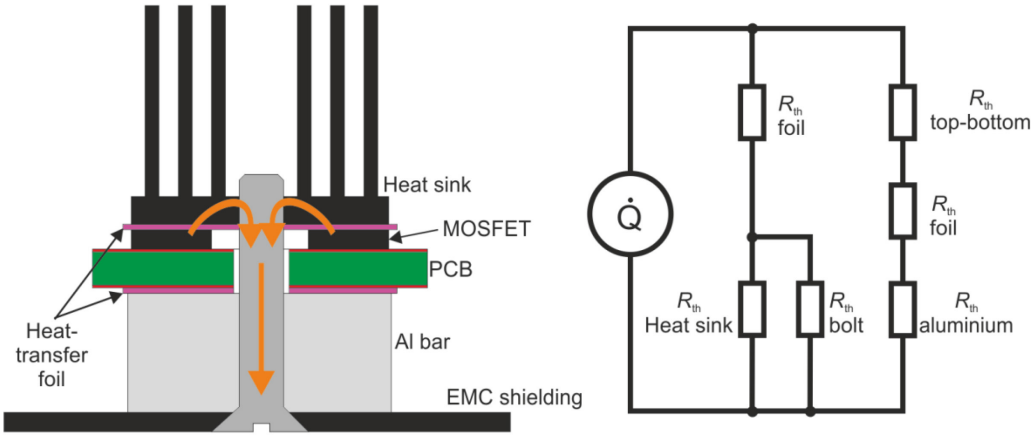

Fig. 19: PCB cross-section (left) and thermal model (right)

Figure 20 shows the bottom side of the final PCB. In total three aluminium bars transfer the heat to the EMC shielding. Between the aluminium bars and the Cu pads on the PCB there is an electrically isolating heat-transfer foil.

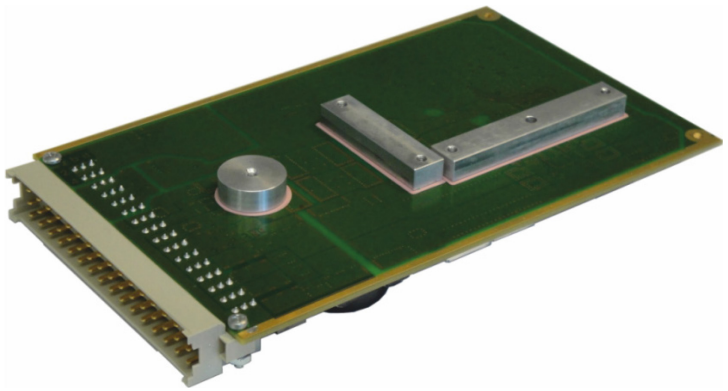

Fig. 20: Bottom side of the PCB

As seen in Fig. 16, there are several components that generate hot spots. Four components were exchanged in order to eliminate these hotspots. Figure 21 shows the location of these components on the PCB. Refer also to the thermal images in Figs. 16 and 22.

(1) the auxiliary d.c./d.c. converter 24 V/15 V in THT (through hole technology) in a plastic case was replaced by a SMD (surface mount device) type in a metallic case with better thermal behaviour;

(2) two chokes of 8.2 μH/13 A each were replaced by four chokes of 3.9 μH/12 A each, such that the heat source area could be enlarged;

(3) the linear auxiliary d.c./d.c. converter 15 V/5 V was replaced by a switched mode converter with much fewer losses;

(4) the 100 mW snubber resistors were replaced by 2 W types, which are larger and offer better heat transfer.

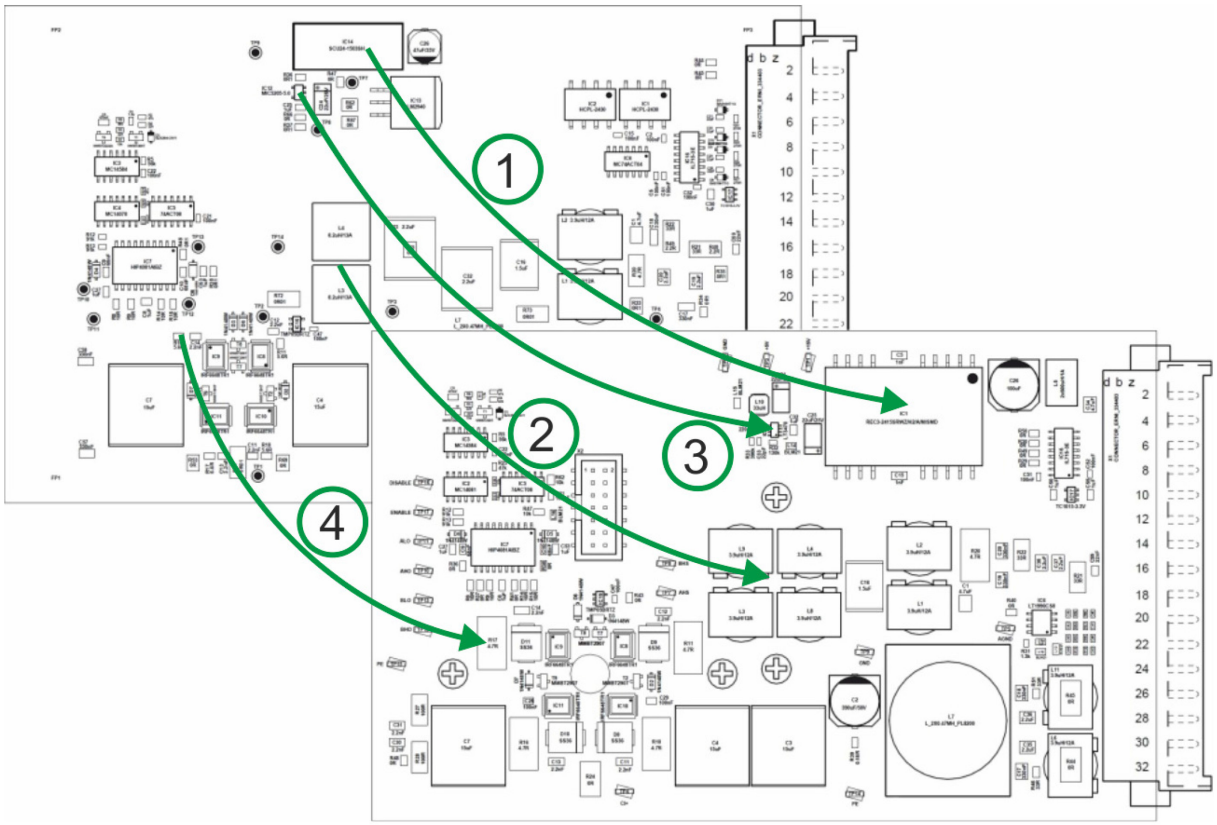

Fig. 21: Replacement of components that cause hotspots

Figure 22 shows the thermal image of the final design with the same temperature scaling as for Fig. 16. It shows a much more homogeneous temperature distribution. The majority of the power circuit is warmed to 50–65ºC, and the rest of the circuit stays at around ambient temperature. No extreme hotspots were observed. The measurements also showed a good correlation with the calculations.

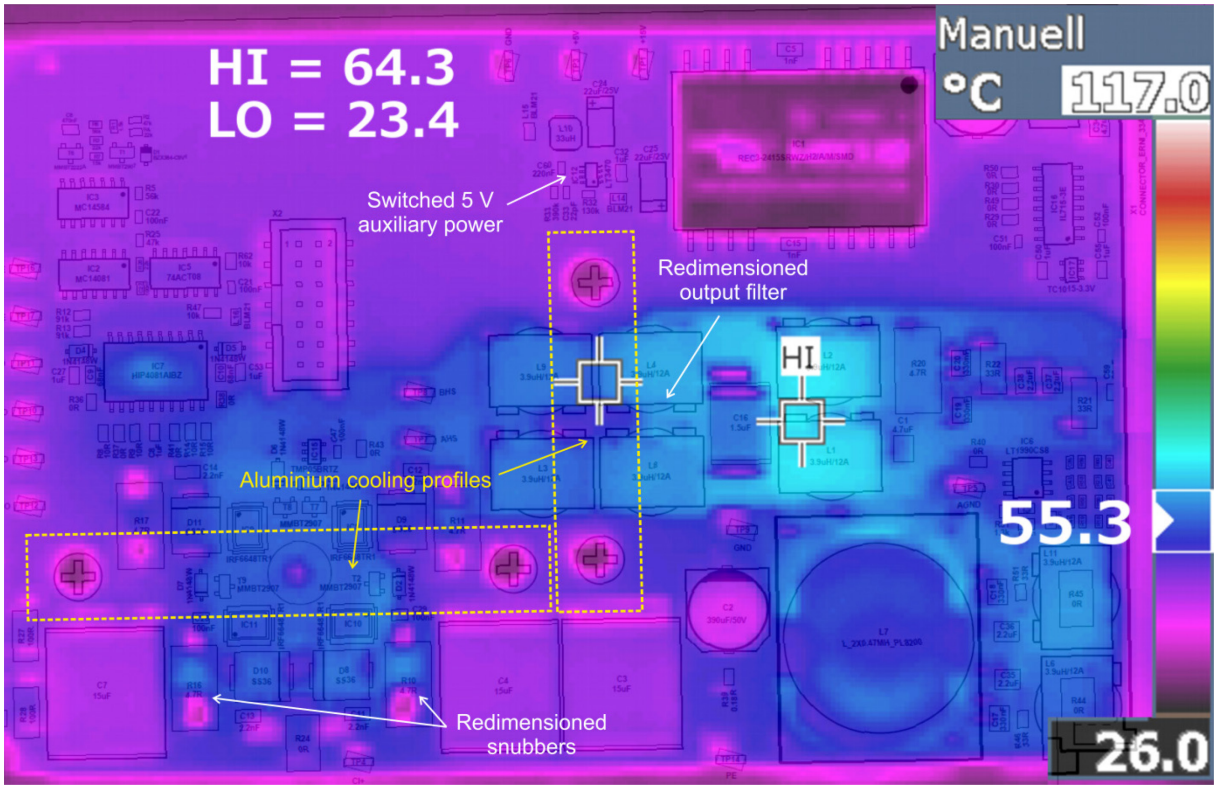

Fig. 22: Thermal image of the final design

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Regulation Theory

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Abstract
This paper reviews the design of regulation loops for power converters. Power converter control being a vast domain, it does not aim to be exhaustive. The objective is to give a rapid overview of the main synthesis methods in both continuous- and discrete-time domains.

Keywords
Power electronic converters; regulation loops design; digital control techniques; discrete-time model; Z-transforms; PID algorithm; RST algorithm.

1 Introduction

Power converters convert electric energy from one form to another which is optimally tailored for user loads. Therefore regulation is an important part of the design and construction of any power converter.

Owing to the fast development of digital electronics, power converter control uses more and more embedded computing systems like microcontrollers or Digital Signal Processors (DSPs). These devices replace progressively analogue controllers that have dominated the control of power electronics systems for many years.

After a period during which the discrete-time control laws were directly obtained from a discretization of the continuous-time control laws in order to ensure continuity with the existing methods and equipment, automation has refined its tools and methodologies: new approaches based on discrete-time models of the processes to be controlled have been proposed. With these new techniques, more powerful synthesis methods have been developed. Alternatives to the still widely used PID-type controllers have emerged, like RST controllers or more exotic ones such as dead-beat or fuzzy controllers. All these alternatives offer potential improvements in performance.

In the first part of this paper, the main concepts of continuous-time control are reviewed. Only the control of single-input single-output linear and time-invariant systems is addressed here. Digital control is presented in the second part. After a few reminders about Z-transforms, the concept of the discrete-time model is introduced. The main digital controller synthesis methods are then described and, depending on the chosen method, the choice of the sampling frequency is discussed.

2 Continuous-time control

2.1 Memory refreshing

To design a controller that makes a system behave in a specific desirable manner, we need a way to predict its behaviour over time, specifically how its outputs will change in response to any applied inputs. Thus a mathematical description (‘model’) of the system to be controlled (also called the ‘plant’) is needed.

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If the plant is a single-input single-output linear and time-invariant system (time-invariant systems are systems whose characteristics do not change with time), then its input $u(t)$ and output $y(t)$ are related by the following differential equation with constant coefficients:

$$a_n \cdot \frac{\mathrm{d}^n}{\mathrm{d}t^n} y + \ldots + a_1 \cdot \frac{\mathrm{d}}{\mathrm{d}t} y + a_0 \cdot y = b_m \cdot \frac{\mathrm{d}^m}{\mathrm{d}t^m} u + \ldots + b_1 \cdot \frac{\mathrm{d}}{\mathrm{d}t} u + b_0 \cdot u \qquad (m \le n), \tag{1}$$

n being the order of the system.

In the frequency domain, transfer functions are obtained from time-domain descriptions via Laplace transform. Assuming zero initial conditions, Eq. (1) leads to the following *system transfer function* $H(s)$:

$$H(s) = \frac{Y(s)}{U(s)} = \frac{\sum_{i=0}^{m} b_i \cdot s^i}{\sum_{j=0}^{n} a_i \cdot s^j}, \tag{2}$$

where s is the Laplace operator.

Some basic but important definitions are recalled:

- The *poles* are the roots of the denominator polynomial of the system transfer function $H(s)$. The *zeros* are the roots of the numerator polynomial.
- The system stability is determined by the location of the poles. If their real part is strictly negative, then the system is stable.
- If the transfer function behaves like K/s^{α} for $s \to 0$, then α is called the *system class*. The static gain is obtained for s equal to zero.
- If there is a period of time during which the output does not react to the input, the system is defined as a system with delay. The transfer function $H_{\mathrm{d}}(s)$ of a system having a time delay of $t0$ can be expressed as

$$H_{\mathrm{d}}(s) = H(s) \cdot \mathrm{e}^{-s \cdot t0} \tag{3}$$

where $H(s)$ is the transfer function of the system without delay.

2.2 Importance of feedback control

Feedback is a very powerful mechanism. Why is it necessary? An intuitive strategy would be to use a feedforward controller and to make the product of the plant and this feedforward controller unity, hence to find a controller that equals the plant inverse ($C = H^{-1}$ in Fig. 1, assuming a unit gain for the actuator transfer function). Then in theory the system output Y would be equal to the controller input *Yref*.

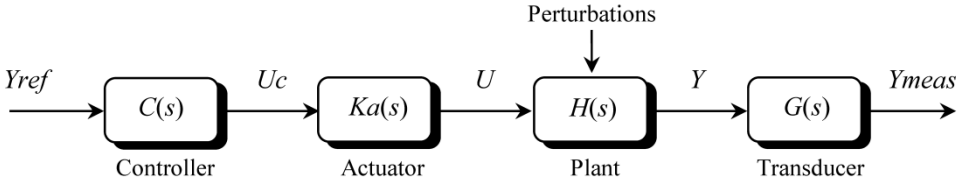

Fig. 1: Open-loop control configuration

This works well as long as the feedforward controller approximates the plant inverse sufficiently well. In practice, uncertainties and unmodelled dynamics make this impossible. To fulfil

the requirements, a feedback correction is necessary to guarantee performance, even with model uncertainties, to reduce sensitivity to parameter variations, to reject disturbances, and obviously to stabilize unstable open-loop systems. Thus a typical control structure combines feedback and feedforward controls (see Fig. 2). The feedback controller guards robust stability and improves static and dynamic precision whereas the feedforward controller improves tracking behaviour (via compensation of the input) or regulation behaviour (via compensation of the perturbations).

It is important to understand that the performance requirements (static, dynamic behaviour, stability, and robustness) of the closed loop translate into constraints on the compensated system in open loop. We will see later in this paper how to make use of the open-loop frequency response to design controllers.

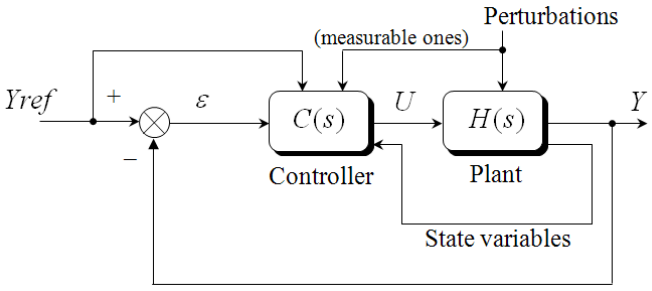

Fig. 2: Typical control structure

The typical control structure for current regulated power supplies is represented in Fig. 3. This so-called 'cascade' structure is based on a nested connection of a fast inner voltage loop and a slower outer current loop. The fast inner voltage loop acts as an active filter to reject the output voltage ripple and the output voltage fluctuations due to float of input mains, and it also simplifies the design of the current loop. The outer current loop ensures the overall stability of the power supply and it provides an inherent overvoltage protection.

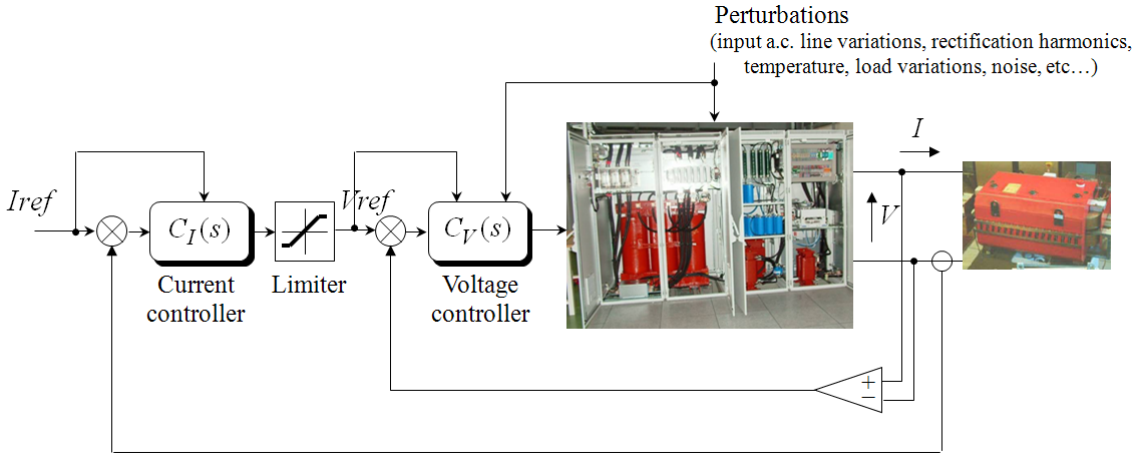

Fig. 3: Cascade control structure

2.3 Analysis of closed-loop systems

2.3.1 Definition of open-loop and closed-loop transfer functions

In this section, we focus on the closed-loop system shown in Fig. 4. To study it, we use the open-loop transfer function obtained by breaking the feedback loop, the expression for which is given by

$$OL(s) = \frac{Ymeas(s)}{\varepsilon(s)} = C(s) \cdot H(s) \cdot G(s) . \tag{4}$$

The open-loop bandwidth is defined as the interval of angular frequencies for which the open-loop gain $|C(jw) \cdot H(jw) \cdot G(jw)|$ is higher than unity.

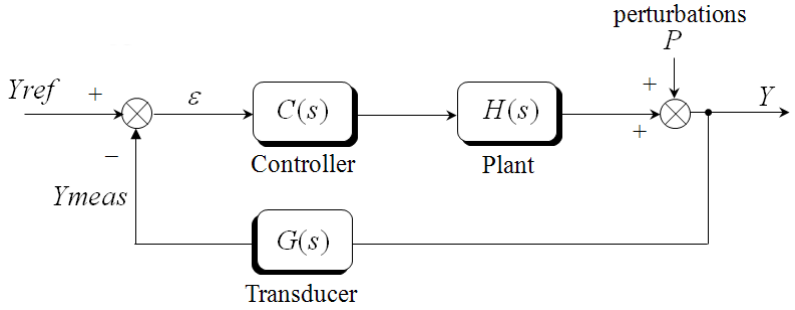

Fig. 4: Closed-loop system

The closed-loop transfer function is

$$CL(s) = \frac{Y(s)}{Yref(s)} = \frac{C(s) \cdot H(s)}{1 + C(s) \cdot H(s) \cdot G(s)} . \tag{5}$$

The transfer functions of the error versus input and perturbation can be calculated as

$$\frac{\varepsilon_{Yref}(s)}{Yref(s)} = \frac{1}{1 + C(s) \cdot H(s) \cdot G(s)} \qquad \varepsilon(s) = \varepsilon_{Yref}(s) + \varepsilon_P(s) . \tag{6}$$

$$\frac{\varepsilon_P(s)}{P(s)} = -\frac{G(s)}{1 + C(s) \cdot H(s) \cdot G(s)}$$

2.3.2 Precision of closed-loop systems

2.3.2.1 Static error

In steady state, the error versus the input can be derived from Eq. (6). Using the 'final value' theorem, we have

$$\lim_{t \to \infty} \varepsilon_{Yref}(t) = \lim_{s \to 0} s \cdot \varepsilon_{Yref}(s) = \lim_{s \to 0} \frac{s}{1 + C(s) \cdot H(s) \cdot G(s)} \cdot Yref(s) . \tag{7}$$

- For a step input ($Yref(s) = K/s$), the error cancels if there is at least one integrator in the open-loop transfer function.
- For a ramp input ($Yref(s) = K/s^2$), two integrators are needed to achieve zero steady-state error.
- For a sinusoidal input $K \cdot \sin(w_0 \cdot t)$, at steady state, the error is a harmonic signal which module $|\varepsilon_{Yref}|$ is such that $\frac{|\varepsilon_{Yref}|}{K} = \left| \frac{1}{1 + C(s) \cdot H(s) \cdot G(s)} \right|_{s = jw_0}$.

So if w_0 is inside the open-loop bandwidth, the error amplitude is inversely proportional to the open-loop gain at w_0: $\frac{|\varepsilon_{Yref}|}{K} \approx \left| \frac{1}{C(s) \cdot H(s) \cdot G(s)} \right|_{s = jw_0}$.

Regarding perturbation rejection, using Eq. (6), we have

$$\lim_{t\to\infty}\varepsilon_P(t)=\lim_{s\to 0}s\cdot\varepsilon_P(s)=\lim_{s\to 0}\frac{-s\cdot G(s)}{1+C(s)\cdot H(s)\cdot G(s)}\cdot P(s)\,. \tag{8}$$

To have a perfect rejection, the open loop must contain the classes of the perturbations. Thus to reject disturbances of class N, at least N integrators are needed in the open-loop transfer function.

2.3.2.2 Dynamic error

Let us assume that the velocity v and the acceleration γ of the input are limited. The input signal is then defined by the following constraints: $v<v_{\max}$, $\gamma<\gamma_{\max}$.

Maintaining the dynamic error ε_{d} below a given limit $\varepsilon_{\mathrm{d}_{\max}}$ results in a specification of a minimum open-loop gain in a certain frequency range:

$$\varepsilon_{\mathrm{d}}<\varepsilon_{\mathrm{d}_{\max}} \qquad \Rightarrow \qquad \left|OL(s)\right|_{s=j\frac{\gamma_{\max}}{v_{\max}}}>\frac{v_{\max}^{\ 2}}{\gamma_{\max}\cdot\varepsilon_{\mathrm{d}_{\max}}}\,. \tag{9}$$

In general, this constraint results in imposing a finite open-loop bandwidth.

2.3.3 Stability and robustness of closed-loop systems

A closed-loop system is stable if the poles of its transfer function have a negative real part.

The stability of a feedback system can also be determined through the simple knowledge of the open-loop frequency response, using the 'Nyquist criterion'. This is of great practical importance for controller design as it easily demonstrates how to modify the controller to make an unstable system stable. The closed-loop system is stable if the critical point –1 is on the left-hand side of the open-loop Nyquist curve, for w increasing. Two quantitative measures are commonly used to determine how stable (robust) the system is. The *phase margin* is the amount of phase lag required to reach the stability limit. The *gain margin*, similarly, states how much the controller gain can be increased before reaching the stability limit.

Phase margin:

$$\Phi_{\mathrm{M}}=180^\circ+\arg\left[OL\left(j\cdot w_{\mathrm{cr}}\right)\right], \tag{10}$$

where w_{cr} is such that $\left|OL\left(j\cdot w_{\mathrm{cr}}\right)\right|=1$.

Gain margin: $\mathrm{G_M}=\dfrac{1}{\left|OL\left(j\cdot w_{\pi}\right)\right|}$, (11)

where w_{π} is such that $\arg\left[OL\left(j\cdot w_{\pi}\right)\right]=-180^\circ$.

Typically, $30^\circ<\Phi_{\mathrm{M}}<60^\circ$, $\mathrm{G_M}>6$ dB.

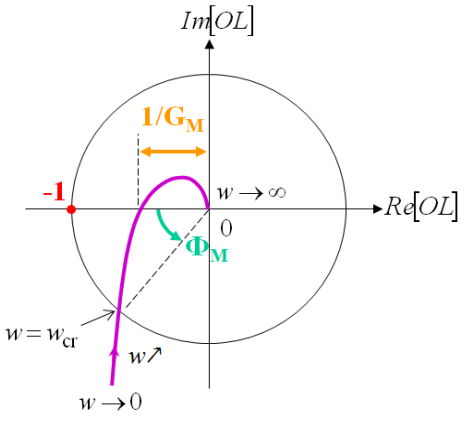

Fig. 5: Closed-loop system stability

There is an obvious contradiction between precision and stability specifications. Thus the controller design will be the result of a trade-off.

2.3.4 *Influence of the poles on the transient behaviour*

The contribution of real and complex poles on the transient behaviour of a system is represented in the complex plane in Fig. 6. An important observation is that the most distant poles to the left yield a faster transient regime. So the poles closest to the imaginary axis are the ones that tend to dominate the response since their contribution takes a longer time to die out. These poles are called *dominant poles* if the ratio of their real part to that of any other poles is typically lower than 1/5. A transfer function can be simplified by keeping only the dominant poles (and the static gain unchanged). This makes control loop analysis and design easier. Also, lower-order controllers can be obtained.

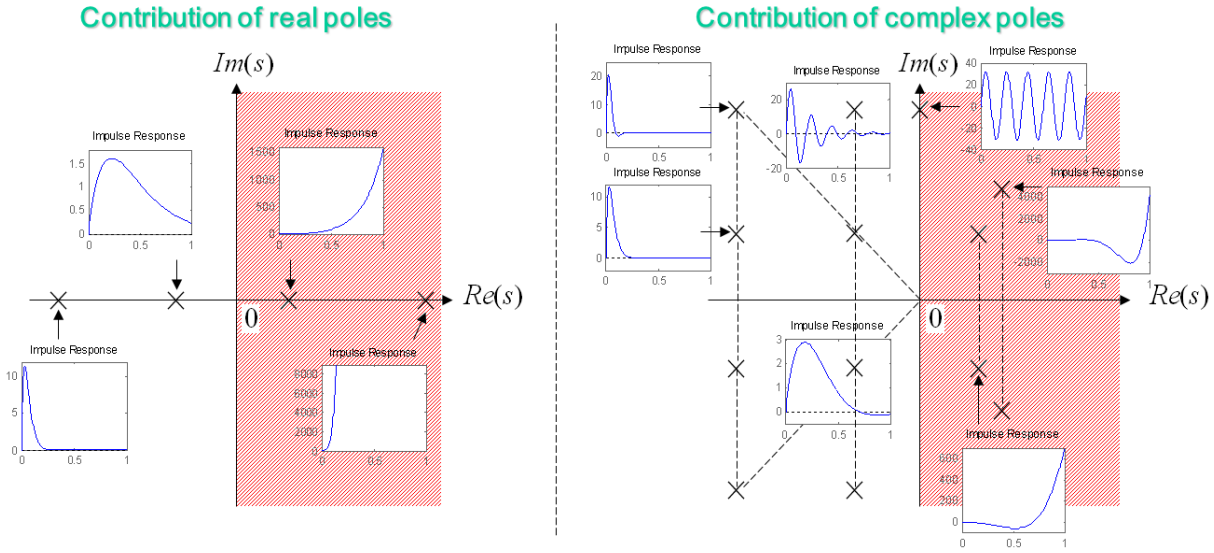

Fig. 6: Influence of the poles on the system transient behaviour

2.3.5 *Particular case: second-order systems with complex conjugate poles*

The search for a good compromise between speed and stability generally leads to the choice of a first- or second-order behaviour for the closed loop. For second-order system behaviour, the design specifications imply constraints on the *cut-off frequency* w_n and the *damping ratio* ζ of the targeted transfer function Eq. (12). Figure 7 shows the parameters usually used to characterize the step response, and Eqs. (13)–(15) link cut-off frequency and damping ratio to these parameters.

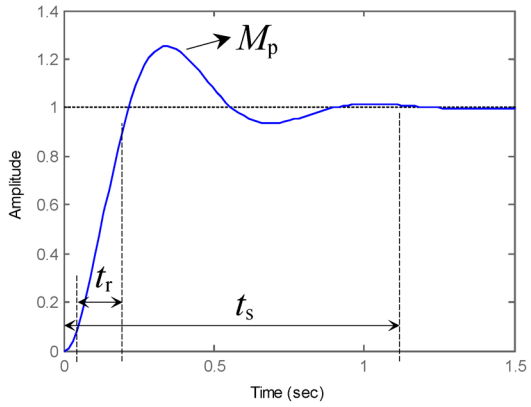

Fig. 7: Step input response

Targeted closed-loop transfer function:

$$CL_{\text{des}}(s) = \frac{w_n^2}{s^2 + 2\cdot\zeta\cdot w_n\cdot s + w_n^2}\ ; \qquad (12)$$

Rise time (10% → 90%):

$$t_r \approx (2.6\cdot\zeta^2 - 0.45\cdot\zeta + 1.2)/w_n\ ; \qquad (13)$$

Peak overshoot: $M_p = e^{-\pi\cdot\zeta/\sqrt{1-\zeta^2}}$; (14)

Settling time (to 1%): $t_s \approx 4.6/\zeta\cdot w_n$. (15)

2.3.6 *Influence of a zero on the system behaviour*

In the case of a second-order system, the corresponding transfer function is

$$CL(s) = K \cdot (s + z_0) / (s - p_1) \cdot (s - \overline{p_1}), \tag{16}$$

where z_0 is assumed to be a strictly negative real number.

So the unit step response of this system can be written as

$$Y(s) = \frac{K}{s} \cdot \frac{s + z_0}{(s - p_1) \cdot (s - \overline{p_1})} = \frac{K \cdot z_0}{s \cdot (s - p_1) \cdot (s - \overline{p_1})} + \frac{K}{(s - p_1) \cdot (s - \overline{p_1})}, \tag{17}$$

which gives in the time domain

$$y(t) = y_{\text{2nd order}}(t) + \frac{1}{z_0} \cdot \frac{d}{dt} y_{\text{2nd order}}(t), \tag{18}$$

where $y_{\text{2nd order}}(t)$ is the step response of the system Eq. (16) without zeros.

The second term of Eq. (18) reveals that the additional zero makes the system faster and more oscillatory, and all the more so as its value is close to zero. So special care should be taken to design appropriate zeros in a closed-loop transfer function.

2.4 Continuous-time controller synthesis

2.4.1 Controller design process

In the design of a controller, the first step is to get the dynamic model of the system to be controlled. The principal difficulty in modelling power converters is that they are inherently non-linear and present several distinct electric configurations during a switching period. By constructing equivalent averaged circuit models, large-signal average models of the power converter can be determined. Then linearization about a quiescent operating point may be necessary to obtain linear small-signal transfer functions [1–4]. To elaborate power converter models, an identification processes from experimental data can also be used.

Once the model is known, the specifications of the desired closed-loop performance have to be defined. As explained in the preceding section, the choice of these specifications results from a trade-off between speed and robustness. This choice is obviously linked to the plant dynamics but also to the power availability of the power converter during the transient: the acceleration of the plant natural response requires control peaks that are greater than the steady-state values. If the control variable comes to saturation, the feedback loop is broken and the actuator remains at its limit independently of the plant output. To prevent actuator saturation, the closed-loop performance has to be chosen accordingly.

The last step is to choose the controller type and its design method.

2.4.2 Proportional-integral-derivative (PID) controller

2.4.2.1 Introducing PID control

The PID controller is by far the most dominant form of feedback in use today [5–7], especially for analogue control. PID feedback is simple and intuitive: it involves only three separate constant parameters to tune the control loop. As shown in Eqs. (19) and (20), it is based on the past control error (integral term), the present control error (proportional term), and the future control error (derivative term). Many controllers (PI) do not even use derivative action. This kind of controller is well suited for systems exhibiting dominant first- or second-order behaviour, for which the desired performance of the closed-loop as compared to the open-loop response of the system is not too demanding.

PID algorithm: $$u(t) = K_{\mathrm{p}} \cdot \varepsilon(t) + K_{\mathrm{i}} \int_0^t \varepsilon(t) + K_{\mathrm{d}} \cdot \frac{\mathrm{d}}{\mathrm{d}t} \varepsilon(t)\,; \tag{19}$$

Controller transfer function: $$C_{\mathrm{PID}}(s) = K_{\mathrm{p}} + \frac{K_{\mathrm{i}}}{s} + \frac{K_{\mathrm{d}} \cdot s}{1 + \frac{K_{\mathrm{d}}}{N \cdot K_{\mathrm{p}}} \cdot s}, \quad 10 \le N_{\mathrm{typ.}} \le 20\,. \tag{20}$$

As a pure derivative amplifies noise, the transfer function standard form includes a low-pass filter on the derivative term.

A number of alternative approaches for PID tuning are available, including the following ones:

- heuristic tuning procedures: Ziegler–Nichols, Cohen–Coon, etc.,
- graphical methods: loop shaping, root locus, etc.,
- pole placement,
- minimization of integral type criterion.

2.4.2.2 Putting it into practice

Let us focus on two design methods—loop shaping and pole placement—in the following example where controllers have to be designed for the current and voltage control loops of a Buck converter feeding an inductive (R-L) load.

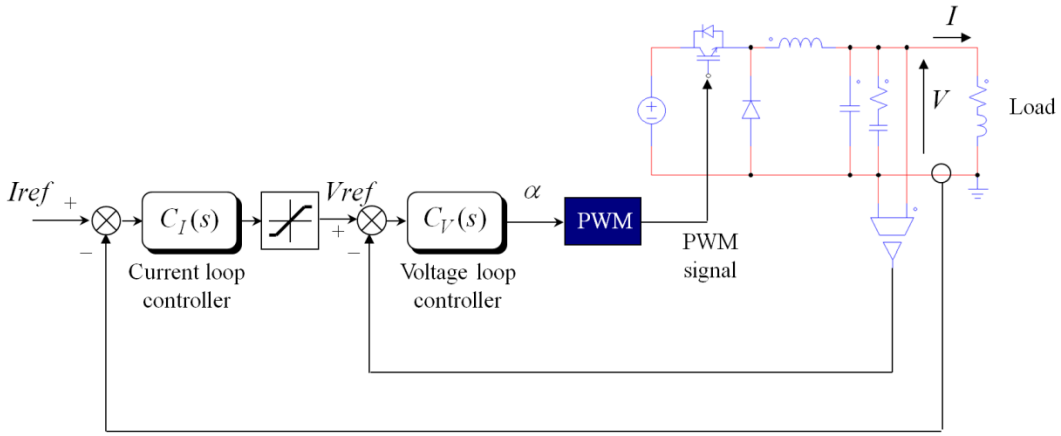

Fig. 8: Control of a Buck converter

Loop shaping is one of the most elementary methods used to design classical controllers such as PIDs. The controller is determined by manipulating (shaping) the open-loop frequency response, such that it meets the design specifications.

Let us assume the following specifications for the voltage loop:

- zero static error,
- dynamic precision, i.e., open-loop gain higher than 40 dB up to w_0,
- bandwidth $\{0, w_c\}$,
- phase margin Φ_M greater than 50°.

The plant model does not have a pole at $s = 0$ (integrator): it is necessary that the controller contains an integral action to cancel the static error. So a PI controller is first tried for $C_V(s)$. Its parameters are adjusted to meet the open-loop gain constraints, as shown on the Bode plot in Fig. 9.

However, with this setting the phase margin requirement cannot be reached. A derivative action is then added to correct the phase margin and meet the stability requirement.

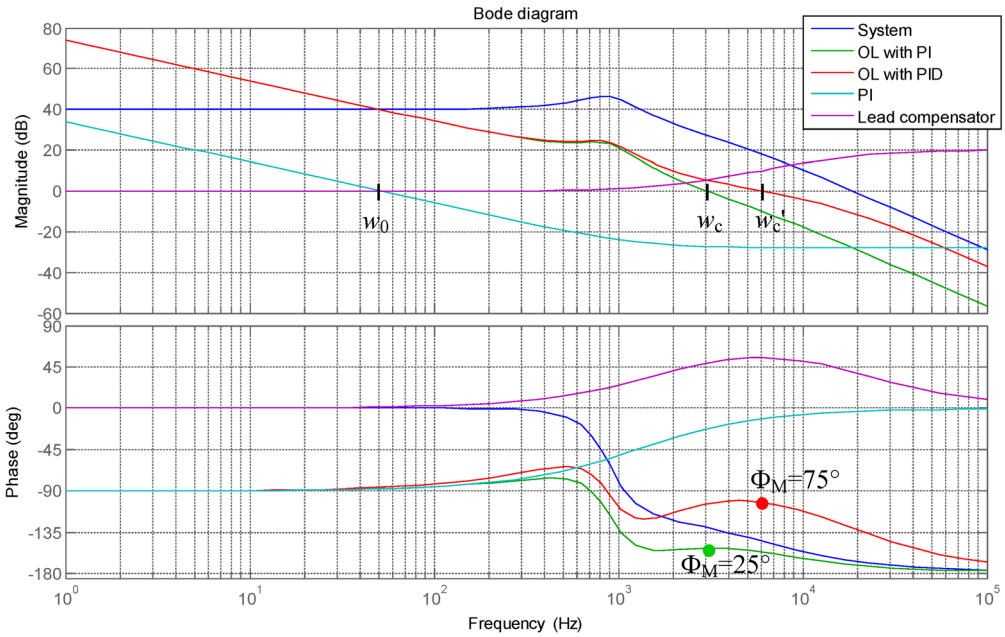

Fig. 9: PID tuning using the loop shaping method

Pole placement is used in the following to design a PI controller for the current loop. This method consists of placing the closed-loop poles at the desired positions by calculating the controller parameters such that this condition is fulfilled.

The open-loop transfer function is

$$OL_I(s) = C_I(s) \cdot CL_V(s) \cdot \frac{b_0}{1 + a_1 \cdot s}, \qquad b_0 = 1/R_{\text{load}}, \quad a_1 = L_{\text{load}}/R_{\text{load}}, \tag{21}$$

where $CL_V(s)$ is the closed voltage loop transfer function.

If the current loop bandwidth is low compared to the voltage loop bandwidth, Eq. (21) can be simplified as follows:

$$OL_I(s) \approx k_{\text{p}} \cdot \left(1 + \frac{k_{\text{i}}}{s}\right) \cdot \frac{b_0}{1 + a_1 \cdot s}. \tag{22}$$

The system pole can be cancelled by setting $k_{\text{i}} = 1/a_1$. The closed-loop transfer function then shrinks down to a first-order transfer function:

$$CL_I(s) = \frac{1}{1 + (a_1/k_{\text{p}} \cdot b_0) \cdot s}. \tag{23}$$

To make the closed-loop behave like a first-order system with a rise time equal to t_{r}, the closed-loop pole has to be placed at $-w_n$, where $w_n = 2.2 / t_{\text{r}}$. This results in the following choice for the parameter k_{p}:

$$k_{\text{p}} = a_1 \cdot w_n / b_0 . \tag{24}$$

The pole cancellation technique requires a good knowledge of the process: if a_1 is likely to vary ($L_{\text{load}} = f(I)$), this method can bring about poor results (especially when the pole is close to the origin). In that case, system pole cancellation should be avoided. The closed loop transfer function is then of second order. The PI parameters can be computed by identifying the coefficients of the closed-loop transfer function denominator with those of the polynomial $s^2/w_n^2 + (2\cdot\zeta/w_n)\cdot s + 1$, where w_n is the desired cut-off frequency (which can be related via Eqs. (13) and (15) to rise time and settling time) and ζ is the damping ratio (which has to be chosen greater than 1 for aperiodic behaviour). We obtain

$$k_{\text{p}} = (a_1 \cdot 2 \cdot \zeta \cdot w_n - 1)/b_0 \,, \qquad k_{\text{i}} = a_1 \cdot w_n^2/(k_{\text{p}} \cdot b_0) \,. \tag{25}$$

This controller setting, however, gives rise to a zero $-k_{\text{i}}$ in the closed-loop transfer function, which may affect the transient response (see Section 2.3.6). A solution to this issue is to cancel this zero by filtering the reference, as shown in Fig. 10.

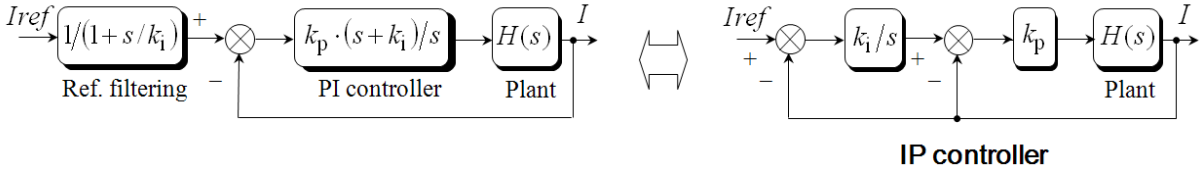

Fig. 10: Reference filtering

Another issue is the so-called *integral windup phenomenon*: when the output of either the current or the voltage controller saturates, the integral term of the controller increases and may become very large. At the end of the saturated mode of operation, a negative error is needed to remove the accumulated positive error, which may give large transients. Many anti-windup methods have been proposed [8–10]. A simple way to implement anti-windup is to switch off the integrator (by zeroing its input) in case of control output saturation. Other schemes, like the one represented in Fig. 11, enable the integral part of the controller to be dynamically saturated.

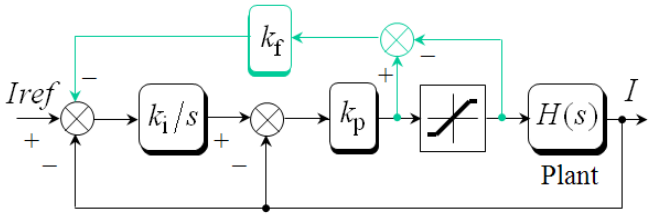

Fig. 11: Example of anti-windup solution

3 Discrete-time control

The development of digital technology over the past two decades along with increased performance demands have led to a growing use of digital control in power converters [11, 12]. The benefits of using digital over analogue control are numerous: performance enhancement (as digital control allows more complex regulation schemes), improved flexibility, system monitoring and archiving capabilities, better noise immunity, to name a few. One major issue is the delay introduced with a digital controller. Other issues, such as aliasing, quantization errors, or limit cycling, may also affect the system operation [13, 14].

3.1 Introducing the Z-transform

The Z-transform is the discrete-time counterpart of the Laplace transform. It is an essential tool for the analysis and design of discrete-time systems. Let us consider a sequence $x(k)$ of sampled signals, where $x(k)$ takes the value of the analogue signal $x(t)$ at the kth sampling instant (the sampling period Ts is assumed constant). The Z-transform of this sequence is defined as

$$X(z) = \sum_{k=0}^{+\infty} x(k) \cdot z^{-k}, \tag{26}$$

where z is a complex variable which is related to the Laplace operator by $z = \mathrm{e}^{s \cdot Ts}$.

From the Laplace time-shifting property, we know that $\mathrm{e}^{-s \cdot Ts}$ is the time delay by Ts seconds. Therefore $z^{-1} = \mathrm{e}^{-s \cdot Ts}$ corresponds to a unit sample period delay. The main properties of Z-transforms are listed below:

- linearity:

$$\mathrm{Z}\left[\lambda \cdot x(k) + \mu \cdot y(k)\right] = \lambda \cdot X(z) + \mu \cdot Y(z), \tag{27}$$

- shifting property:

$$\mathrm{Z}\left[x(k-n)\right] = z^{-n} \cdot X(z), \tag{28}$$

- convolution:

$$\mathrm{Z}\left[x(k) * y(k)\right] = \mathrm{Z}\left[\sum_{n=-\infty}^{n=+\infty} x(n) \cdot y(k-n)\right] = X(z) \cdot Y(z), \tag{29}$$

- final value:

$$\lim_{k \to \infty} x(k) = \lim_{z \to 1} (z-1) \cdot X(z). \tag{30}$$

Some examples of Z-transforms:

- discrete impulse: $X(z) = 1$,
- discrete step: $X(z) = \dfrac{1}{1 - z^{-1}}, \quad |z| > 1$,
- discrete ramp: $X(z) = \dfrac{z^{-1}}{\left(1 - z^{-1}\right)^2}, \quad |z| > 1$.

Tables of commonly encountered *Z*-transforms can be found in the literature (see the references).

3.2 Relation between Laplace transforms and Z-transforms

Let $x(t)$ be a causal continuous-time signal whose Laplace transform is $X(s)$, and let $x(k)$ be the discrete-time signal obtained by sampling $x(t)$ at a uniform rate $1/Ts$.

3.2.1 Case of signals having only simple poles

If $X(s)$ has only simple poles, it takes the following form:

$$X(s) = \sum_{i=1}^{N} \frac{A_i}{s - s_i}. \tag{31}$$

The expression of the corresponding Z-transform is

$$X(z) = \sum_{i=1}^{N} \frac{A_i}{1 - e^{s_i \cdot Ts} \cdot z^{-1}} . \tag{32}$$

Thus, a pole $s_i = \sigma_i + j \cdot w_i$ in $X(s)$ gives rise to a pole $z_i = e^{s_i \cdot Ts} = e^{\sigma_i \cdot Ts} \cdot e^{j \cdot w_i \cdot Ts}$ in $X(z)$.

This relation enables one to establish the correspondence between the pole location in the s-domain and that in the z-domain.

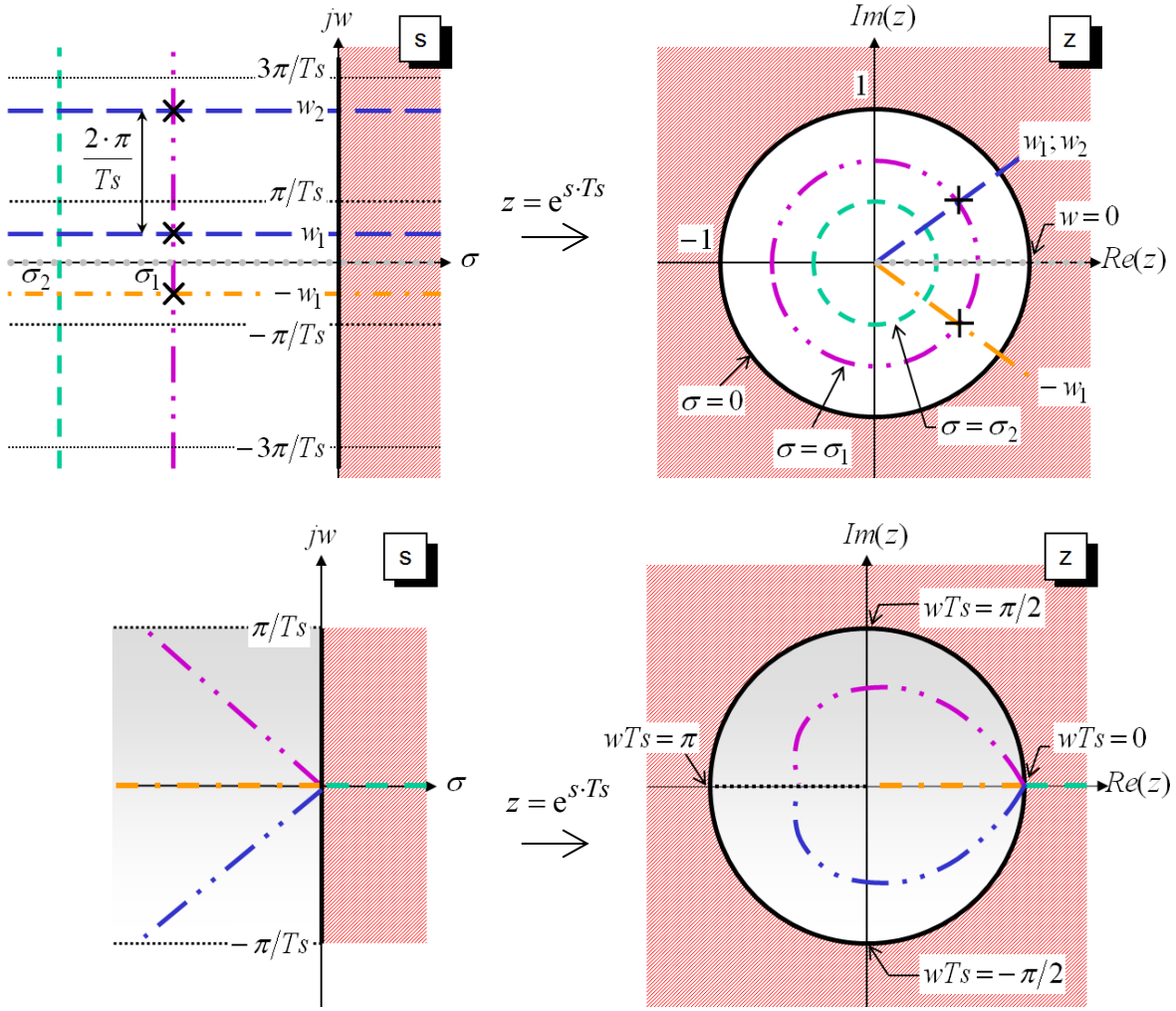

Fig. 12: Mapping of the *s*-plane to the *z*-plane

- The portion of the *s*-plane to the left of the imaginary axis maps to the inside of the unit circle in the *z*-plane, and the imaginary axis maps to the unit circle. So the stability region in the s-plane $\{ \sigma_i < 0 \}$ maps to $\{ |z_i| < 1 \}$.
- Lines of constant frequency in the *s*-plane become radial lines in the *z*-plane. The negative real axis in the *s*-plane maps to the interval 0 to 1 in the *z*-plane.
- Lines of constant real part map to circles centred at the origin.
- The lines of constant damping ratio in the *s*-plane become logarithmic spirals in the *z*-plane.

An important observation is that poles in the *s*-plane whose imaginary parts differ by a multiple of $2 \cdot \pi / Ts$ belong to the same locations in the *z*-plane: the unit disc can only represent signals of frequency up to the half the sampling frequency (the Nyquist frequency). The condition which has to be satisfied so that two different poles in the *s*-plane do not correspond to the same point in the *z*-plane is

$$Ts < \pi / \max_i |w_i| . \tag{33}$$

3.2.2 General case

In the general case, the relation between $X(s)$ and $X(z)$ is given by

$$X(z) = \sum_{s_i = \text{poles of } X(s)} \text{Residues} \left\{ X(s) \cdot \frac{1}{1 - \mathrm{e}^{s \cdot Ts} \cdot z^{-1}} \right\}_{s = s_i} . \tag{34}$$

The residue at s_j, a pole of multiplicity *m*, can be calculated as follows:

$$\text{Residue} \left\{ X(s) \cdot \frac{1}{1 - \mathrm{e}^{s \cdot Ts} \cdot z^{-1}} \right\}_{s = s_j} = \frac{1}{(m-1)!} \cdot \lim_{s \to s_j} \frac{\mathrm{d}^{m-1}}{\mathrm{d}s^{m-1}} \left[(s - s_j)^m \cdot X(s) \cdot \frac{1}{1 - \mathrm{e}^{s \cdot Ts} \cdot z^{-1}} \right] . \tag{35}$$

3.3 Modelling of digitally controlled continuous-time systems

Let us focus on the physical process represented in Fig. 13, which is digitally controlled at the period *Ts*, and whose output is sampled at the same period. The structure of this hybrid system consists of a sampler (the analog-to-digital converter, or ADC), a digital controller, the continuous-time process, and a so-called hold-device (here assumed to be a digital-to-analog converter, or DAC). The sampler is preceded by an anti-aliasing filter (not represented in Fig. 13), which should preferably be taken into account for modelling.

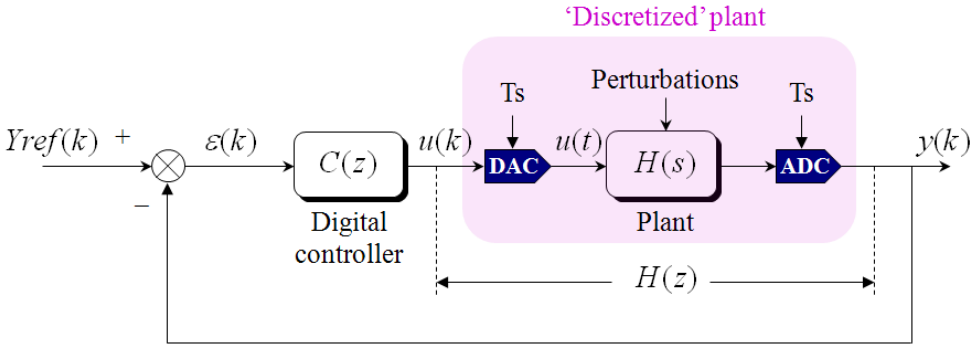

Fig. 13: Digitally controlled plant

The DAC converts $u(k)$ to $u(t)$ by holding each sample value for one sampling interval (zero-order hold operation). Hence it introduces a delay equal to *Ts*/2. The transfer function of a zero-order hold is

$$H_{\text{ZOH}}(s) = \frac{1 - \mathrm{e}^{-s \cdot Ts}}{s} . \tag{36}$$

From an external point of view, the set {zero-order hold + plant + sampler} is a discrete system, whose transfer function can be derived from the plant transfer function according to

$$H(z) = (1 - z^{-1}) \cdot \mathrm{Z} \left[\frac{H(s)}{s} \right] . \tag{37}$$

It is interesting to note that if $H(s)$ has poles $s = s_i$, then the transfer function $H(z)$ of the 'discretized' system has poles $z = e^{s_i \cdot Ts}$. But the zeros are unrelated. Let us define

$$Y(z) = Z[y(k)] \quad ; \quad Yref(z) = Z[Yref(k)] \quad ; \quad E(z) = Z[\varepsilon(k)] \quad ; \quad U(z) = Z[u(k)].$$

The open-loop transfer function is then

$$OL(z) = \frac{Y(z)}{E(z)} = C(z) \cdot H(z) \tag{38}$$

and the closed-loop transfer function is

$$\frac{Y(z)}{Yref(z)} = \frac{C(z) \cdot H(z)}{1 + C(z) \cdot H(z)}. \tag{39}$$

The use of the operator z^{-1} is often preferred as it refers to the past and not the future. The transfer function of the digital controller can then be written as

$$C(z) = \frac{U(z)}{E(z)} = \frac{b_0 + b_1 \cdot z^{-1} + ... + b_p \cdot z^{-p}}{1 + a_1 \cdot z^{-1} + ... + a_n \cdot z^{-n}}. \tag{40}$$

Hence,

$$(1 + a_1 \cdot z^{-1} + ... + a_n \cdot z^{-n}) \cdot U(z) = (b_0 + b_1 \cdot z^{-1} + ... + b_p \cdot z^{-p}) \cdot E(z). \tag{41}$$

Using the Z-transform shifting property, Eq. (28), the following difference equation is obtained, where the present output is dependent on the present input and the past inputs and outputs:

$$u(k) = b_0 \cdot \varepsilon(k) + b_1 \cdot \varepsilon(k-1) + ... + b_p \cdot \varepsilon(k-p) - a_1 \cdot u(k-1) - ... - a_n \cdot u(k-n). \tag{42}$$

This is the controller algorithm.

3.4 Analysis of closed-loop discrete systems

3.4.1 Stability and robustness of closed-loop discrete systems

As seen in Section 3.2, a discrete system is stable if all the poles of its transfer function have a modulus strictly inferior to 1. So the closed-loop discrete system Eq. (39) is stable if all the roots of the characteristic equation $1 + C(z) \cdot H(z) = 0$ have a modulus strictly inferior to 1. The stability margins are defined as:

Phase margin:

$$\Phi_M = 180° + \arg\left[OL(e^{j \cdot w_{cr} \cdot Ts})\right], \tag{43}$$

where w_{cr} is such that $\left|OL(e^{j \cdot w_{cr} \cdot Ts})\right| = 1$.

Gain margin:

$$G_M = \frac{1}{\left|OL(e^{j \cdot w_\pi \cdot Ts})\right|}, \tag{44}$$

where w_π is such that

$$\arg\left[OL(e^{j \cdot w_\pi \cdot Ts})\right] = -180°.$$

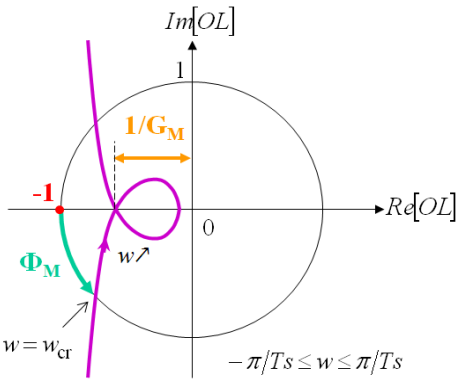

Fig. 14: Closed-loop discrete system stability

3.4.2 *Influence of the poles on the system behaviour*

The influence of the system poles on its transient behaviour is summarized in Fig. 15. Two interesting remarks are as follows:

- poles closer to the origin lead to a faster transient regime;
- the impulse response caused by poles having negative real part cycles back and forth between positive and negative deviations from the steady-state value.

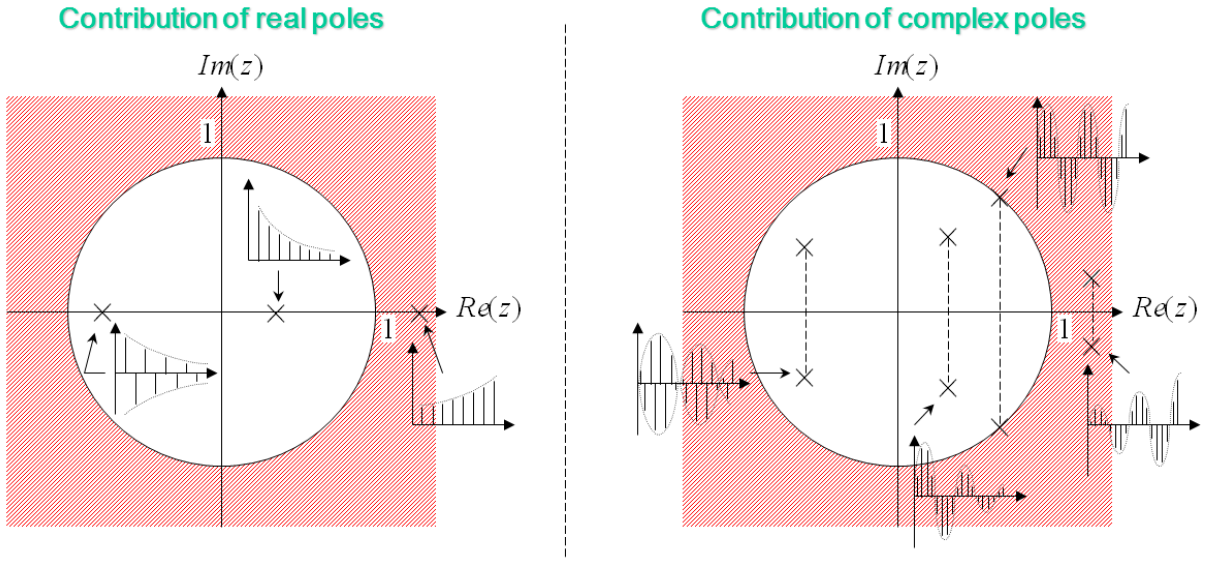

Fig. 15: Influence of the poles on the system transient behaviour

3.4.3 *Particular case: second-order systems*

As seen previously, a common controller design method consists in deriving the controller parameters from a pole placement, such that the dominant closed-loop dynamics is of first or second order. If a second-order system behaviour is chosen, this strategy consists in identifying the coefficients of the closed-loop transfer function denominator with those of the following reference polynomial:

$$Den_{CL_{\text{des}}}(z) = (1 - z_1 \cdot z^{-1}) \cdot (1 - \bar{z}_1 \cdot z^{-1}) \cdot P_{\text{aux}}(z)\,, \tag{45}$$

where $z_1 = \mathrm{e}^{-w_n \cdot Ts \cdot \left(\zeta - j \cdot \sqrt{1-\zeta^2}\right)}$ and $\bar{z}_1$ are the desired dominant poles, and P_{aux} is a polynomial containing additional faster poles.

The choice of the dominant poles depends on the closed-loop behaviour specifications: the rise time and peak overshoot requirements impose the values of the cut-off frequency w_n and the damping ratio ζ of the closed-loop system, according to Eqs. (13) and (14). The settling time requirement puts a constraint on the sampling period:

$$t_s = 4.6/\zeta \cdot w_n \;\Rightarrow\; |z_1| < \mathrm{e}^{-4.6 \cdot Ts/t_s} \approx 0.01^{Ts/t_s}\,. \tag{46}$$

3.4.4 *Precision of closed-loop discrete systems*

The conclusions in the continuous-time domain remain valid: to achieve zero steady-state error, the open-loop transfer function must contain the internal model of the reference (for example, at least one integrators (pole at $z = 1$) is required for a step input). To reject perturbations of class N in steady state, at least N integrators are needed in the open-loop transfer function.

3.5 Discrete-time controller synthesis

There are two main strategies employed to design digital controllers:

- Emulation design, which consists in designing first a controller in the continuous-time domain. Afterwards, the controller is discretized such that the overall system preserves its characteristics.
- Direct discrete-time design, which consists in discretizing the plant at first using an appropriate hold device. Analysis and design can then be carried out in the discrete-time domain.

3.5.1 Emulation design

3.5.1.1 Principle of emulation design

The first step is the continuous-time controller design. At this stage the sampling is ignored. The next step is the discretization of the controller by using an approximation (emulation) method enabling the approximation at best of the continuous-time controller. The usual approximation methods are the Euler method and the Tustin method (also called bilinear transformation), which consist in substituting s by Eqs. (47) and (48). The controller algorithm (difference equation) can then be derived.

Backward Euler transformation: $$s \to \frac{1}{Ts} \cdot \left(1 - z^{-1}\right); \tag{47}$$

Tustin transformation: $$s \to \frac{2}{Ts} \cdot \frac{1 - z^{-1}}{1 + z^{-1}}. \tag{48}$$

As an example, let us discretize a PI controller using the Tustin transformation:

$$C(s) = k_\mathrm{p} \cdot \left(1 + k_\mathrm{i}/s\right);$$

$$C(z) = C(s)\Big|_{s=\frac{2}{Ts}\cdot\frac{1-z^{-1}}{1+z^{-1}}} = k_\mathrm{p} \cdot \left(\frac{1 + k_\mathrm{i} \cdot Ts/2 + \left(-1 + k_\mathrm{i} \cdot Ts/2\right) \cdot z^{-1}}{1 - z^{-1}} \right).$$

3.5.1.2 Comparison between Euler and Tustin approximation methods

Both approximation methods preserve the stability, as shown in Fig. 16.

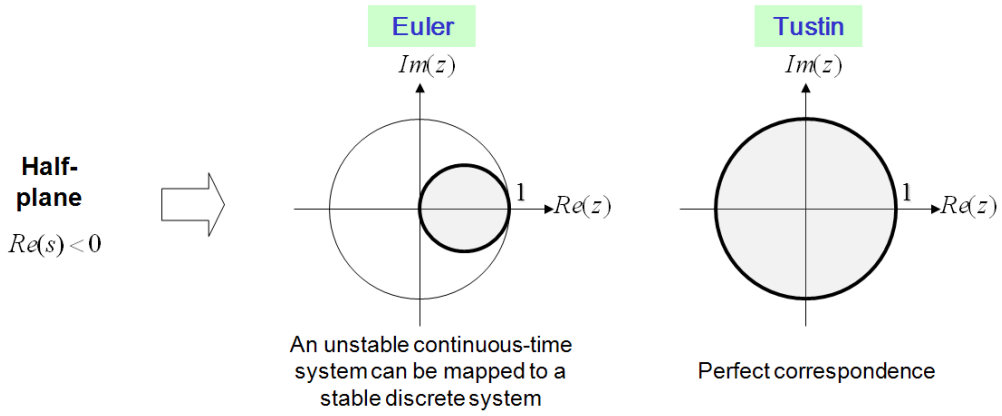

Fig. 16: Transformation of the stability region

Let us examine the image of a pole s_0 of a continuous-time system, obtained through these transformations:

– With the Euler transformation, the corresponding pole in the discrete-time domain is

$$z_0 = 1/(1 - s_0 \cdot Ts) = 1 + (s_0 \cdot Ts) + (s_0 \cdot Ts)^2 + (s_0 \cdot Ts)^3 + \ldots . \quad (49)$$

– With the Tustin transformation, the corresponding pole is

$$z_0 = (1 + s_0 \cdot Ts/2)/(1 - s_0 \cdot Ts/2) = 1 + (s_0 \cdot Ts) + \frac{1}{2} \cdot (s_0 \cdot Ts)^2 + \frac{1}{4} \cdot (s_0 \cdot Ts)^3 + \ldots . \quad (50)$$

Compared to the relation

$$z_0 = e^{s_0 \cdot Ts} = 1 + (s_0 \cdot Ts) + \frac{1}{2} \cdot (s_0 \cdot Ts)^2 + \frac{1}{6} \cdot (s_0 \cdot Ts)^3 + \ldots \quad (51)$$

Eqs. (49) and (50) constitute, respectively, a first-order and a second-order approximation. The higher the sampling frequency, the smaller the approximation error.

The poles (and the zeros) being not preserved, the system frequency response is changed. By way of example, the frequency responses of the derivative terms obtained through both transformations are shown in Fig. 17.

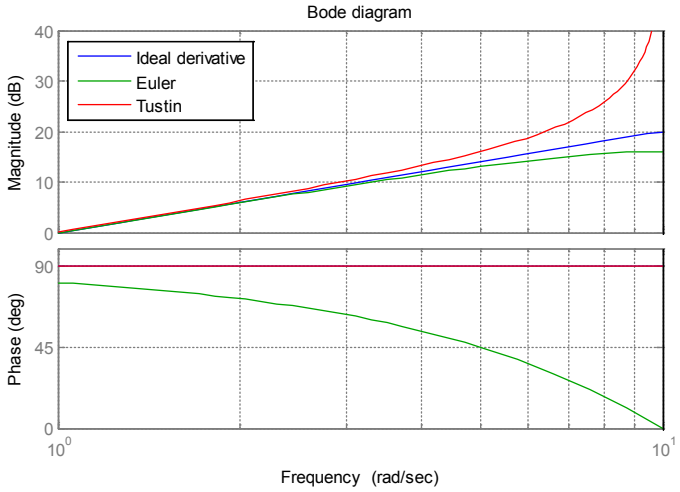

Fig. 17: Discretization of a pure derivative (Ts = 0.3)

It can be seen that there is an inherent filtering effect at high frequencies with the Euler transformation, whereas with the Tustin transformation the magnitude increases with the frequency, resulting in noise amplification at high frequencies. Thus the Euler transformation is more appropriate for the discretization of high-pass filters, and the Tustin approximation is more appropriate for the discretization of low-pass filters. To convert continuous-time controllers to discrete-time ones, the Tustin method is the approximation of choice, as it provides better accuracy.

To conclude, an emulation controller always suffers performance degradation as compared to its continuous-time counterpart. To make the set {ADC – digital controller – DAC} behave the same as the continuous-time controller, a very fast sampling frequency may be needed. Special attention should be paid to the impact on the loop phase margin of the control delay (ADC and DAC delays + delay due to the computation of control algorithm by the processor) and the anti-aliasing filter.

3.5.2 Direct discrete-time design

Working entirely with discrete systems, using plant discrete-time modelling, is another approach. This design method enables us to relax the constraint on the sampling period.

3.5.2.1 Discussion on the choice of the sampling period

A too small sampling period has the following consequences.

- Fast and expensive control hardware is required.
- Numerical issues may occur: the relation between poles in the s-domain and the z-domain is given by $z_i = \mathrm{e}^{s_i \cdot Ts}$. So for $Ts \to 0$ we have $z_i \to 1 \ \ \forall s_i$. This may cause trouble when working in finite precision.
- The plant discretization may lead to the introduction of unstable zeros, which are difficult to compensate for.

On the contrary, a too large sampling period results in the following.

- Loss of information and aliasing, in the case of the violation of the Nyquist–Shannon sampling theorem.
- The regulation may not react readily enough to disturbances affecting the system.
- Plant discretization may yield poles having a negative real part: this is not desirable as the step response caused by such poles cycles back and forth between positive and negative deviations from the steady-state value. To prevent this, the following condition must be satisfied: $1/Ts > (2/\pi) \cdot \left| \ \mathrm{Im}(s_i) \ \right|$.

A suitable choice for the sampling period is

$$\frac{1}{Ts} \in \left[6 \cdot F_{\mathrm{B}}^{\mathrm{CL}} \ , \ 25 \cdot F_{\mathrm{B}}^{\mathrm{CL}} \right], \tag{52}$$

where $F_{\mathrm{B}}^{\mathrm{CL}}$ is the desired closed-loop bandwidth [2,14].

3.5.2.2 RST-controller design

The general structure of a discrete controller for linear single-input single-output systems is represented in Fig. 18.

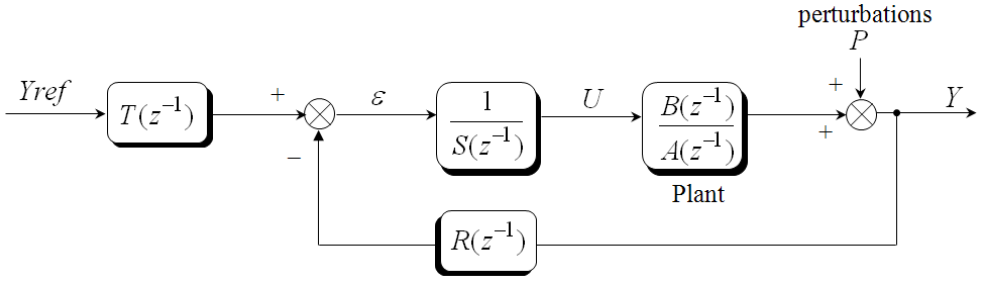

Fig. 18: RST-controller structure

This tri-branched structure is known as the RST structure: *R*, *S*, and *T* are three z^{-1} polynomials to be determined, usually by pole-zero placement. The control signal is calculated as

$$U(z) = \frac{T(z^{-1})}{S(z^{-1})} \cdot Yref(z) - \frac{R(z^{-1})}{S(z^{-1})} \cdot Y(z). \tag{53}$$

This is a combination of feedforward (first term) and feedback (second term), which can be tuned separately. The general approach with RST is to decouple the tracking behaviour (reference

following) from the regulation behaviour (disturbance rejection); R and S give the regulation behaviour, and T gives the tracking behaviour [15–18].

The tracking transfer function is

$$\frac{Y}{Yref} = \frac{B \cdot T}{A \cdot S + B \cdot R} \tag{54}$$

and the regulation transfer function is

$$\frac{Y}{P} = \frac{A \cdot S}{A \cdot S + B \cdot R}. \tag{55}$$

Note that a PID controller is a special case of RST controller, where

$$Num_{\text{PID}}(z^{-1}) = R(z^{-1}) = r_0 + r_1 \cdot z^{-1} + r_2 \cdot z^{-2},$$

$$Den_{\text{PID}}(z^{-1}) = S(z^{-1}) = (1 - z^{-1}) \cdot (1 + s_1 \cdot z^{-1}),$$

$$T(z^{-1}) = R(z^{-1}).$$

The RST control law can be synthesized using the following design method:

1. Choice of the desired closed-loop transfer function:

$$CL_{\text{des}}(z^{-1}) = B_m(z^{-1}) / A_m(z^{-1}) \tag{56}$$

If a second-order system behaviour is chosen, A_m has the following form (see Section 3.4.3):

$$A_m(z^{-1}) = P_{\text{dom}}(z^{-1}) \cdot P_{\text{aux}}(z^{-1}) = (1 - z_1 \cdot z^{-1}) \cdot (1 - \bar{z_1} \cdot z^{-1}) \cdot P_{\text{aux}}(z^{-1}), \tag{57}$$

where $z_1, \bar{z_1} = \mathrm{e}^{-\zeta \cdot w_n \cdot Ts} \cdot \mathrm{e}^{\pm j \cdot w_n \cdot Ts \cdot \sqrt{1-\zeta^2}}$ are the dominant poles.

If a first-order system behaviour is desired, P_{dom} is of the form

$$P_{\text{dom}}(z^{-1}) = (1 - a_1 \cdot z^{-1}), \tag{58}$$

where $a_1 = \mathrm{e}^{-Ts/\tau}$, τ being the desired time constant.

2. Cancellation of stable poles and zeros of the plant transfer function:

Let us expand the plant transfer function:

$$H(z^{-1}) = \frac{B(z^{-1})}{A(z^{-1})} = \frac{B^-(z^{-1}) \cdot B^+(z^{-1})}{A^-(z^{-1}) \cdot A^+(z^{-1})} \tag{59}$$

– $A^-(z^{-1})$ contains the poles which will not be compensated, namely poles lying outside the unit circle (called unstable poles), poorly damped poles, and poles with negative real part.

– $B^-(z^{-1})$ contains the zeros which will not be compensated, namely zeros lying outside the unit circle (unstable zeros), the plant pure delay (of the form z^{-d}), poorly damped zeros, and zeros with negative real part.

$B^-(z^{-1})$ cannot be a factor of $A \cdot S + B \cdot R$ (the closed loop would be unstable). Thus $B_m(z^{-1})$ must be of the form

$$B_m = B^- \cdot B_{m_1} . \tag{60}$$

The pole–zero cancellation yields

$$R(z^{-1}) = A^+(z^{-1}) \cdot R_1(z^{-1}) , \tag{61}$$

$$S(z^{-1}) = B^+(z^{-1}) \cdot S_1(z^{-1}) , \tag{62}$$

$$T(z^{-1}) = A^+(z^{-1}) \cdot B_{m_1}(z^{-1}) . \tag{63}$$

3. Perturbation rejection in steady state: an appropriate number of integral terms is introduced into the loop by means of the polynomial *S*:

$$S_1(z^{-1}) = (1 - z^{-1})^{n-l} \cdot S_2(z^{-1}) , \tag{64}$$

where *n* and *l* are, respectively, the perturbation and plant classes.

4. Computation of *R* and *S*: the polynomials $R_1(z^{-1})$ and $S_2(z^{-1})$, of the smallest possible degree, are determined by the resolution of the Diophantine equation:

$$A^-(z^{-1}) \cdot (1 - z^{-1})^{n-l} \cdot S_2(z^{-1}) + B^-(z^{-1}) \cdot R_1(z^{-1}) = A_m(z^{-1}) \tag{65}$$

Then *R* and *S* are derived from Eqs. (61), (62), and (64).

5. Computation of *T* using Eq. (63). To ensure unity gain to the closed loop, the condition $T(1) = R(1)$ must be satisfied.

Let us return to the example used in Section 2.4.2.2—the RST controller for the outer current loop is designed in the following. The design specifications are:

- regulation behaviour—second-order system behaviour with a closed-loop bandwidth equal to $F_{\mathrm{B}}^{\mathrm{CL}}$;
- tracking behaviour—no overshoot.

The controller sampling period is chosen according to Eq. (52).

Let us assume that oversampling is used to improve resolution and reduce noise of the current measure, and that the cut-off frequency of the anti-aliasing filter is high compared to $F_{\mathrm{B}}^{\mathrm{CL}}$; hence there is no need to take it into account in the open-loop transfer function.

Let us also assume that the bandwidth of the inner voltage loop is high in comparison with the sampling frequency of the outer current loop: the digital model of the voltage source can be reduced to a simple unit gain.

Thus the plant transfer function shrinks down to

$$H(s) = \mathrm{e}^{-tc \cdot s} \cdot \frac{b_0}{1 + a_1 \cdot s} , \text{ with } b_0 = 1/R_{\mathrm{load}} , \quad a_1 = L_{\mathrm{load}}/R_{\mathrm{load}} , \tag{66}$$

where $tc = n \cdot Ts - \theta$ ($0 \le \theta < Ts$) is the delay associated with conversion and computation times.

The discrete-time model can then be derived from Eq. (37):

$$H(z^{-1}) = (1 - z^{-1}) \cdot Z\left[\frac{e^{-tc \cdot s}}{s} \cdot \frac{b_0}{1 + a_1 \cdot s}\right] = b_0 \cdot z^{-n} \cdot (1 - z^{-1}) \cdot Z\left[\frac{e^{\theta \cdot s}}{s} \cdot \frac{1}{1 + a_1 \cdot s}\right].$$

Using Eqs. (34) and (35), we have

$$Z\left[\frac{e^{\theta \cdot s}}{s} \cdot \frac{1}{1 + a_1 \cdot s}\right] = \lim_{s \to 0}\left[\frac{e^{\theta \cdot s}}{1 + a_1 \cdot s} \cdot \frac{1}{1 - e^{s \cdot Ts} \cdot z^{-1}}\right] + \lim_{s \to -1/a_1}\left[\frac{1}{a_1} \cdot \frac{e^{\theta \cdot s}}{s} \cdot \frac{1}{1 - e^{s \cdot Ts} \cdot z^{-1}}\right]$$
$$= \frac{1}{1 - z^{-1}} - \frac{e^{-\theta / a_1}}{1 - e^{-Ts/a_1} \cdot z^{-1}}.$$

Finally,

$$H(z^{-1}) = \frac{B(z^{-1})}{A(z^{-1})} = b_0 \cdot z^{-n} \cdot \frac{1 - e^{-\theta/a_1} + (e^{-\theta/a_1} - e^{-Ts/a_1}) \cdot z^{-1}}{1 - e^{-Ts/a_1} \cdot z^{-1}}. \tag{67}$$

Let us assume that $Ts << a_1$ (sampling period small compared to load time constant) and $tc << Ts$. Equation (67) becomes

$$H(z^{-1}) = \frac{B(z^{-1})}{A(z^{-1})} \approx \frac{b_0}{a_1} \cdot z^{-1} \cdot \frac{Ts}{1 - z^{-1}} = \frac{k_1 \cdot z^{-1}}{1 - z^{-1}}. \tag{68}$$

An integrator is placed into the polynomial $S(z^{-1})$, i.e., $S(z^{-1}) = (1 - z^{-1}) \cdot S_1(z^{-1})$. The polynomials S_1 and R are then calculated by solving the following Diophantine equation:

$$(1 - z^{-1})^2 \cdot S_1(z^{-1}) + k_1 \cdot z^{-1} \cdot R(z^{-1}) = A_m(z^{-1}) = (1 - z_1 \cdot z^{-1}) \cdot (1 - \bar{z_1} \cdot z^{-1}), \tag{69}$$

where $z_1, \bar{z_1} = e^{-\zeta \cdot w_n \cdot Ts} \cdot e^{\pm j \cdot w_n \cdot Ts \cdot \sqrt{1 - \zeta^2}}$, $w_n = 2 \cdot \pi \cdot F_B^{CL}$, and $\zeta \ge 1$. We obtain

$$S_1(z^{-1}) = 1 \;\Rightarrow\; S(z^{-1}) = 1 - z^{-1}, \tag{70}$$

$$R(z^{-1}) = r_0 + r_1 \cdot z^{-1}, \text{ with } r_0 = \frac{2 - (z_1 + \bar{z_1})}{k_1}, \quad r_1 = \frac{z_1 \cdot \bar{z_1} - 1}{k_1}. \tag{71}$$

If a simple gain is chosen for T, there is no undesirable zero in the tracking transfer function (no overshoot). To ensure unity gain to the closed loop, we must have

$$T(z^{-1}) = r_0 + r_1. \tag{72}$$

If a good tracking of the reference (with no lagging error) is required, the polynomial $T(z^{-1})$ can be fixed as follows:

$$T(z^{-1}) = A_m(z^{-1}) / k_1 = (1 - z_1 \cdot z^{-1}) \cdot (1 - \bar{z_1} \cdot z^{-1}) / k_1. \tag{73}$$

Then the tracking transfer function becomes

$$\frac{Y(z)}{Yref(z)} = \frac{B(z^{-1}) \cdot T(z^{-1})}{A(z^{-1}) \cdot S(z^{-1}) + B(z^{-1}) \cdot R(z^{-1})} = \frac{k_1 \cdot z^{-1} \cdot T(z^{-1})}{A_m(z^{-1})} = z^{-1}, \quad (74)$$

which means that the control loop replicates exactly the reference with one sampling step delay. This control technique, called dead-beat control, is very attractive since it can theoretically provide the fastest dynamic response for a digital implementation [18–20]. However, it requires an accurate modelling of the plant (polynomials *A* and *B*). In the case of model and parameter mismatches, significant deviations from the expected closed-loop performance can take place. Therefore, identification from experimental data may be necessary to refine the plant model. Moreover, if the plant parameters are likely to vary (e.g., magnet saturation), adaptive control with on-line tuning of the RST parameters may be required.

4 Conclusion

A brief review of regulation loops design in the continuous-time domains has first been made: the choice of the closed-loop performance has been discussed. PID controller synthesis using classical methods has been presented along with illustrating examples. Two different approaches to synthesize digital controllers have then been examined. The first one basically comprises translating an existing analogue controller (generally of PID type) into a digital one by using an approximation method. A good approximation of the continuous-time controller may imply the use of a high sampling frequency. The second method consists in synthesizing the digital controller by working with discrete systems exclusively. The sampling frequency is then chosen in accordance with the desired closed-loop bandwidth. This enables a better use of the potentialities of digital control, as the decrease of the sampling frequency favours the implementation of more complex control algorithms (RST type, requiring greater computational time), and the introduction of better digital signal filtering.

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High Precision Current Measurement for Power Converters

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Abstract
The accurate measurement of power converter currents is essential to controlling and delivering stable and repeatable currents to magnets in particle accelerators. This paper reviews the most commonly used devices for the measurement of power converter currents and discusses test and calibration methods.

Keywords
Current measurement; current transformer; DCCT; calibration.

1 Introduction

Power converters for particle accelerators are required to deliver extremely accurate currents to the accelerator magnets. An essential element in guaranteeing the required performance is the current measurement device used for the control of the power converter current. For this reason, a lot of the developments within the field of current measurement for power converters over the last 50 years have been driven by the accelerator community and have happened in collaboration with the accelerator world. In the following sections the main current measuring devices available for power converter applications will be reviewed and discussed, including some of their advantages and disadvantages. Test and calibration methods will be discussed and their application to different accuracy requirements evaluated.

2 Metrology—Terms and definitions

There can be some confusion when using metrology terms in power converter applications for accelerators. Accelerator applications require repeatable and stable magnetic field conditions, and therefore power converters must provide repeatable and stable currents. The measurement devices used to measure these currents play a crucial part in obtaining this performance.

Current measuring devices are often specified by manufacturers and users in terms of ‘accuracy’ and ‘precision’. It is therefore useful to clarify the use of these terms and some of the metrology vocabulary required to properly describe and characterize the performance of measurement devices.

According to the guide to the expression of uncertainty in measurement [1], accuracy is a qualitative concept referring to the closeness of agreement between a measurement and the true value of the measurand (or an accepted reference value). The quantitative expression of the accuracy (or lack of it) of a system is called uncertainty. Uncertainty is a non-negative parameter characterizing the quantity values attributed to a measurand. It is often expressed by a standard deviation. As for precision, it refers to the spread between measurements under the same conditions with no regard for the true value of the measurand [1].

The difference between precision and uncertainty is that uncertainty is given with regards to the true value of the measurand. The most common approaches to express uncertainty are:

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– representing each component of uncertainty by a standard deviation;
– obtaining the combined uncertainty using the root-sum-of-squares method;
– multiplying the combined uncertainty by a coverage factor *k*, to increase the level of confidence.

A coverage factor of $k = 1$ means that 68.3% of the measurements are asserted to lie within the given uncertainty. A level of confidence of 95.5% corresponds to a coverage factor $k = 2$.

In accelerator applications, it is often useful to characterize a current measurement system's capabilities in terms of *gain* and *offset* errors, *linearity*, *repeatability*, *reproducibility* and *stability*.

Repeatability is extremely important in accelerator applications. Repeatability can be defined as the closeness of agreement between successive measurements carried out under the same conditions, while reproducibility refers to changing conditions [1]. The offset and gain errors refer to the systematic error at zero and full scale. Linearity describes a difference in the systematic errors throughout the measuring range, and stability can be defined as the change of measurement errors with time.

3 Current measuring devices

Table 1 presents a comparison of several well-known current measuring devices, including direct-current current-transducers (DCCTs) and current transformers (CTs) and some of their most important characteristics.

Table 1: Current measuring devices

	DCCTs	**Hall effect**	**CTs**	**Rogowsky**	**Shunts**
Principle	Zero flux detector	Hall effect	Faraday's law	Faraday's law	Ohm's law
Output	Voltage/current	Voltage/current	Voltage/current	Voltage	Voltage
Accuracy	Best devices can reach ppm uncertainty	Best devices can reach 0.1% uncertainty	Typically not better than 1% uncertainty	Typically percentage uncertainty, better is possible with digital integrators	PPM uncertainty for low currents, percentage for high currents
Ranges	Tens of A to tens of kA	Hundreds of mA to tens of kA	Tens of A to tens of kA	High currents up to 100 kA possible	From mA up to several kA
Bandwidth	kHz for higher DC currents, up to a couple of hundred kHz for lower DC currents	DC up to a couple of hundred kHz	Typically 50 Hz up to a few hundred kHz	A few Hz possible, up to MHz	Up to hundreds of kHz with coaxial assemblies
Isolation	Yes	Yes	Yes	Yes	No
Error sources	Magnetic (remanence, external fields, centring); Burden resistor (thermal settling, stability, linearity, temperature coefficient); Output amplifier (stability, noise, common mode rejection, temperature coefficient)	Magnetic; Burden resistor; Output amplifier; Hall sensor stability (temperature coefficient, piezoelectric effect)	Magnetic (remanence, external fields, centring, magnetizing current); Burden resistor	Magnetic integrator (offset stability, linearity, temperature coefficient)	Power coefficient; Temperature coefficient; Ageing; Thermal voltages

As can be seen, DCCTs guarantee the best performance but they are also the most complex devices, with several possible error sources.

3.1 Current transformers

Current transformers (CT) are instrument transformers that produce, from an AC primary current, a proportional secondary current. The secondary winding is connected to a burden resistor to produce a measurable voltage signal.

The simplified equivalent circuit, referred to the secondary, of a current transformer [2] is shown in Fig. 1.

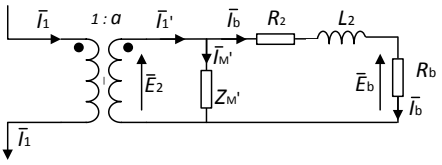
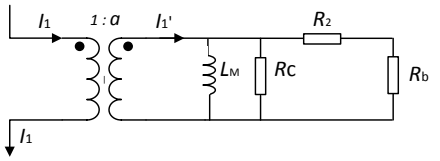


Fig. 1: Current transformer simplified equivalent circuit

The magnetizing current causes an amplitude and phase error in the CT. The secondary leakage impedance adds to the burden resistor, affecting the current distribution between I_M and I_b. To improve accuracy, the magnetizing inductance must be maximized and leakage inductance must be minimized (high μ_r, good winding distribution). It is important to remember that, as the CT approaches saturation, the magnetizing inductance decreases, increasing the error ratio.

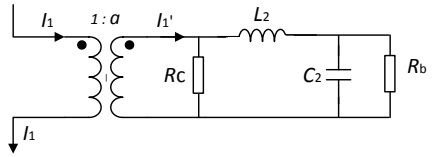
Other sources of uncertainty include errors due to external magnetic fields. External fields move the CT closer to saturation and therefore a magnetic shielding should be used to minimize this effect.

Figure 2 shows the low frequency and high frequency models of the CT.



$$f_{LF} = \frac{\omega_{LF}}{2\pi} = \frac{R_C || (R_b + R_2)}{2\pi L_M} \tag{1}$$

(a)



$$f_{p1} = \frac{\omega_{p1}}{2\pi} = \frac{1}{2\pi R_b C_2} \qquad f_{p2} = \frac{\omega_{p2}}{2\pi} = \frac{R_C}{2\pi L_2} \tag{2}$$

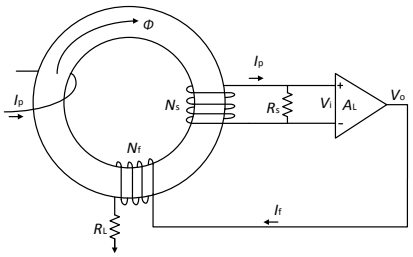
(b)

Fig. 2: Current transformer (a) low and (b) high frequency simplified equivalent circuits

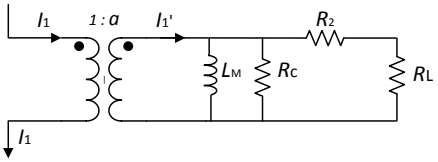
To extend the CT's low-frequency response the magnetizing inductance should be maximized. This means using high-permeability cores (e.g. silicon steel or nickel alloy). Limited low-frequency response causes droop in pulse measurement applications. The high cut-off frequency is mostly determined by leakage inductance and stray capacitance which, with some approximations, gives the origin of the two real poles shown in Fig. 2.

3.2 Hereward transformer

In the 1960s, H.G. Hereward proposed an active current transformer circuit that used electronic feedback to extend the low-frequency response of a CT and improve its accuracy (Fig. 3) [3]. In this device, an active circuit senses the voltage across the CT burden and uses a feedback loop to produce a compensation current that keeps the total flux in the cores at zero. The compensation current is a fractional image of the primary current. The effect of the feedback is equivalent to increasing the magnetizing inductance L_M by (A_L + 1), in which A_L is the open loop gain of the sensing amplifier. This technique results in improved accuracy and extended low-frequency response.



(a)



$$f_{\mathrm{LF}} = \frac{\omega_{\mathrm{LF}}}{2\pi} = \frac{R_{\mathrm{C}} || (\boldsymbol{R}_{\mathrm{L}} + R_2)}{2\pi L_{\mathrm{M}}} \tag{3}$$

(b)

Fig. 3: Hereward transformer simplified equivalent circuit

3.3 DCCTs

In DCCTs this principle is taken further and combined with the magnetic modulator principle (used since the 1930s in fluxgate magnetometers) to provide an accurate measurement of currents ranging from DC to a few hundred kHz [4].

3.3.1 Theory of operation

In a DCCT the primary current generates a magnetic flux that is seen by three cores (Fig. 4). A magnetic modulator drives two of the sensing cores in and out of saturation. The current peaks due to saturation of the cores are symmetrical if there is no DC flux in the cores and unequal if there is a DC flux in the cores. The current peak asymmetry due to any DC flux is measured and combined with the AC component measured by the third core. A control loop generates a compensation current that makes the total flux zero. This current is a fractional image of the primary current and can be measured with a burden resistor and an amplifier [5].

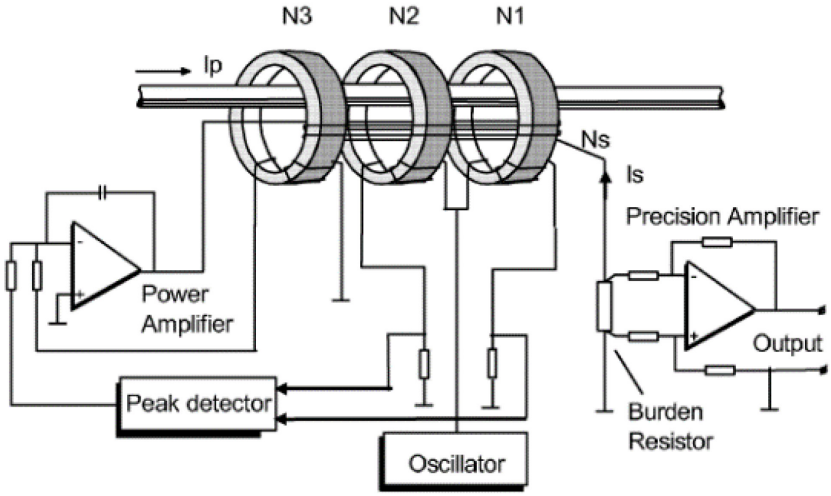


Fig. 4: DCCT theory of operation

3.3.2 Sources of error in DCCTs

Errors in DC measurements with DCCTs can come from different sources. The most common are related to the magnetic head, the burden resistor and the output amplifier:

- magnetic head: sensitivity to external magnetic fields, return bar, centring;
- burden resistor: gain error, settling at full scale (FS), stability at FS, linearity, gain temperature coefficient (TC);
- output difference amplifier circuit: offset error, settling at zero, stability at zero, offset and gain TC, noise, common mode rejection ratio (CMRR).

3.3.3 Magnetic circuit

The magnetic head of a DCCT plays an essential role in guaranteeing the ratio and offset accuracy in a DCCT. The magnetic circuit comprises high-permeability tape-wound magnetic cores with modulation windings. A magnetic shielding is used around the cores to protect them from external and leakage fields. The secondary windings are wound on top of the shielded assembly.

In addition to the factors mentioned in Section 3.3.2, magnetic remanence and modulation noise due to poor matching of sensing cores are other important factors to be considered in the design of the magnetic heads (Fig. 5).

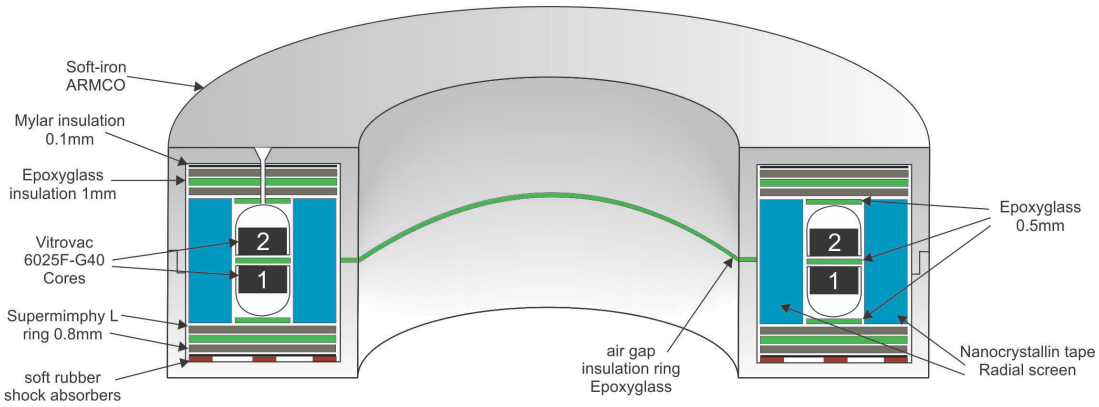


Fig. 5: DCCT magnetic head design

3.3.4 Burden resistor

The burden resistor is the most common source of uncertainty in DCCTs. Four-wire current sensing resistors are normally used. For power dissipation, a foil-based technology is a better choice than a wire. Common foil substrates are alumina and copper. A film deposited on a substrate is also a popular solution (thin film, thick film).

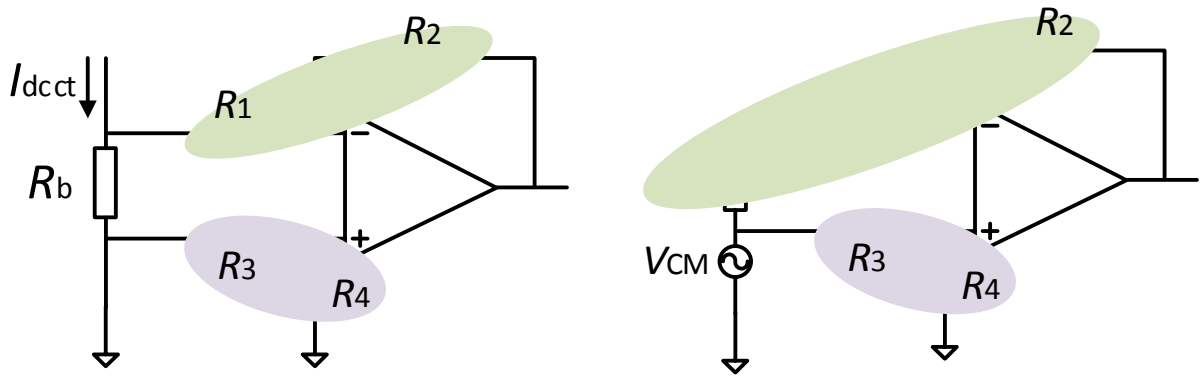
An important aspect to consider in the choice of resistors is that tolerance and stability do not always go together: processes that lead to tighter tolerances can result in degraded stability due to degraded power distribution and the creation of hotspots.

The main factors affecting resistor performance are related to their thermal behaviour. Well-known thermal effects upon resistance include the change of resistance with ambient temperature (ΔT.TCR) and the change of resistance with internal temperature due to self-heating ($P.\theta R$.TCR). Less well-known effects include the power coefficient of resistance, which describes the transient effect of a change of resistance due to mechanical and thermal gradient phenomena linked to self-heating. Hysteresis under power cycling and humidity absorption/evaporation are other important factors that must be considered.

As mentioned above, resistor foil-based technologies are preferred, and bulk metal foil is now widely used in precision applications. It consists of a rolled metal foil (NiCr) bonded to a substrate, usually alumina. The foil/hard-epoxy/alumina combination is designed to give zero TCR to ambient changes of temperature: the foil TCR compensates for mechanical compression due to the substrate's lower thermal expansion coefficient. The resulting TCR is close to zero. This works well when temperature changes occur in all layers equally. However, with dissipation in the foil, thermal gradients are different, which results in an over-compression of the foil and the effective TCR turning more negative. The power coefficient of resistance describes this effect [6].

3.3.5 Output amplifier

The output amplifier of a DCCT is usually a difference amplifier circuit (Fig. 6). Some important points on the design of this stage are the gain resistor drift (matched networks are often used) and the common mode rejection, for which the matching of the gain ratios plays a crucial role. One should notice that the burden resistor affects the matching of the gain ratios, degrading the common mode rejection. This has to be taken in consideration in the choice of the ratio values. For the same reason, gain adjustment through potentiometers should be avoided and can be replaced by digital calibration.



(a) (b)

Fig. 6: DCCT output amplifier circuit. Matched ratio networks are typically used to implement the ratios R2/R1 and R4/R3 (a). The common mode rejection of the circuit is determined by the matching between the two ratios, which is affected by the burden resistor (b).

3.4 Hall effect transducers

Hall effect current transducers have been the transducers of choice for DC to AC current measurement applications, when percentage accuracy is required. They are cheap, simple and easy to use, with PCB and cable-mounted versions for a wide range of currents. There are basically two types of Hall effect probes:

- open loop: a Hall probe is placed in the air gap of a toroidal magnetic circuit. The magnetic flux generated by the primary current produces a Hall voltage in the probe, which is then amplified to produce the output signal;
- closed loop: Hall voltage is used in a closed loop to generate a compensating current, which is an image of the primary current.

When comparing these two types, closed loop models are preferred for higher accuracy applications, although limited to not better than 0.1% uncertainty. For open loop models, 1% uncertainty is typical. These limitations are mostly due to the stability of the Hall probe. Sensitivity to EMI can also be an issue. Concerning bandwidth: core geometry, thickness of laminations, core material and Hall chip all impact the bandwidth of open loop probes, typically not better than 50 kHz. Closed loop probes can go up to 200 kHz.

3.5 Selection of current measuring devices

The choice of a current measuring device for a given application depends on various factors: type of application (current range, bandwidth), required accuracy, required output signal (voltage, current), need for isolation from primary current circuit, reliability (mean time between failures (MTBF)), installation constraints, availability and cost.

For high current, high accuracy applications (e.g. >1 kA, <50 ppm), DCCTs are the devices of choice. Although voltage output devices are more common, current output devices are also available with secondary currents ranging typically from 1 A to 5 A. They are normally composed of a magnetic head and a separated electronic chassis. This chassis must be installed close to the converter control electronics in order to minimize output signal transmission distances. This type of DCCT usually guarantees very good reliability.

For medium current, high to medium accuracy (e.g. hundreds of amperes, <100 ppm), DCCTs are still the only devices able to deliver the required performance. In this case it might be easier and advantageous to use current output devices. Current output allows the designer to adapt the burden and amplifier choice and design to the required accuracy. In many cases, for these currents, electronics and head are integrated together and installed close to the power components of the power converter and far from the control electronics, this means a harsher environment and longer transmission distances for the output signal. In such cases, current output can be an advantage.

For low accuracy (e.g. percentage uncertainty) applications, current transformers and Hall effect transducers must be considered. Their simplicity and cost-effectiveness make them more attractive than the more complex and expensive DCCTs. Shunts are another current measurement solution for application where electrical isolation is not required.

A special mention for fast applications: if bandwidth is limited to a few hundred kHz, the solutions described above may still apply. In particular, DCCTs' small signal bandwidth can go up to a few hundred kHz. One thing to watch out for in DCCTs is the modulation voltage noise at the output of the DCCT and the voltage induced in the primary, which can be a problem in fast applications.
For bandwidths higher than some hundreds of kHz, Rogowsky coils and coaxial shunts should be considered, as long as accuracy requirements remain around the percent figure.

3.6 Test methods

There are several methods for evaluating current measuring devices and, in particular, DCCTs. The most important are discussed here.

In the reference device method, the primary current is measured both by the DUT and by a reference device, which are then compared (Fig. 7). According to ANSI/NCSL Z540.3-2006, the performance of the reference device must be at least four times better than the device under test (DUT).

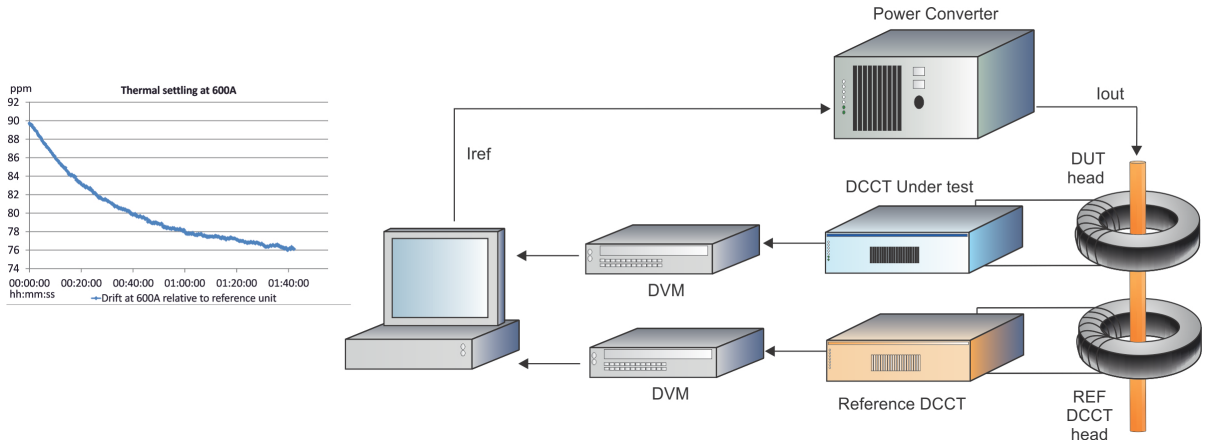


Fig. 7: The reference device test method

In the reference current method for testing DCCTs, a relatively small reference current is injected into an auxiliary winding with enough turns to simulate primary ampere turns (Fig. 8). The auxiliary winding can be permanent or temporary. The output of the DCCT is then measured with a precision digital voltmeter and the errors calculated.

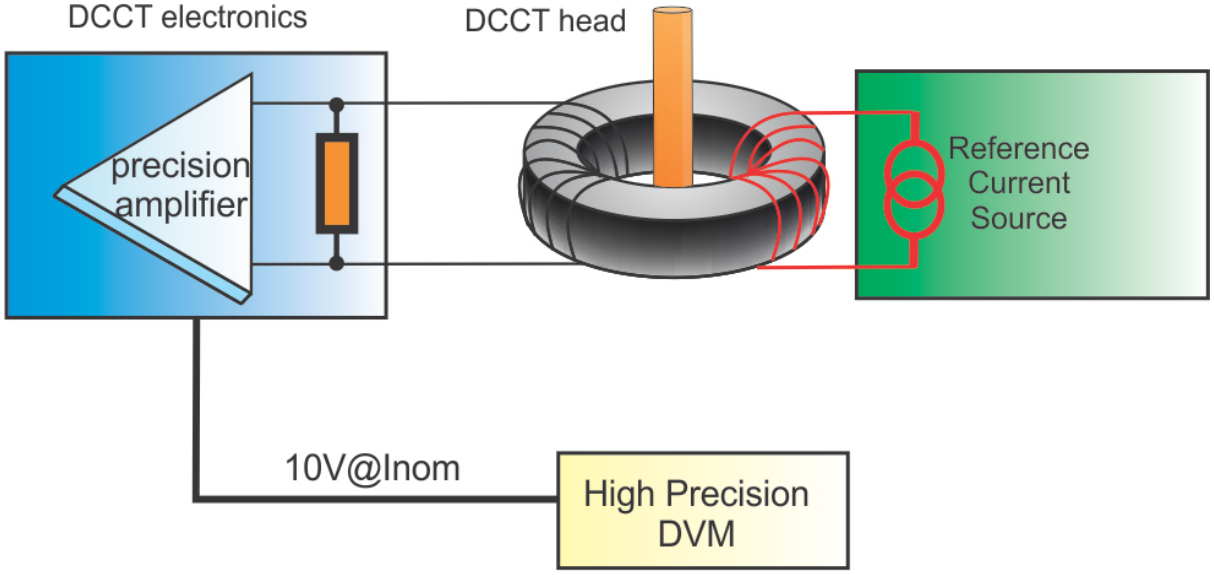


Fig. 8: The reference current test method

In DCCTs, a reference current can also be injected directly into the burden resistor in place of the compensation current (Fig. 9). The output of the DCCT is then measured with a precision digital voltmeter and the errors calculated. This test allows us to understand which errors are caused by the burden and output amplifier. This method must be used with care as common mode voltages between the burden resistor ground and the precision amplifier ground depend on the point of connection of the current source "low" terminal.

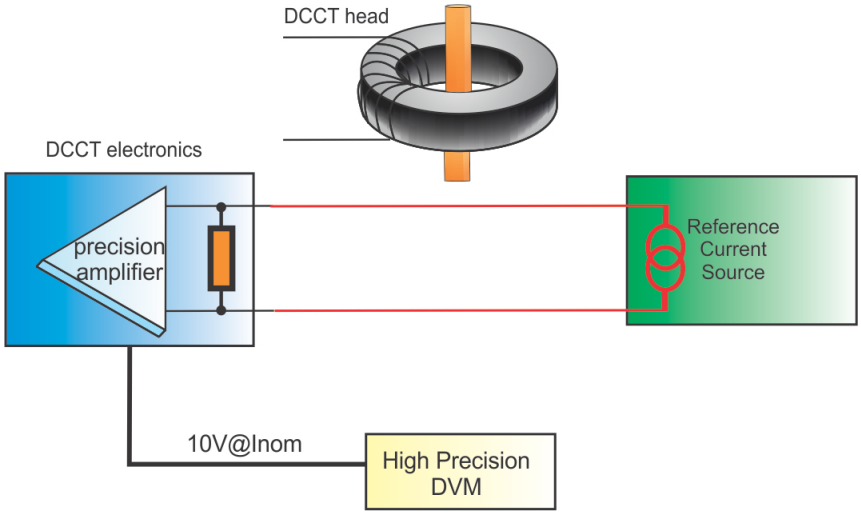


Fig. 9: The burden injection test method

On current output devices, the reference current can be compared 'back-to-back' with the DCCT current output as shown in Fig. 10. This test evaluates the quality of the current output of the DCCT, which is normally much better than the voltage output.

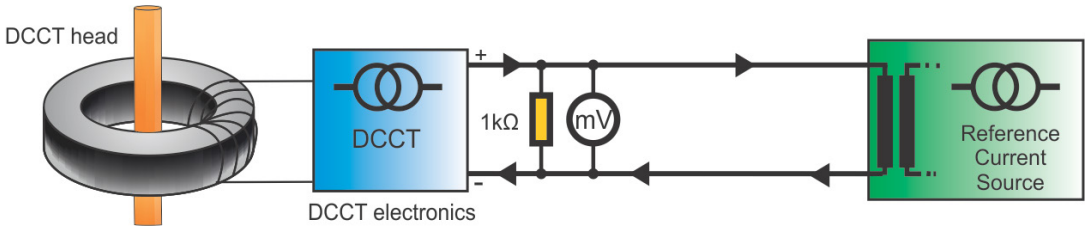


Fig. 10: The back-to-back test method

3.7 Test strategy

The test methods described above can be used for testing a current measuring device before installation and for calibration after installation. For high and very high accuracy applications, where <10 ppm measurement uncertainty is required, DCCTs are normally used. In these cases, intensive testing prior to installation is essential. These tests are performed in high-precision testbeds with specially chosen reference units or modified DCCTs. The test campaign can include installation and environmental tests such as centring, return bar influence, external magnetic field influence, temperature coefficient, EMC (voltage dips, burst test immunity, conducted noise), as well as performance tests such as gain, offset drift; settling at I_{nom}, linearity, noise, repeatability, reproducibility and settling at I_{min}.

In the most demanding applications these tests must be individually performed and the results properly tracked. For the less demanding applications, type-tests on a few units might be enough. In addition, integration tests should be performed upon installation of the DCCT in the power converters, to validate EMC and performance [7].

3.8 Calibration strategy

The first question to evaluate when deciding on a calibration strategy is knowing if a calibration strategy is really needed. Some of the issues to be considered when answering this question are:

- is long-term stability an important requirement in my application?
- what is the long-term drift of my current measuring devices?

- is there a need for tracking between different power converters?
- what is the impact of DCCT replacement? For example, replacing a DCCT that has drifted can cause a jump seen by the machine, and calibration can limit the size of this jump.

The calibration strategy must be adapted to the requirements of the application. For high- and very high-accuracy applications (e.g. <10 ppm relative accuracy, 50 ppm yearly drift) the calibration winding method and calibration against reference units are the best calibration methods. Both methods require specific calibration equipment, such as a suitable current source and suitable reference devices.

For medium accuracy applications (e.g. <100 ppm relative accuracy, 1000 ppm yearly drift) the comparison against a reference unit remains the best solution. The injection of a reference current into the burden resistor might be a more practical alternative for field calibrations where the installation of a reference unit is not possible. Again, these methods require either a suitable current source or suitable reference devices.

For low-accuracy applications with requirements in the order of percentage yearly drift, the need for calibration must be weighed against cost and effort, often resulting in a decision not to calibrate.

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Analogue to Digital and Digital to Analogue Converters (ADCs and DACs): A Review Update

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Abstract
This is a review paper updated from that presented for CAS 2004. Essentially, since then, commercial components have continued to extend their performance boundaries but the basic building blocks and the techniques for choosing the best device and implementing it in a design have not changed. Analogue to digital and digital to analogue converters are crucial components in the continued drive to replace analogue circuitry with more controllable and less costly digital processing. This paper discusses the technologies available to perform in the likely measurement and control applications that arise within accelerators. It covers much of the terminology and 'specmanship' together with an application-oriented analysis of the realisable performance of the various types. Finally, some hints and warnings on system integration problems are given.

Keywords:
DACs; ADCs; delta-sigma; quantum voltmeter; IEC60748-4-3.

1 Introduction

Analogue to Digital and Digital to Analogue Converters (ADCs and DACs) are some of the most important components in measurement and control technology. Their job is to transfer information between the real world and the digital world as faithfully as possible. See Fig. 1 for a typical situation.

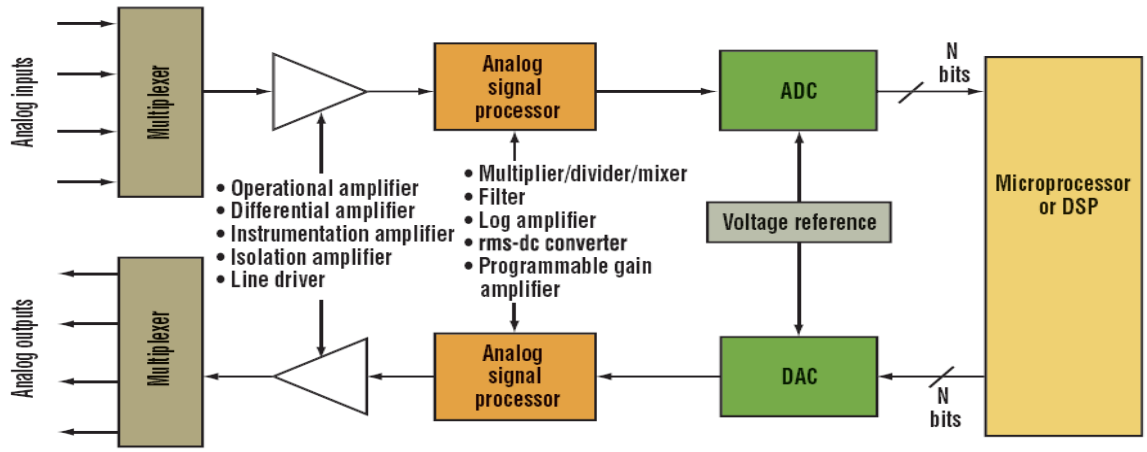

Fig 1: Measurement and control loop

Because of the advances in digital processing and its continuing improvement in cost effectiveness it is becoming more and more desirable to trade-off analogue for digital circuitry. An expression for this, commonly used in the communications business, is the trend to push 'digital to the antenna', thus notionally replacing all of the circuitry in a communications receiver with digital processing. The purpose of this article is to consider current commercial ADC and DAC technology

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suitable for application in measurement and control rather than the very highest performance special-purpose devices. This paper is an update on that appearing at the CERN accelerator school 2004.

2 Terms, nomenclature and specifications

Three standards that define specification terms for ADCs and DACs are:

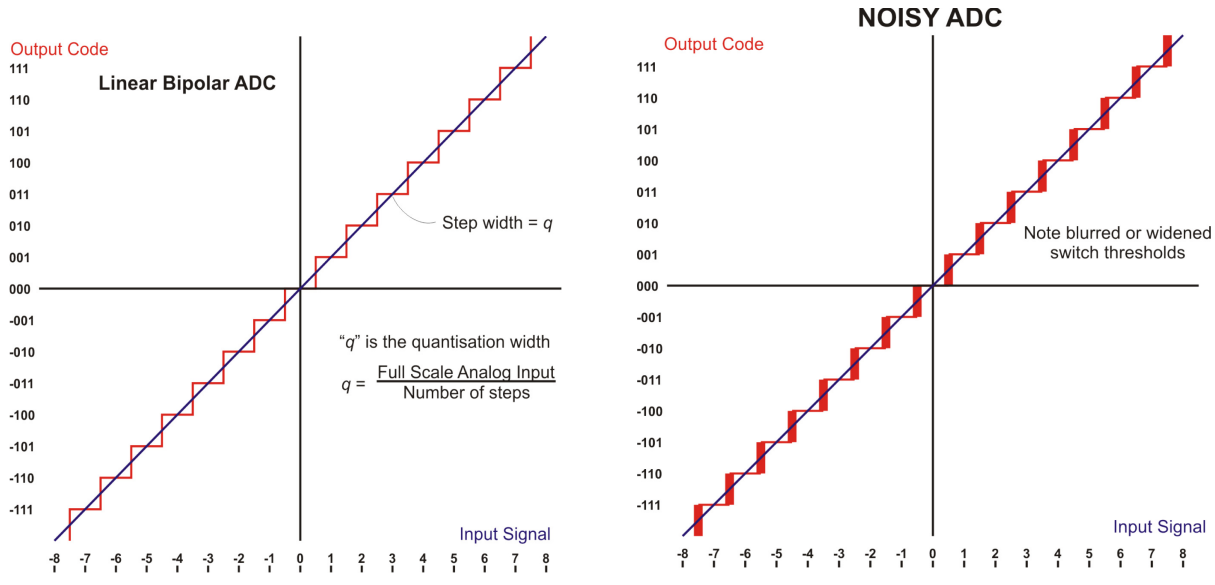
- IEC 60748-4, see Ref. [1];
- IEEE 1241, see Ref. [2];
- Dynamic testing of analogue to digital converters (DYNAD), see Ref. [3].

The IEC standard presently includes a general specification and is currently being updated to include the dynamic specifications that are covered by the other two standards. These, IEEE 1241 and DYNAD (which is the output of a European project SMT4-CT98-2214), concern dynamic specifications mainly defined in the frequency domain. A useful general standard is IEC 60748-4-3, which now covers dynamic performance.

2.1 General specifications

The most important terms are best discussed with reference to simplified diagrams showing a 7-bit converter. In all the ensuing discussions we will deal only with converters intended to have equal step sizes (that is, each bit or quantization level is of equal weight). This is not true of certain specialist converters, for example, companding types.

In Fig. 2(a) we have an ideal bipolar converter where the vertical scale is the output code and the horizontal scale is the analogue input. Each step in code represents an analogue increment of q, called the step width. As can be seen, starting from 0, each step occurs at ½ q analogue levels. Figure 2(b) shows the same with some random noise added, which results in an uncertainty in the switching thresholds. In these and all of the ensuing descriptions and figures we assume that zero and end point errors have been corrected by a $y = mx + c$ calibration.



(a) (b)

Fig 2: (a) Linear bipolar ADC; (b) noisy ADC

2.2 Misunderstood terms: 'resolution' and 'noise'

'Resolution', subject to much manufacturer 'specmanship', is the smallest discernible increment in analogue terms—however, this should be regarded as 'repeatably' discernible since all good measurement should be repeatable, another way of saying that it is not buried in noise or instability. A weakness, in this author's view, of IEC 60748-4 is that it defines resolution as the 'nominal value of the step width', which is far too simplistic and misleading for some types of ADC, resulting in specifications for some being quoted at '32 bits resolution' where reality is nearer 18 bits!

'Noise' comes from many sources and is not necessarily random and not necessarily 'white' since $1/f$ noise is always present. As far as specification numbers are concerned, noise is also represented very differently for varied applications. In DVMs it usually means 'peak' but in most integrated circuit (IC) ADCs it is rms. Presenting it as a percentage of full scale is another variable. DVMs tend to regard full scale as the maximum unipolar excursion possible but IC ADCs regard it as the full range from +ve peak to –ve peak operating range. The result is that the quantitative numbers can vary by 6:1 or more depending on these definitions.

2.3 Quantization error or noise Q_n

The quantization error of a perfect ADC is that error introduced by the finite number of digital codes, i.e. from the nominal step size. Figure 3 shows this. One can clearly see that the error, as signal is smoothly increased, changes in a saw-tooth manner between $+q/2$ to $-q/2$ where q is the nominal step size.

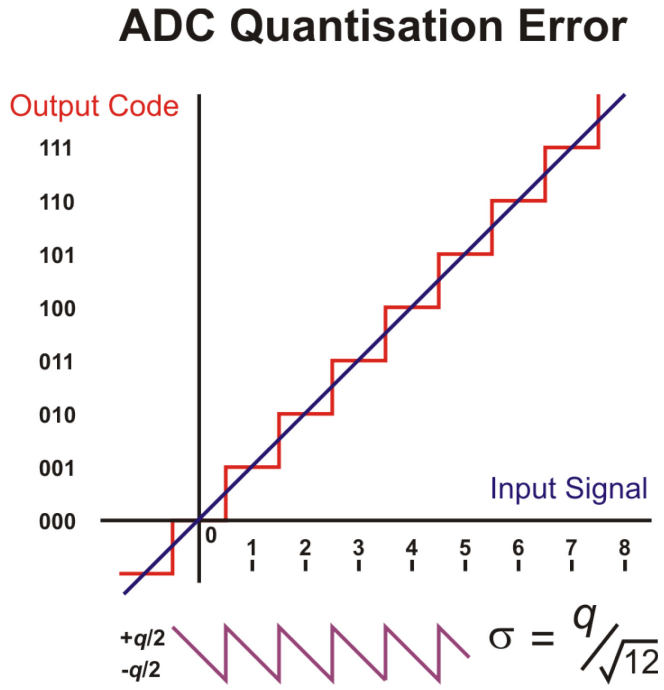


Fig. 3: ADC quantization error

This has a standard deviation of $\sigma = q/\sqrt{12}$ and so, in dynamic applications where there is little correlation between the error and the input signal, it is referred to as 'quantization noise' and has a magnitude of:

$$Q_n = q/\sqrt{12} \text{ rms.} \quad (1)$$

2.4 Differential non-linearity

Differential non-linearity (DNL) is a measure of how individual steps may be in error (for example if comparator bias is incorrect). It is the difference between the ideal step position (in analogue terms) and its actual position. A good ADC will hold this error to $q/2$ (Fig. 4).

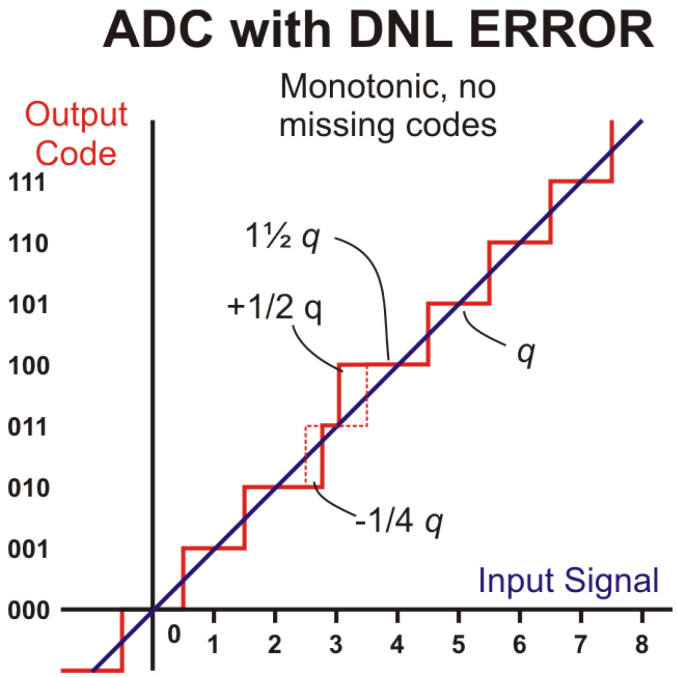


Fig. 4: ADC with DNL error. DNL is defined as the difference between ideal and actual step width

2.5 Missing codes

If the DNL exceeds $q/2$ it is possible that a missing code can occur, i.e. the converter 'jumps' between non-adjacent codes (Fig. 5).

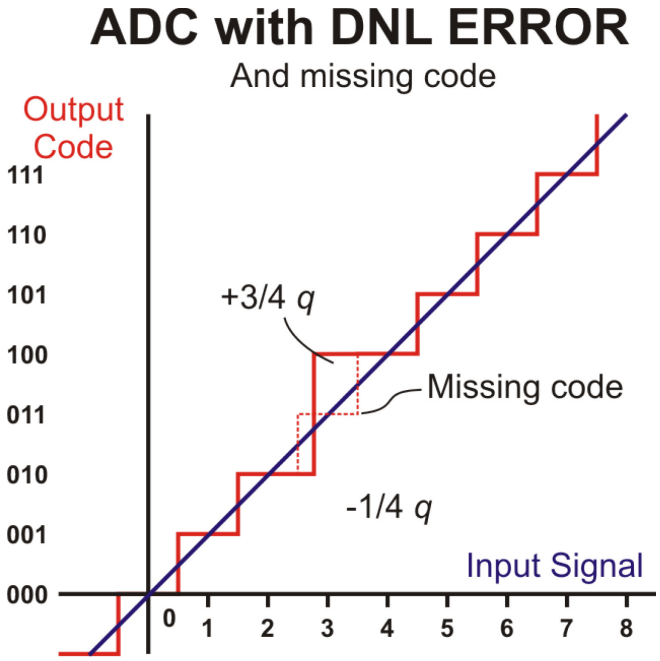


Fig 5: ADC with DNL error and missing code

2.6 Non-monotonic

Non-monotonic literally means that two different analogue values that are separated by an appreciable increment can produce the same code and this may indeed happen (Fig. 6).

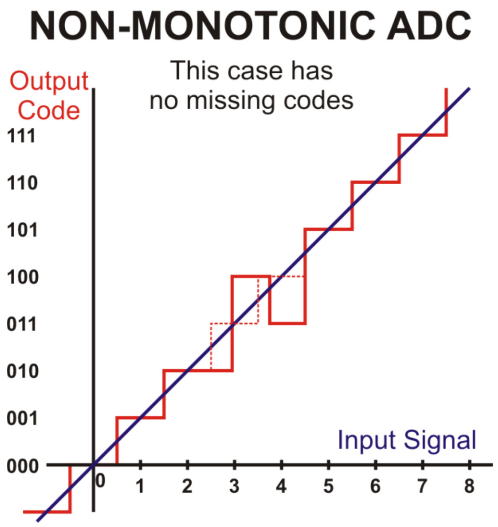


Fig 6: Non-monotonic ADC: this case has no missing codes. Non-monotonic is defined as having a negative differential in the output codes.

However, although the term 'non-monotonic' is still used it is better defined as a negative differential of code values for smoothly incrementing analogue values. The example is a special case, showing how this can happen without there being a missing code, although a missing code is a more likely result.

2.7 Integral non linearity

Integral non linearity (INL) can affect all types of ADC and DAC whereas DNL would not normally affect integrating types such as charge balance and Σ-Δ (delta-sigma). It is defined as the difference between the actual transition at any level and the ideal transition. It occurs where there is an accumulation of very small DNL errors over a range of steps or input signal. It is important to appreciate how it is specified because one can define the ideal transitions as standing on a straight line between zero and full scale endpoints or a 'best fit' regression line. In this case INL errors may be distributed symmetrically about a straight line rather than appearing at twice the magnitude, on one side alone (Fig. 7)

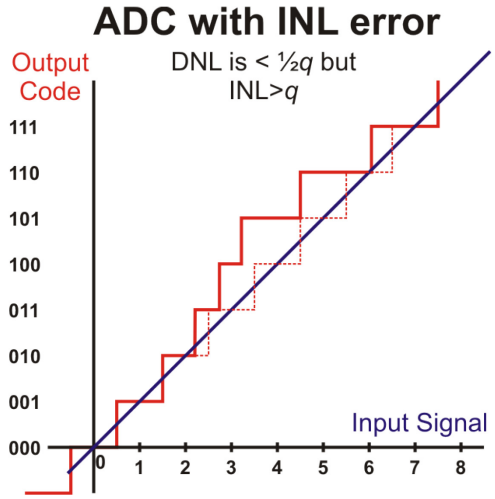


Fig 7: ADC with INL error: DNL is <1/2 q but INL > q. Defined as extreme deviation from ideal transition

2.8 Dynamic terms

ADC data sheets will often be written in terms of AC 'frequency-domain' specification and it is important to understand some of the terms used, even if the application is more 'time-domain' or DC related.

2.9 Signal to noise ratio

Signal to noise ratio (SNR) and the following terms assume that the ADC is to be used to digitize a sine wave set to an amplitude whose peak-to-peak value equals the maximum-to-minimum capability of the ADC. However, this is then translated to ratios of rms values. SNR is the rms ratio of the full scale sine wave to the total noise present, assuming that the quantization noise is random and uncorrelated with signal or other noise. It is a function of the frequency and amplitude of the signal and is therefore specified for a defined signal.

2.10 Spurious free dynamic range

Non-linearities and intermodulation products introduce harmonics and spurs into the output spectrum, usually observed through fast Fourier transform (FFT) conversion. The spurious free dynamic range (SFDR) is the range (in dB) between the fundamental and the highest harmonic or spur that occurs within the Nyquist range of ½ the clock rate of the ADC (or over a specified range). Clearly it too will be a function of the amplitude and frequency of the applied signal although the full scale amplitude previously described is usually assumed to give the best ratio.

2.11 Signal to noise and distortion

Signal to noise and distortion (SINAD) is commonly used but, whilst useful for an overall system specification, is less so to a designer choosing an ADC to use. It is the SNR but with the spurs and harmonics of the SFDR included and assumed to be an additional uncorrelated noise source. Clearly, when designing a system in practise, one needs to be able to distinguish between truly random terms and signal-dependent terms, especially if the system performs some sort of filtering or averaging that can reduce the effects of random noise but not of distortion.

2.12 Effective number of bits

Most IC manufacturers use the term effective number of bit (N_{ef} or ENOB) where DYNAD uses N_{ef} and IEEE 1241 uses 'effective bits', E. It is used to give a specification for an ADC's degradation in resolution when making a measurement where it, the ADC, introduces noise, distortion and spurs. It is thus related to SINAD and can be shown to be (or is defined to be):

$$N_{\text{ef}} = \text{ENOB} = \frac{(\text{SINAD} - 1.76)}{6.02}\,\text{dB}, \tag{2}$$

where SINAD is expressed in dB of full scale.

2.13 Oversampling

Oversampling is used to describe the operation of a converter where samples are taken at a rate higher than two times the input signal's highest frequency (the Nyquist rate) and some sort of result is obtained by combining these samples. Generally it is the ratio of the sampling rate to the converter's maximum useable bandwidth. In reality an oversampling ADC is one in which a number of samples of the analogue signal are combined to give a better result (usually higher resolution) than any one sample provides. In order to do this there must be variation in the result for each sample of a perfectly steady signal and this is ensured by inherent or added noise, usually called 'dither'.

3 Types of ADC and DAC

3.1 Flash ADCs

Flash ADCs at their simplest can be made with a simple comparator, which senses a voltage threshold and drives a logic level; '1-bit'. More generally they are made with many such arrangements in parallel, each comparator set to a different threshold. The threshold normally divides a full-scale range by the number of comparators. Bandwidths into the GHz are possible (Fig. 8).

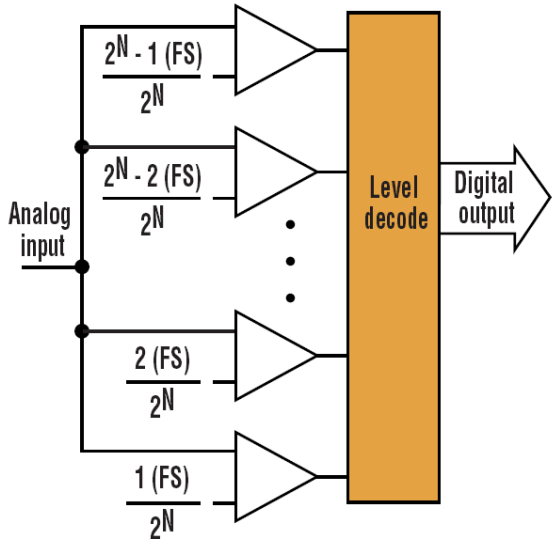


Fig 8: Flash ADC architecture. FS, Full-scale analogue input voltage

Modern high-density processing is accomplished mainly in low-voltage technologies that require even greater accuracy and lower noise of comparator thresholds. This, of course, makes the processing and testing expensive.

The Flash ADC is almost unique in not incorporating a DAC in an internal loop. It is this that makes it particularly fast, with a very direct path from analogue input to digital output. It is the workhorse component, at varying resolutions, from 1 bit to 10 bits, within other types of ADC architecture, particularly 'pipeline' and Σ-Δ (where it is often '1 bit').

3.2 Pipeline ADCs

Pipeline converters retain most of the bandwidth capabilities of Flash but at higher resolution at the expense of increased sample delay, called latency (Fig. 9).

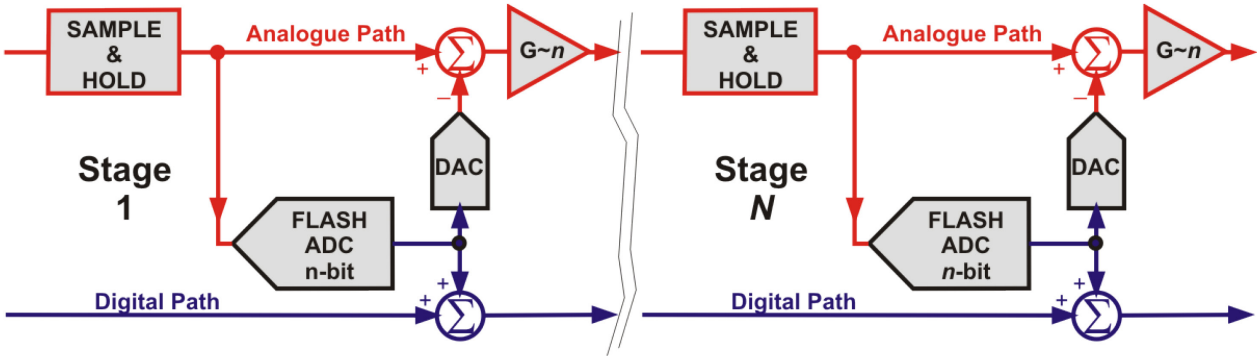


Fig 9: Principle of pipeline ADC with n^N bits

They do this by incorporating a number of stages of Flash ADC and DAC in series. This is the pipeline and each stage converts, say, *n* bits in the Flash but then uses the DAC to subtract the actual Flash output, converted to analogue from the incoming signal, to derive an analogue remainder. This is amplified by *n* and fed to the next stage to be digitized. Broadly speaking, with n stages, the resolution is n^N but a large degree of self-adjustment has to be incorporated to prevent DNL errors so some resolution is 'wasted' at each stage. It should be evident from this description that the bandwidth can be virtually as high as the Flash converters involved but that there is an addition of delays through the stages—thus leading to considerable latency or group delay.

3.3 Successive approximation register ADCs

Successive approximation register (SAR) ADCs have been around for a long time; even the earliest DVMs used them (Figs 10 and 11).

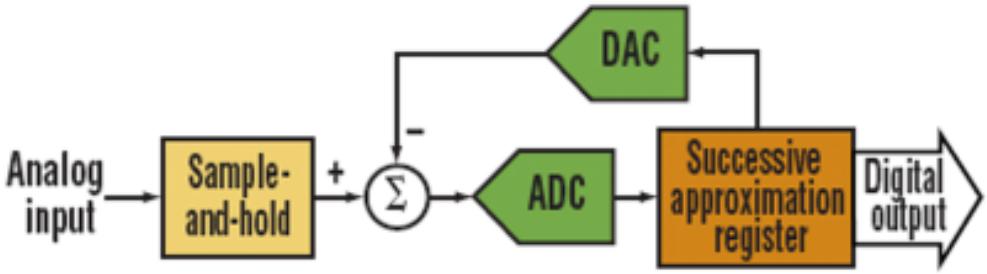


Fig. 10: SAR architecture

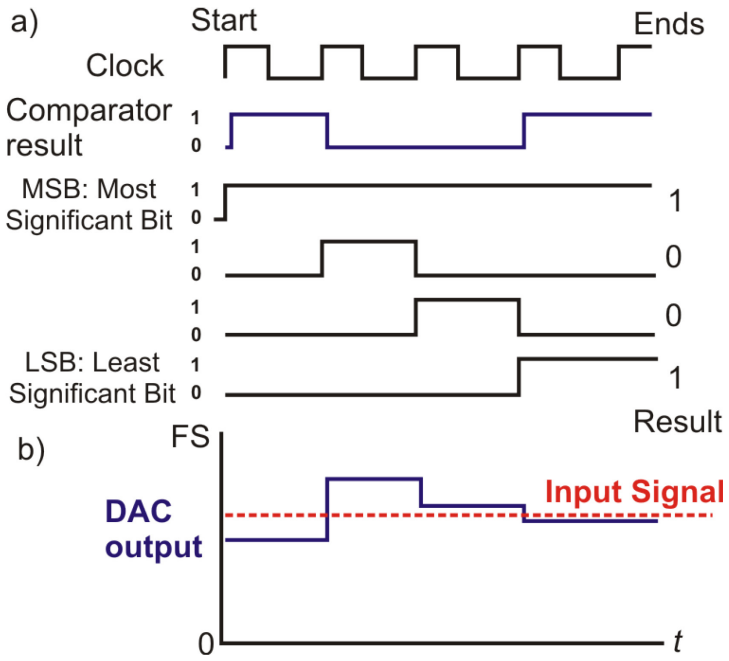


Fig. 11: a) SAR logic sequence. b) SAR DAC convergence

The SAR converter operates by testing whether or not the input signal is above or below thresholds set by the ladder DAC. Generally, one starts at ½ of full scale to determine the MSB then sets either ¼ or ¾ scale to determine the next bit and so on. In this example, the ADC in Fig. 10 is simply a comparator, but more complex arrangements can incorporate a Flash converter.

3.4 Charge balance, dual slope

The dual slope converter is the most commonly used of the charge balance type. For low-frequency measurement, in simple DVMs and panel meters, it is very cost-effective indeed and well matched to DC measurement with integral noise reduction.

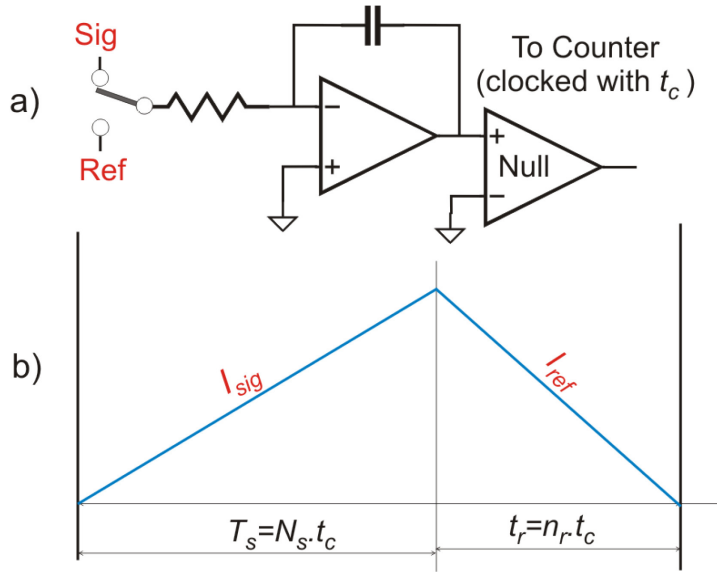


Fig. 12: Dual Slope Integrator, a) schematic, b) integration waveform

Basically it utilizes the unknown signal to be measured to charge a capacitance for a pre-set time. It then discharges *through the same components*, with a known reference signal and measures the time this takes. The analogue accuracy is thus dependent only (to a first order) on the reference. Compare this to SAR which also needs as good a reference but in addition a highly critical ladder network of precision resistors or capacitors.

3.5 Charge balance, multi-slope

A further refinement that can be used to get something like an order improvement in speed and/or resolution is used in 'top end' DVMs like the Agilent 3458 and Fluke 8508A. Here, in order to improve resolution, reduce the effects of null detector noise and allow smaller integration capacitors to be used, quanta of reference current is removed concurrently with the signal charging. As long as charge balance is maintained and 'accounted for' by the logic any such arrangement is valid.

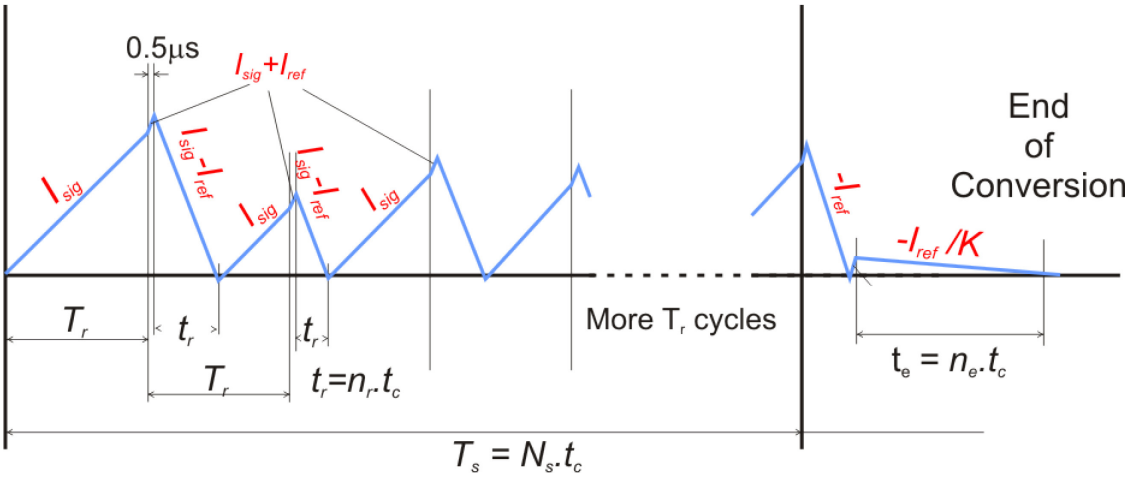


Fig. 13: Multislope charge balance integrator sequence

As previously stated there is a large discrepancy in the custom and practise between specifying DVMs and ADCs. Table 1 expresses the specifications of top-end DVMs in a typical ADC format.

Table 1: DVM and ADC specification comparison

Specification	DVM data-sheet specification	ADC 'bit' specification
Nominal resolution	±8½ digits	28+ bits
Real (2 σ) resolution	±7½ digits	24+ bits
Integral non-linearity (INL)	0.1 ppm (1×10^{-7})	23 bits
Differential non-linearity	No specification. 'Perfect'	28 bits

3.6 Δ-Σ, delta-sigma, often called Σ-Δ sigma-delta

Delta-sigma (Δ-Σ) is often interchangeably called sigma-delta (Σ-Δ) This conversion technique is usually thought of as a 'charge balance' technique but this is misleading. It is true that over very long periods of time it does maintain a charge balance in its integrator *but* it produces valid, accurate results much faster than would be expected from charge balance equations. In fact, for high resolution, this is several *orders* faster. For example, the CERN Σ-Δ converter produces *independent* 1 ppm resolution conversions in only 1000 clock cycles where dual slope would need 1 000 000. See Ref. [4].

Perhaps the slow take-up of this technology for DC and Low Frequency (LF) metrology has been because this is very difficult to explain with time domain arguments. The frequency domain proponents have no problem! See Refs. [5, 6].

The converter shown in Fig. 14 utilizes a 1-bit DAC (which is very accurate in spite of its low resolution) and the action of the feedback loop is to drive the DAC with a bit stream that balances the incoming signal. Confidence in applying negative feedback-loop theory explains the operation in the time domain!

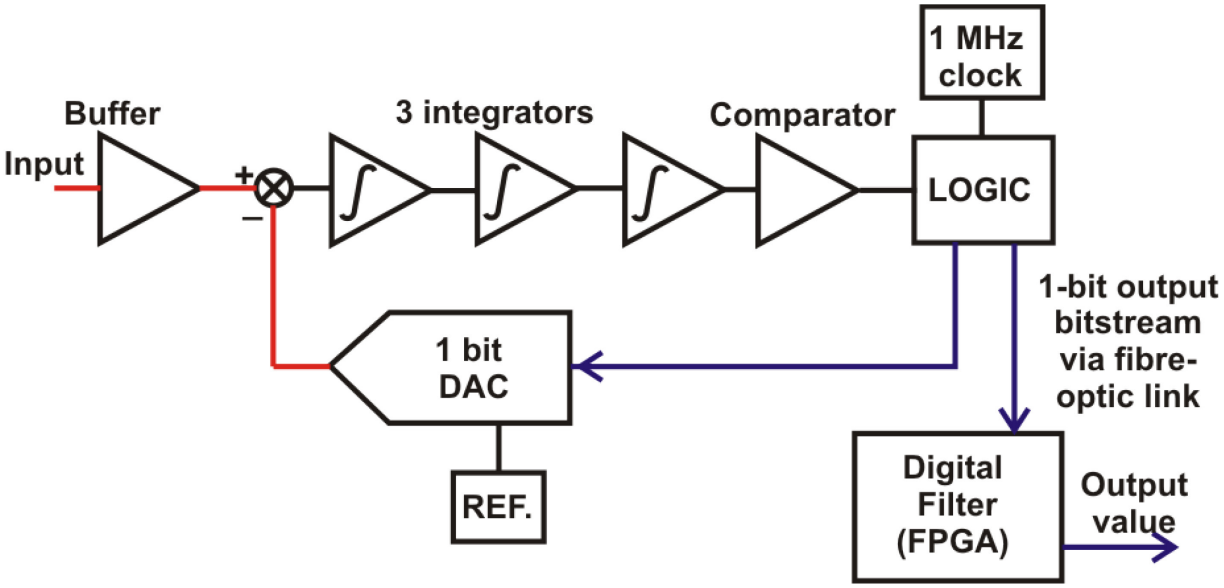


Fig. 14: The CERN 1-bit converter

The cumulative gain of the integration stages, forming the modulation filter, is very high indeed, in CERN's case in the order of 4×10^{11} at 10 Hz! Clearly, at 10 Hz there can be no significant error at the summing junction.

The cleverness is in achieving this within a loop while maintaining loop stability and, in effect, this is accomplished by feed-forward in the modulation filter, i.e. the integrators. DAC versions of this arrangement, where the input is a bit stream and there is analogue feedback around the loop, are probably

the most commonly produced data conversion components of all. They are the basis of the '1-bit' DAC in CD players and have been shipped in millions of units.

Figure 15 shows a simulation result for a 1-bit architecture that uses a digital 4 × 25 stage rolling average filter—it thus obtains all of its information in 100 clocks where dual slope could only achieve 1% resolution. The simulator clearly shows that the resolution far, far exceeds the 'simple' first-order dual slope capability, and further increased digital filtering gives vast improvements in real resolution.

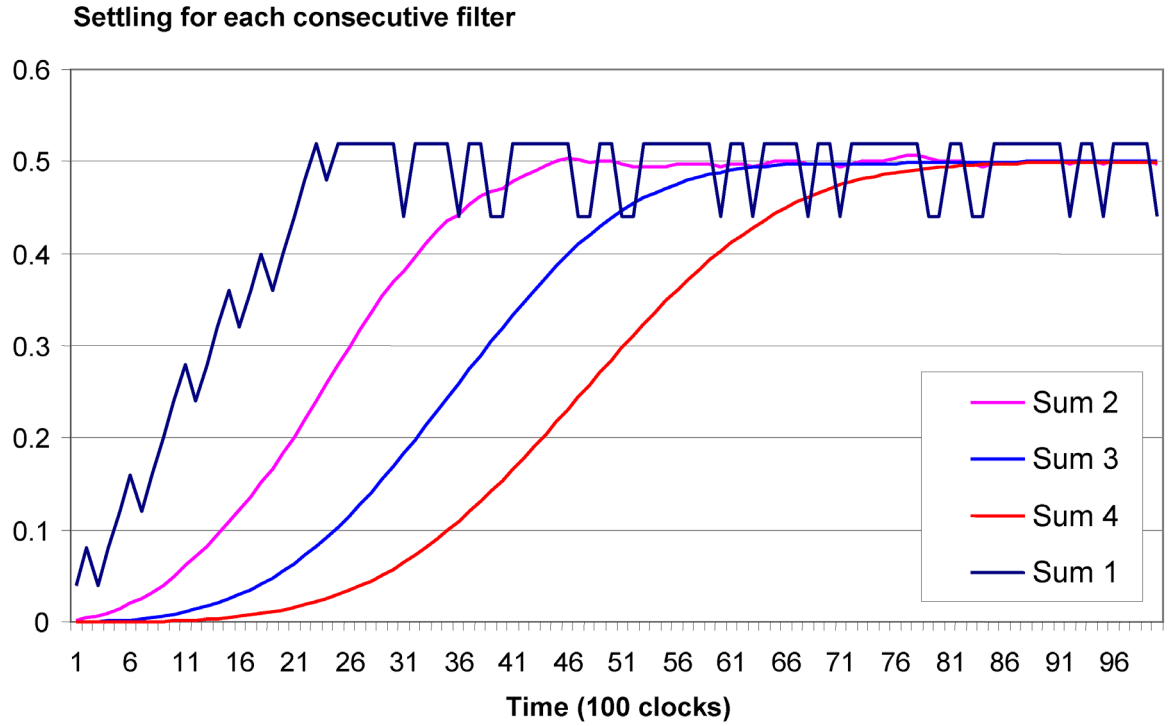


Fig. 15: Delta-sigma 1-bit third-order 4 × 25 average filter settling. Note that resolution in 100 clocks is better than 0.1%.

3.7 Characteristics of Δ-Σ

Since Δ-Σ seems ideally suited to accelerator DC and LF work, it is useful to look carefully at its characteristics, both good and bad.

Firstly, using IC products from 'merchant semiconductor' companies may give some surprises. Since suppliers are mainly aiming Δ-Σ converters at AC applications, both specification and performance is tailored for this—however the volume of production brings down the cost.

Bandwidths are usually limited but, because of the very high sampling rate, anti-aliasing filters are simple. The multi-stage digital filters allow very high data rates but there are long delays and much of the data is redundant. Clearly, a newly applied signal must replace all data present from the previous one, and this typically takes as many clocks as there are filter stages. However, it is possible to 'look ahead' and take data from early stages of the filter concurrently with the final, more filtered, data. This, of course, can be used for feed-forward in digital control loops.

IC manufacturers promote their devices as, say, '24 bit' or '22 bit' where generally this is the resolution at the 1 σ noise level and with the longest integration times (slowest speed) set, i.e. it is the SNR expressed in bits under the most favourable conditions. Also linearity (INL) is seldom better than 5 ppm (or 18 bits).

There are some problems that are unique to Δ-Σ. Normally, because of the very high loop gain, there is sufficient noise that a sort of chaotic behaviour results and there are no systematic errors in the output due to loop operation. (Of course, there are other systematic errors in, for example, the DAC accuracy.) However, it is well known that certain bit patterns in the feedback loop can be favoured and very low frequency, resonance-like, behaviour results. These conditions, in the frequency domain, look like very low frequency tones and they tend to be common when operation is near zero and the pattern therefore tends to be near symmetric. They are therefore called 'idle tones'. They are, at least in part and perhaps totally, due to unwanted feedback paths (remember how high the loop gain is). They tend to show up more in single chip devices where modulator and digital filters are in the same device.

Of a similar nature and perhaps considered as a 'zero-beat' idle tone, is a characteristic called a 'sticky zero', a hysteresis condition where there is a tendency to lock at zero until the signal is sufficient to overcome the 'glue'—an amount greater than the theoretical resolution. Again, great care in preventing unwanted loops between analogue and digital seems to prevent this.

3.8 Choosing the best ADC for the job

Table 2 gives relevant performance against possible requirements. The relative merit scores cannot be taken as correct for all devices under all situations but do at least give an idea. Probably, if one looks at the introduction of new devices from IC manufacturers it would be pipeline and Δ-Σ that have become the most prevalent in recent years.

Table 2: ADC type performance comparison

ADC type characteristic	Flash	Pipeline	SAR	Charge balance	Sigma-delta
Throughput	Excellent	Very good	Good	Poor	Fair
Bandwidth	Excellent	Excellent	Very good	Very poor	Fair
Resolution	Poor	Good	Very good	Excellent	Excellent
Latency/Hz	Excellent	Fair	Very good	Poor	Fair
Linearity/bit	Very good	Good	Fair	Very good	Very good
Multiplexing	Excellent	Poor	Very good	Fair	Poor
Other	Power! Cost	Very fast clock	DNL stability?	DC only	Easy anti-aliasing

4 Choosing the right specifications

This paper has discussed the relative merits of different architectures and pointed out some specification pitfalls. There remain some aspects of system integration that are not always apparent.

- Many devices have internal references that look to save an external component but beware—internal references are usually of the band-gap type because of the low voltages available. Internally, a band-gap reference is derived from a very low voltage; 60 mV is common and thus is very noisy, particularly with 1/*f* noise. Compensated Zeners are at least an order better than band-gaps.
- The resulting zero performance is then dependent on the reference and internal DAC.
- Ensure that the device you choose produces overload codes and flags that your system can handle—not all are user-friendly.
- Remember that INL is often *orders of magnitude worse* than quoted 'bit specs' and even if the target application system can correct for this there is usually not a specification for stability of INL.

4.1 Application problems

Assuming that an application system is designed with care and perhaps verified with simulation there is still likely to be a 'first time round' problem: probably noise. Noise problems are unlikely to show up in simulation and are very difficult to predict—experience suggests the following:

- use ground planes;
- 'bury' HF traces between planes on inner PCB layers;
- if possible make long-path HF signals differential and low voltage level;
- use common mode choke;
- think in terms of current paths—where does HF current flow?
- make signals 'flow' smoothly through the system;
- don't forget that sampling can alias HF noise and bring it down to the frequency of interest;
- HF connects ADC analogue and digital grounds on a plane or with capacitors between planes.

At low frequencies it can also be useful to:

- use 'star points' to control current paths;
- remember that 1/*f* noise cannot be averaged out totally and becomes a limit to achievable performance;
- use chopper stabilization to overcome drifts and 1/*f* noise in amplifiers. With the availability of suitable components it is now cheap and simple to do so;
- prevent differential temperatures from being developed across sensitive circuit areas, i.e. prevent heat flow.

4.2 An application example

A very high performance ADC has been developed, see Fig. 16.

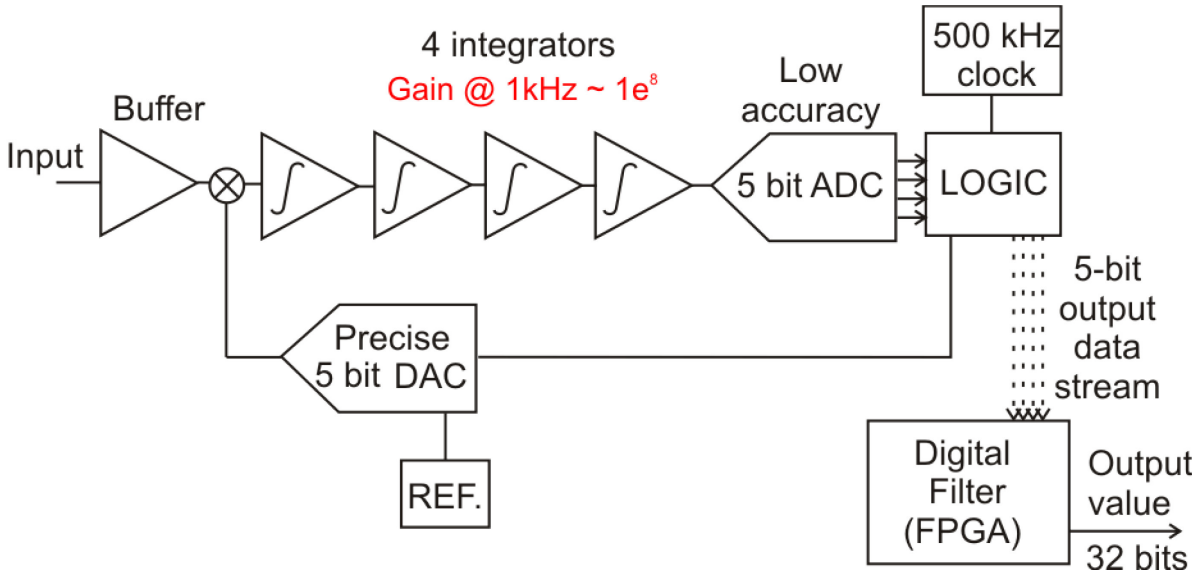


Fig. 16: A very high performance Σ-Δ ADC

In this example the 1-bit DAC is replaced with a 5-bit pulse width modulation (PWM) DAC and the output comparator replaced with a 10-bit pipeline ADC of which 5 bits are used. This architecture can achieve '28-bit' performance in resolution and 24 bits in linearity.

In order to achieve 5-bit resolution of the PWM at up to 500 KHz it is necessary to clock the pipeline ADC at 20 MHz. We thus have the difficult combination of 20 MHz clocking on the same PCB near to where 100nV DC performance is needed!

Figure 17 shows the PCB layout arrangement chosen, about half of the full size.

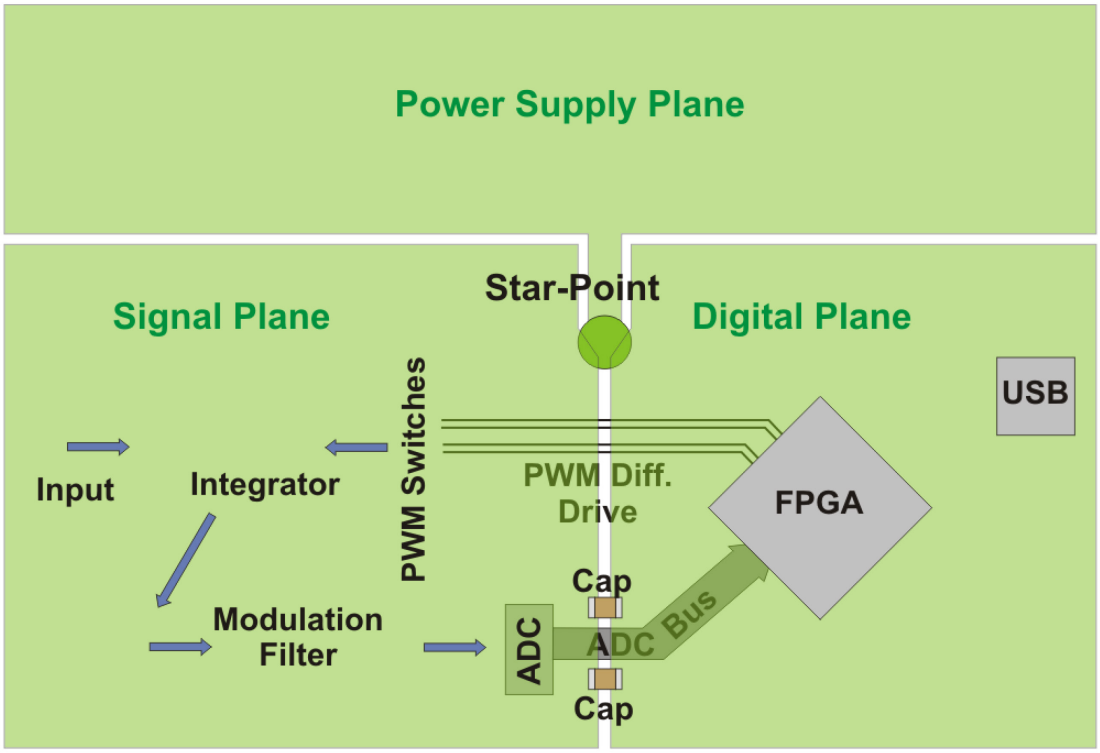


Fig. 17: Practical board layout

The PWM drive (with sub-ns edges) is passed from the field-programmable gate array (FPGA) to the analogue section of the circuit (the signal plane in Fig. 17) with differential signal traces (and indeed, the analogue switching is differential). A 'star-point' localizes LF currents and prevents those in power supply and digital planes from causing voltage drops in the signal plane.

This arrangement can be considered as a good example of any high-performance ADC application. Currents are controlled or 'steered' by the use of different ground planes, and circuitry is arranged for even current flow. In fact, the above PCB had a problem because signal-related ground currents could feedback from the output of the modulation filter to the PWM switches and integrator, causing idle tones and sticky zeros. The solution was to split the ground plane between these areas with a slot in the PCB. Furthermore, the sampling ADC drives very fast transient currents into the input capacitance of the FPGA and the two caps are fitted to 'encourage' local HF current loops rather than letting the return current pass back through the 'star-point'. Always remember to think about where the currents flow whether they are LF signal-related or HF with the ability to cause interference noise. A later version included analogue isolation between the modulation filter and the sampling ADC with the ADC placed on the digital plane.

5 Finally, the future—cryogenics?

The steering magnets at CERN and in many other accelerator projects are cryogenic. Much fundamental metrology is now based on quantum physics operating in liquid helium. Why not put some of the measurement in the cryogenic environment? Figure 18 is a suggestion and has been in operation at the UK's National Physical Laboratory.

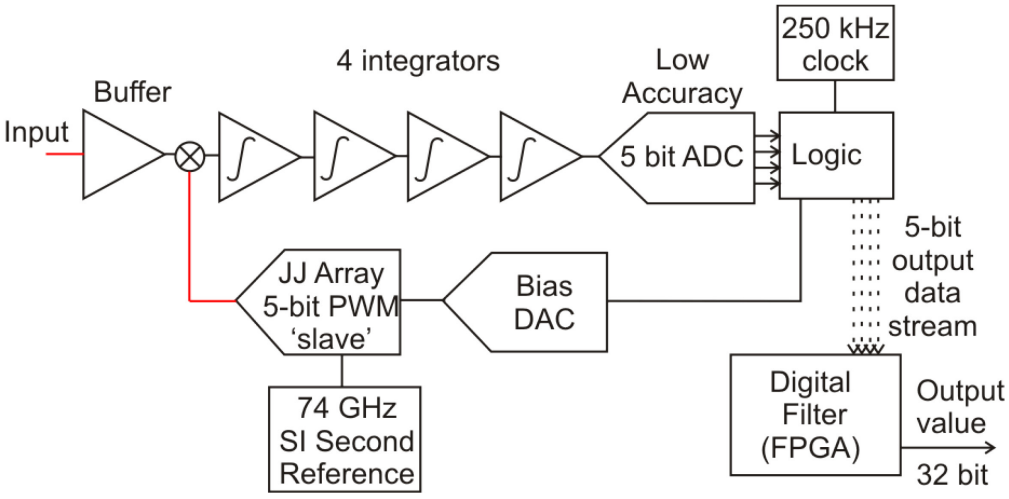


Fig. 18: Integration of Σ-Δ modulator with Josephson junction array (JJ)

Its operation is quite simple—the bias DAC is a two-level PWM generator that turns ON and OFF precisely the bias to the Josephson Junction (JJ) array. The operation of the JJ is to lock the amplitude of the resulting pulse to a quantum level dependent only on fundamental constants and on the SI second. See Refs. [7, 8]. Sadly, the speed with which the array could be switched was limited by the capacitance and delays in the JJ drive electronics but with further development could become a 'quantum voltmeter'.

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There is also much valuable material on many semiconductor manufacturers' web sites.

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Controls and Interfaces

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Abstract
Reliable powering of accelerator magnets requires reliable power converters and controls, able to meet the powering specifications in the long term. In this paper, some of the issues that will challenge a power converter controls engineer are discussed.

Keywords
Power converters; regulation; control; reliability.

1 Introduction

Power converter control has moved more and more into the digital domain. As a result, the choices of control hardware have evolved extremely rapidly, and the potential performance of that hardware has expanded exponentially. Exploiting the potential of the hardware has fallen on software and programmable logic developers, with the result that the effort needed to develop converter control software can now surpass the effort needed to develop the hardware.

The diversity of potential hardware solutions means that it is not possible to proscribe a ‘right way’ to approach the control of converters. Instead, this short paper introduces some of the topics that should be considered to meet both performance and reliability targets. It will focus in particular on the control of continuously regulated power converters, rather than fast pulsed converters.

2 Defining the requirements

It is obvious that finding a good controls solution starts with defining the problems to be solved. This can be surprisingly difficult. At its most basic, the powering of an accelerator will involve a number of circuits, mostly involving magnets, but some may be providing high voltage for RF klystrons or other RF devices, or electrostatic elements for low-energy beams. Obviously the power engineers need to know the required rating of each converter, but for the controls a lot of additional information should be captured for each circuit, including the following.

- What will be the regulated signal: voltage, current or field?
- How is the reference of this value defined?
  - DC (e.g. for storage ring or Linac circuits).
  - Function of time run on demand (e.g. for non-cycling accelerators such as the Large Hadron Collider (LHC)).
  - Function of time run by a cyclic timing system (e.g. for cycling accelerators such as the CERN Proton Synchrotron (PS)).
  - Calculation in real-time based on an outer regulation loop (e.g. orbit or tune).
- How accurately must the value be controlled? It is important to distinguish between absolute accuracy, reproducibility, and stability. These are treated in more detail in Ref. [1].

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– What are the rate of change and acceleration limits?

From this you can define the requirements for the timing system, the analogue measurement system, and the regulation. This is not simple and will take time. Ultimately, this will lead to the key requirements of the controller hardware, including:

– the regulation rate;
– the measurement rate;
– the processing power;
– the noise and resolution of the analogue acquisition system;
– the interface for sending the reference (voltage and/or modulation) to the power converter.

2.1 Scalability

A very important factor in the design of the controls is the scale of the system. If you have ten circuits then an elaborate automatic configuration management system is not justified. Once there are 100 circuits, managing them individually will start to become time-consuming; and once a system has more than 1000 circuits, then automatic management tools are mandatory.

The calibration of the analogue measurement components will be important, particularly for the main circuits of an accelerator, which are usually the most demanding of accuracy. If an analogue component such as an analogue to digital converter (ADC) or direct current–current transformer (DCCT) is replaced, a method is needed to ensure that the control of the circuit can continue to meet the specification after the intervention. This can be manual for a small system, but for large installations an automatic calibration system is highly desirable.

3 Converter controls reliability

It is vital to remember that getting all of the circuits to work according to the specification when the facility is commissioned is only part of the challenge. It is equally important to keep them working with the required reliability for the lifetime of the facility. For this challenge, the mean time between failures (MTBF), mean time to repair (MTTR), and the scale of the system are all important. The bigger the system, the more attention should be given to reducing the MTBF and MTTR.

3.1 Hardware reliability

It is obvious that the MTBF of the global system will depend on the MTBF of the controller hardware. This is too big a subject to treat in detail in this short paper, but experience shows that once early failures have been resolved, control electronics can achieve remarkably high levels of reliability. One million hours MTBF per controller has been achieved at CERN; however, to get to this level requires attention to every aspect of the design and production (and some luck). For more information about practical reliability, consult the Bibliography. Here are some points to keep in mind.

– Use only the best quality connectors.
– Avoid the need for wiring by using circuit boards to link circuits.
– Design for test and, if you expect to manufacture more than a hundred or so units, build test hardware at the same time. Base your test hardware on standard off-the-shelf components, such as PXI cards. If your device is hard to test then it is probably too complicated and should be redesigned to be more modular.
– Avoid fans if possible, while keeping the operating temperature of components below 50°C. If fans have to be used, consider using a temperature-based controller so they only

run as fast as necessary. Choose fans with the highest MTBF you can get and try to mount them so that the axis of rotation is vertical. Monitor the temperature in the controller and have a warning threshold. Consider preventative maintenance by replacing all of the fans once they have reached around 70–80% of their rated operating life.

- Pay close attention to electromagnetic compatibility (EMC). Follow best practice for grounding and carry out burst tests to see if the required immunity has been achieved. Use relays and opto-couplers or optical fibres for long-distance signals, and design for the worst-case over-voltages on converter-related signals in the event of an earth fault on the magnet circuit.
- Use standard protocols, cables, and connectors.
- Avoid radiation areas if at all possible. If you have to design electronics to work in radiation, then allow a lot more time and money for their development and get expert advice. See Ref. [2] for more information about this.
- Avoid potentiometers and other adjustable components.
- Avoid electrolytic capacitors, and overate passive components for power and voltage.
- Don't miniaturize unnecessarily. Use the largest passive devices that fit and the biggest pad sizes on active devices. Only use ball grid array (BGA) packages when unavoidable. Include pads to mount test connectors for a logic analyser for use during the development phase.
- Exploit programmable logic and make it easy to update. For large installations, allow the logic to be reprogrammed over the network.
- Don't use programmable digital circuits just for the sake of it. If a function can be done simply with an analogue circuit, then this will need less effort to maintain. All software (including programmable logic) has a major overhead for maintenance in the long term.
- If the controller incorporates multiple circuit boards, enclose the assembly in a metal cassette.
- Plan for the obsolescence of the hardware and the development systems. How will you compile the logic and software in 25 years? Investigate virtual machines before it is too late.

Apart from good design, the operating conditions can impact reliability.

- Do not trust commercial power supplies. Either design your own or use a pair of supplies with monitored redundancy, or both.
- If possible, keep the electronics powered and warm all the time, reducing the thermal cycles to which the hardware is subjected.
- Keep powered spare controllers in the vicinity of the operational systems.
- Keep the operational environment clean of dust, with temperature and humidity close to nominal, and protect the electronics from water damage in the event of leaks from water-cooled cables or components in the power converter.
- Use halogen-free cables to reduce the impact of fire damage.
- Incorporate a means to remotely identify, and hence track, individual parts.
- Predict the expected failure rate of components, and put in place the means to track failures and repairs. This should be used to determine real-world failure rates and to

identify new failure modes, allowing preventive actions to be taken in the case of unexpectedly high failure rates.

3.2 Converter spares policy

The power engineers will need to address the same issues of MTBF and MTTR when designing or specifying the power converters and when defining the spares policies. Different approaches may be taken according to the types of converters used. Below are two examples that have an impact on the specification for the controls.

3.2.1 Converters made from modular components

In this approach, large converters are made from multiple sub-converter racks containing multiple standard modules. The modules are light enough that one or two people can swap a faulty unit with a spare within a few minutes. In this case, a circuit can only be powered by one converter, but most failures will be in the power modules which can be quickly swapped. The controller will only ever be responsible for the one circuit, so addressing and configuration are static.

In this case, the challenge for the control system is to accurately identify which module needs to be replaced in the event of a fault. For this, a very reliable system to capture the first fault must be deployed. In the case of the LHC power converters, the power engineers adopted an $n + 1$ redundancy policy for this class of converters, so they all have one more sub-converter than those required to deliver the nominal current. The low-level converter electronics can compensate for the loss of a sub-converter in real time by increasing the current supplied by the others.

However, sometimes this may not work and the trip of a sub-converter may result in a cascade of trips in the other sub-converters. The LHC ATLAS experiment's toroidal field magnet converter has eight sub-converters, each containing six modules. If one module is unreliable and trips off randomly every day or so, and if this results in tripping the whole converter, then this will quickly become a problem unless the controls can accurately identify the faulty module.

This means that the first-fault logging must not only identify the first fault within a sub-converter, but also the first sub-converter to trip. This may require time-stamping of the faults with a resolution of the order of 10 μs.

3.2.2 Monolithic converters

For large monolithic converters, the power engineers may install one spare converter in an area, to cover a number of operational converters. In the event of a failure, the circuit cables are patched to the spare unit, which allows the faulty converter to be repaired later.

The spare converter might have its own controller, in which case it must take over the address of the controller of the failed converter. This can present some interesting configuration challenges if the spare converter is not exactly of the same type as the failed unit. Alternatively, the controller from the failed unit might be patched or moved to control the spare.

Whichever approach is adopted, the probability of mistakes by the team making the intervention should be minimized by reducing the complexity of their task.

3.3 Addressing the controller

The controller addressing scheme will depend upon the network architecture. However, it is reasonable to assume that the controller will be made from components that can be exchanged in the event of failure. So this raises the question of how a controller knows its address. This might be a MAC address on Ethernet, or a fieldbus address if a fieldbus is used.

The new controller's address could be configured manually by the team who are performing the intervention, perhaps by using jumpers or switches. But this is error prone and can easily result in two controllers appearing on the network with the same address. This almost inevitably causes disruption to the system and can be hard to diagnose, so there is a strong motivation to avoid this kind of error.

A preferred approach is to encode the address in some passive device that gets plugged onto the controller. This might be the network connector or it could be in a separate dongle. In either case, a simple circuit board can encode a digital value with copper tracks so that, once soldered, a failure of the dongle is highly improbable. Alternatively, an I^2C electrically erasable programmable read-only memory (EEPROM) (or equivalent) could be used, but being an active device it will have a lower MTBF.

3.4 Analogue calibration

The conversion of an analogue signal into a scaled value inside the controller requires two distinct pieces of information:

- the nominal scale factor;
- the calibration error.

There is no avoiding the need for the nominal scale factor but different approaches are possible for the calibration error. In one approach, the analogue hardware can be designed with calibration components such as potentiometers. In this way, the calibration errors can be reduced to within the specification and the software can consider the measurement to be perfect.

While this simplifies the software, it puts a significant burden on the team responsible for keeping the analogue measurement devices calibrated and, in the case of potentiometers, it increases the chances of component failure and error.

A preferred approach is to avoid all adjustable components and to accept that all of the analogue measurement devices will have calibration errors. Provided that these errors can be measured, then they can be compensated in software. If such an approach is adopted, it also opens the possibility to compensate non-linearity and temperature effects.

If a known and trusted reference signal can be selected automatically then the software can measure the calibration errors itself. If not, then calibration of an analogue measurement device such as a DCCT might be done on a test stand. The measured calibration errors can then be stored for later use by the controller.

Where to store this calibration data is a key question. For a few circuits this could be entirely manual with the values written in a notebook and entered into the controller by hand. Obviously this is impractical for a big system with hundreds or thousands of circuits. An alternative is to store the calibration data in a non-volatile memory inside the device. This is a simple concept and can be effective for small- to medium-sized systems.

For large systems, using a central database is recommended. In this case, a way to identify the measurement device is needed. Ideally this should be machine-readable so that the controller can automatically identify the connected devices and request their calibration data from the database. Although this is a significant investment in terms of software development, it is an important step towards the goal of full automatic configuration.

3.5 Automatic configuration

For large systems, accurate automatic configuration of the controllers is hugely important for the reliability of the whole system. It is a worthy objective to avoid all manually configurable components such as switches and jumpers in the design of the hardware.

All configuration parameters can be stored centrally in a database. These parameters fall into three categories.

- Parameters associated with an individual component. For example, the calibration errors for a particular DCCT or ADC.
- Parameters associated with a type of a component. For example, the scale factor for a type of DCCT head.
- Parameters associated with an individual circuit. For example, the magnet inductance.

For the first category, individual components must be identified by the component type and a unique serial number. This is typically converted into a barcode that is stuck onto the component. For automatic configuration to be possible, the controller needs to be able to know the barcode of each attached component that has configuration parameters.

For the second category, the component type field from the barcode can be used to look up configuration parameters in the database associated with that type of component.

For the third category, the name of the circuit can be used to look up the circuit parameters. Obviously the control system needs to know the association between controller address and circuit name.

3.6 Software reliability

Converter control is a real-time problem, so many modern programming languages are unsuitable. The natural choice remains the low-level languages C and C++. Increasing processing power is making the real-time challenge easier to face, but bear in mind that embedded programming is time-consuming so, where possible, move the programming to a level where standard tools such as Linux (with real-time extensions) can be used. Please consult the Bibliography for recommended books on embedded systems programming.

It is obvious that software reliability is improved by adopting:

- a source code versioning tool such as git;
- a continuous integration tool such as Bamboo or Jenkins;
- an issue tracking tool such as JIRA or Trac;
- code reviews.

Unit testing may also help, but it has limits when programming real-time multi-threaded software.

With real-time programming, time is at the heart of everything, so invest in a way to record the time taken to execute every important part of the real-time code. This can be a simple min/max pair, or a histogram if the profile is significant.

4 Regulation

The core business of converter controls is (usually) the delivery of the correct current in the circuit as a function of time. In special cases, the field in a magnet might be measured and regulated, or the voltage provided to power an RF generator or an electrostatic element in a beam line.

Numerous control strategies are possible, but two that have been widely adopted for accelerator power converter control are:

- digital implementation of a classical ‘analogue’ regulator such as a proportional integral derivative (PID) controller using state equations;

– digital implementation of a digital regulator based on the RST polynomial algorithm.

Each has benefits. The classical approach is simple for a non-expert to tune as the number of parameters is small, while the RST approach can provide excellent performance with a constant tracking delay (the time between the reference being set and the measurement arriving at the reference value).

4.1 Classical regulation

Many laboratories have developed digital controllers that have implemented PID regulators using classical state equations. In particular, the Swiss Light Source at PSI has developed both electronics and corrector power supplies that have been widely used at many light sources [3]. The digital signal processor (DSP) in the electronics implements the current regulator and pulse width modulation (PWM) without an intermediate voltage regulation loop. This has allowed a high bandwidth of more than 1 kHz for the corrector circuits, which has been valuable for the orbit feedback needed by light sources to stabilize the electron beam in the insertion devices.

4.2 The RST algorithm

The RST algorithm is becoming increasingly popular because of its performance and flexibility. The RST algorithm is defined in Eq. (1),

$$\sum_0^n\{Act_i \cdot S_i\} = \sum_0^n\{Ref_i \cdot T_i\} - \sum_0^n\{Meas_i \cdot R_i\}\,, \tag{1}$$

where $i = 0$ corresponds to the current sample, $i = 1$ is the previous sample and so on. This notation was proposed by Landau [4]; however in many textbooks the R and S polynomials are exchanged. The application of the RST algorithm to power converter control is described in Ref. [5].

From Eq. (1), it is easy to see that if you know the new reference and measurement, you can calculate the new actuation, Act_0, if you keep the history of the previous n samples of the reference, measurement, and actuation,

$$Act_0 = \frac{\sum_0^n\{Ref_i \cdot T_i\} - \sum_0^n\{Meas_i \cdot R_i\} - \sum_1^n\{Act_i \cdot S_i\}}{S_0}\,. \tag{2}$$

Typically the actuation will be the voltage reference for an inner voltage regulation loop, but if the DC bus is very stable and the PWMs are very linear, then actuation could be the modulation reference directly. Either way, if the actuation is limited, it is easy to back-calculate the reference that, when combined with the new measurement, will result in this limited actuation when used in Eq. (2). This is given in Eq. (3),

$$Ref_0 = \frac{\sum_0^n\{Act_i \cdot S_i\} + \sum_0^n\{Meas_i \cdot R_i\} - \sum_1^n\{Ref_i \cdot T_i\}}{T_0}\,. \tag{3}$$

In this way the reference history can be kept coherent with the measurement and actuation histories. This is equivalent to the anti-windup feature of a traditional regulation algorithm.

The benefit of the RST equation is that any linear regulator up to order n can be implemented by choosing the appropriate RST polynomial coefficients. Simple PI, PID, or PII controllers can be implemented as well as more complex higher order systems, without changing the software. The challenge with the RST approach is the calculation of the coefficients. This cannot be done by hand and either requires an expert using MATLAB (or equivalent), or a library that encodes the knowledge of an expert for a particular type of load.

4.3 Circuit load model

The majority of the circuits in a typical accelerator are inductive and resistive. Figure 1 shows a generic first-order model that can cover most cases.

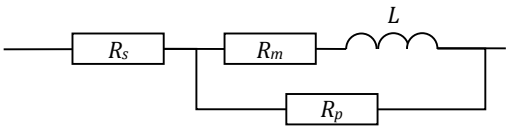


Fig. 1: Generic first-order inductive load model

There are three resistances in the model.

R_s – series resistance representing the resistance of the cables.

R_m – magnet resistance. This will be zero for superconducting magnets or circuits that do not contain a magnet.

R_p – parallel resistance. This is rarely used but in some circuits in which many magnets are connected in series, the parallel resistance is needed to damp out resonances.

The transfer function for this first-order model is presented in Eq. (4),

$$G(s) = \frac{1}{R_s + \frac{1}{\frac{1}{R_p} + \frac{1}{R_m + sL}}}. \tag{4}$$

The frequency response of the gain (current/voltage) has the classic first-order form presented in Fig. 2.

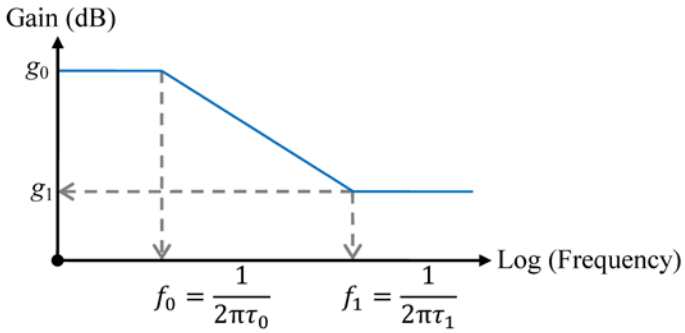


Fig. 2: Bode diagram for first-order load model

This response is defined by DC and high-frequency gains, g_0 and g_1, which can be calculated using Eqs. (5) and (6),

$$g_0 = \frac{1}{R_s + \frac{R_p R_m}{R_p + R_m}}, \tag{5}$$

$$g_1 = \frac{1}{R_p + R_s}. \tag{6}$$

The frequencies of the first-order pole and zero, f_0 and f_1, are defined by the periods τ_0 and τ_1, which can be calculated using Eqs. (7) and (8),

$$\tau_0 = \frac{L}{R_m + \frac{R_p R_s}{R_p + R_s}}, \tag{7}$$

$$\tau_1 = \frac{L}{R_p + R_m}. \tag{8}$$

For very large super-conducting magnets, the stray capacitance between coils can be significant (as discussed in the next section) and a different load model may be more appropriate.

4.3.1 Parallel resistance

If a circuit requires the parallel resistance to damp resonances, this may have an important consequence upon the control of the current in the magnet. The parallel resistor will allow some of the circuit current to bypass the inductor during transients.

Figure 3 illustrates the effect on the circuit current of this prompt response to steps in the voltage. It means is that for some time after each step in voltage, the magnet current will not equal the circuit current, which can be significant because it is the circuit current that the controller measures and regulates. It is important for the accelerator physicists to be aware of this fact, since they are interested in the magnet current.

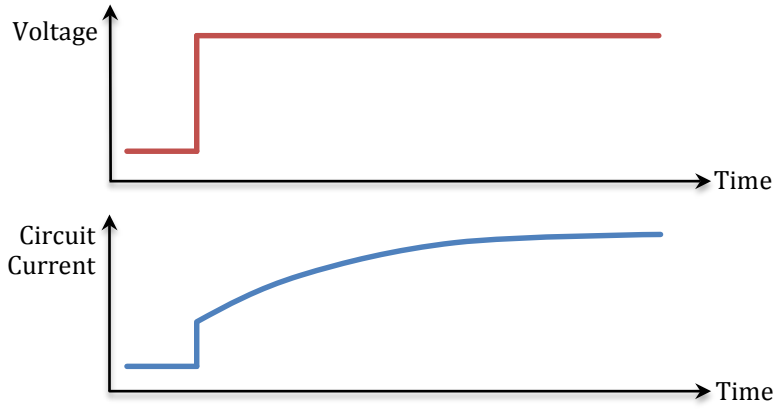


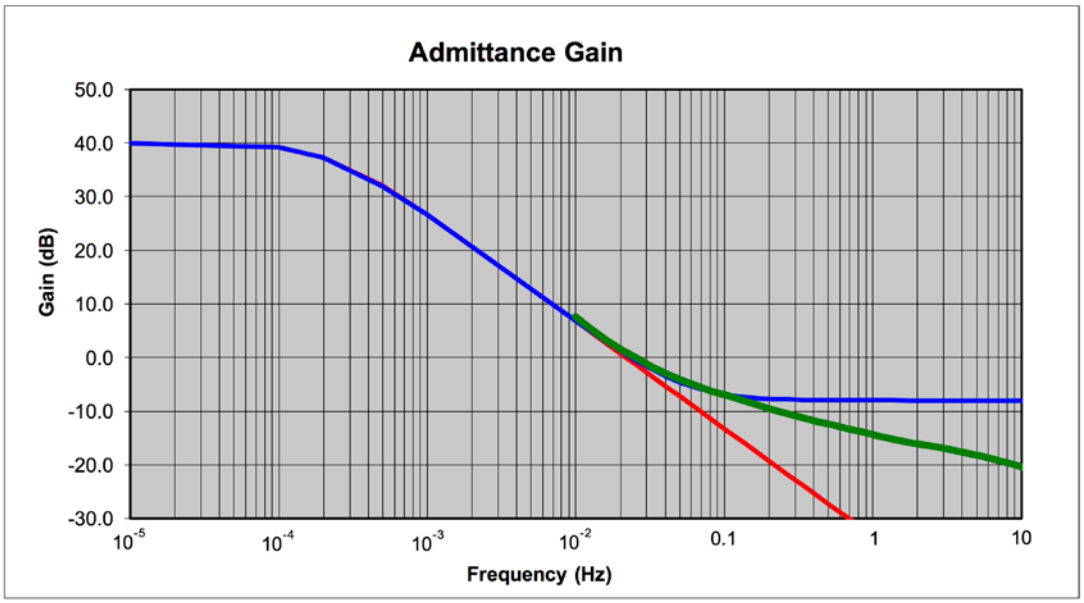
Fig. 3: The presence of a parallel resistance (R_p) in the load results in a prompt response in the current to steps in the applied voltage.

In the LHC, the main dipole and quadrupole circuits are the only ones that require parallel damping resistors. The characteristics of these circuits are given in Table 1. The key ratio is g_1/g_0, which are ~10^{-7} and ~10^{-6}, respectively. These circuits need to be regulated with ppm level accuracy, so it is fortunate that this ratio is very small. A lower value of R_p would have jeopardized the quality of the regulation of the magnet current.

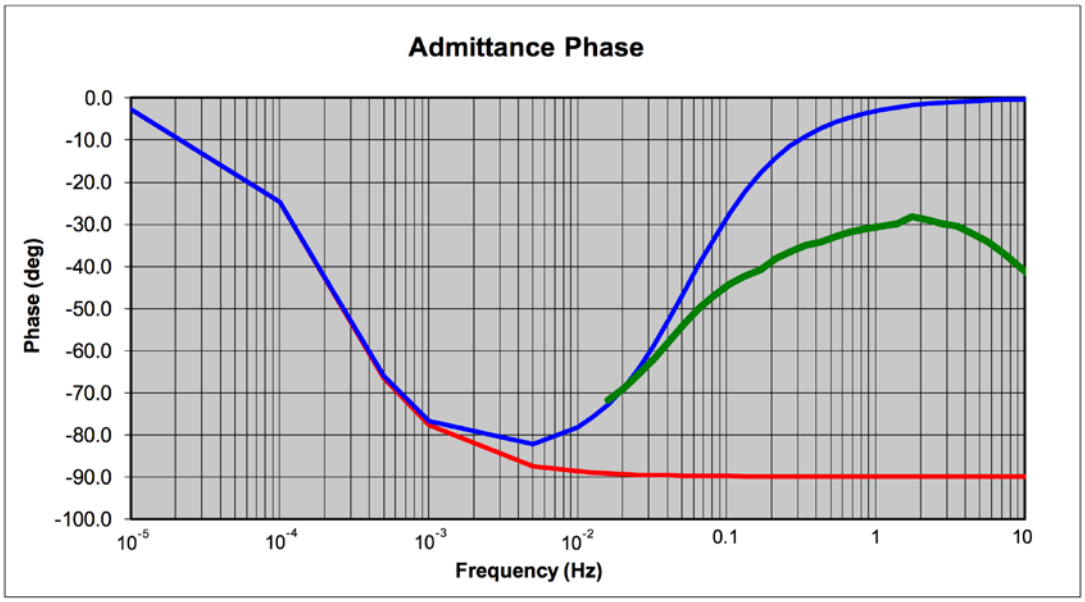
Table 1: LHC main circuit characteristics

Circuit	L	R_s	R_p	R_m	g_0	g_1	τ_0	τ_1	f_0	f_1
Dipoles	15.7	1×10^{-3}	1.54×10^{4}	0	1×10^{3}	6.5×10^{-5}	1.6×10^{4}	1.0×10^{-3}	1.0×10^{-3}	1.6×10^{2}
Quadrupoles	0.286	1×10^{-3}	1.06×10^{3}	0	1×10^{3}	9.4×10^{-4}	2.9×10^{2}	2.7×10^{-4}	5.6×10^{-4}	5.9×10^{2}

The simple first-order model shown in Fig. 1 does not describe any stray capacitances, which can be particularly significant for large superconducting magnets. An example is illustrated in Fig. 4, which shows the measured frequency response (green line) of the LHC ATLAS experiment's toroidal magnet circuit. The circuit does not have a parallel resistor ($R_p = \infty$) but the measured response only follows the model (red line) given by Eq. (4) up to about 2 mHz. It then diverges from the first-order attenuation of 20 dB/decade and follows a slower attenuation of around 6 dB/decade. This is because of unmodelled stray capacitance between the huge magnet coils. The blue line shows the theoretical response if the circuit had a 2.5 Ω parallel resistor. This matches the measured response quite well up to about 30 mHz. By defining a fictitious 2.5 Ω parallel resistor in the circuit model, the RST regulator improves the bandwidth for the rejection of perturbations by an order of magnitude.



(a)



(b)

Fig. 4: The ATLAS experiment at the CERN LHC has a large toroidal magnet assembly comprising ten coils. Figure (a) shows the Admittance Gain (dB) and figure (b) shows the Admittance Phase (degrees) against frequency. The green lines shows the measurement. The red line shows the theoretical response of the first-order model, while the blue line shows the theoretical response of the model if the circuit had a 2.5 Ω parallel resistance (R_p).

4.3.2 Unmodelled effects

As well as stray capacitance (as mentioned above), two other unmodelled effects may be significant in some magnet circuits.

– Eddy currents. These can be particularly important for magnets that have a solid iron yoke, where the time constant of the decay of the eddy currents can be in the order of seconds. Solid yoke magnets are typically cheaper to build, so for DC applications solid magnets with slow

eddy current decay time constants may be chosen. The effect of these eddy currents can be modelled as coupled inductor circuits, which can then be used to extend the load model to higher orders. However, this is not usually done and adequate performance is generally possible without it, provided that the magnet is not ramped too rapidly. For fast-cycling magnets, it is more or less essential for the magnet designers to use a laminated iron yoke that will have smaller eddy currents and a much shorter eddy current decay time constant.

– Saturation of the iron. If the magnet uses an iron yoke and if the magnetic field exceeds about 1 T, then the iron will start to saturate. When this happens, the differential inductance falls and this reduces the time constant of the circuit. This may need to be compensated, especially if the circuit is ramped rapidly. One approach to this compensation is discussed below. For DC circuits, if the saturation is not too extreme (<~20%), then it may be possible to tune the circuit for the middle value of the inductance and accept that the performance will not be optimal at the extremes.

4.4 Magnet saturation

Figure 5 shows a measurement of the differential inductance and stored energy for a real magnet circuit, in this case the 101 main magnets of the CERN PS accelerator. This shows the dramatic reduction in the differential inductance as the current rises due to the saturation of the iron in the yokes. When regulating the current, the time constant of the circuit will drop by more than 50%, which can lead to instability if it is not compensated. Figure 6 shows a photograph of the first PS magnet, which was produced in 1956. Figure 7 shows the measurement of the field and current for a cycle of the PS lasting 1.8 s. The field was being regulated up to 1.25 T (12 500 G), and the influence of the saturation of the iron yoke is clearly visible in the shape of the current signal as it approaches the maximum value of 5390 A. The current accelerates even as the field is decelerating.

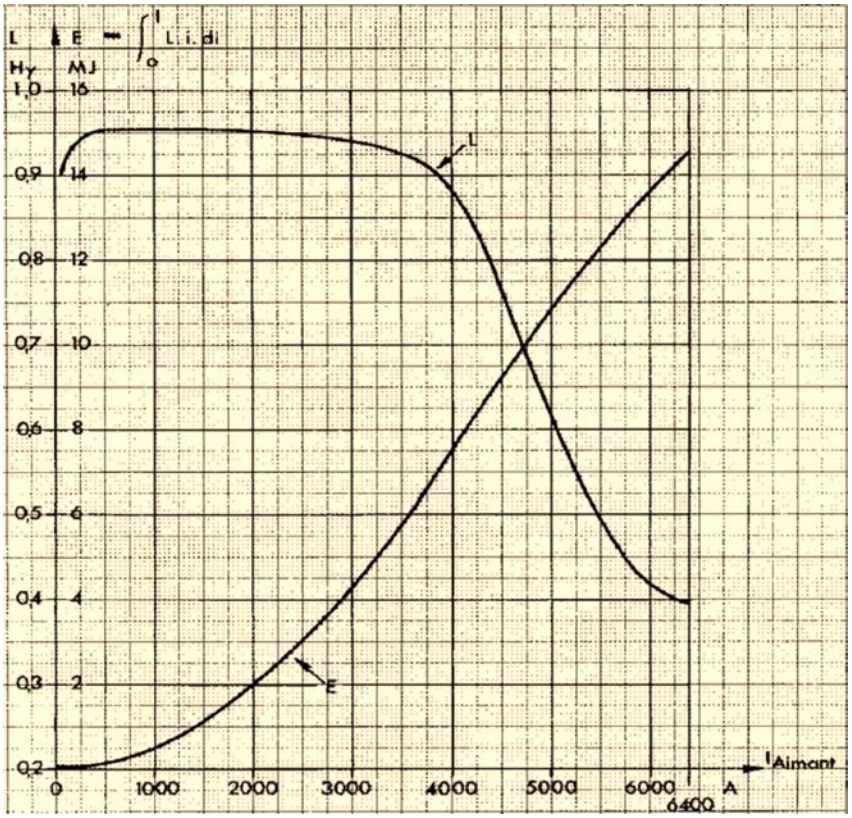


Fig. 5: Measurement of the differential inductance (L) and stored energy (E) of the 101 main magnets in the CERN PS accelerator, as a function of current. This illustrates the 55% reduction in the differential inductance, which the regulator must accommodate.

Fig. 6: Photograph from 1956 of the first PS magnet and members of the group who designed it. The CERN PS uses 100 of these magnets in the accelerator and one more on the surface for magnetic field measurements.

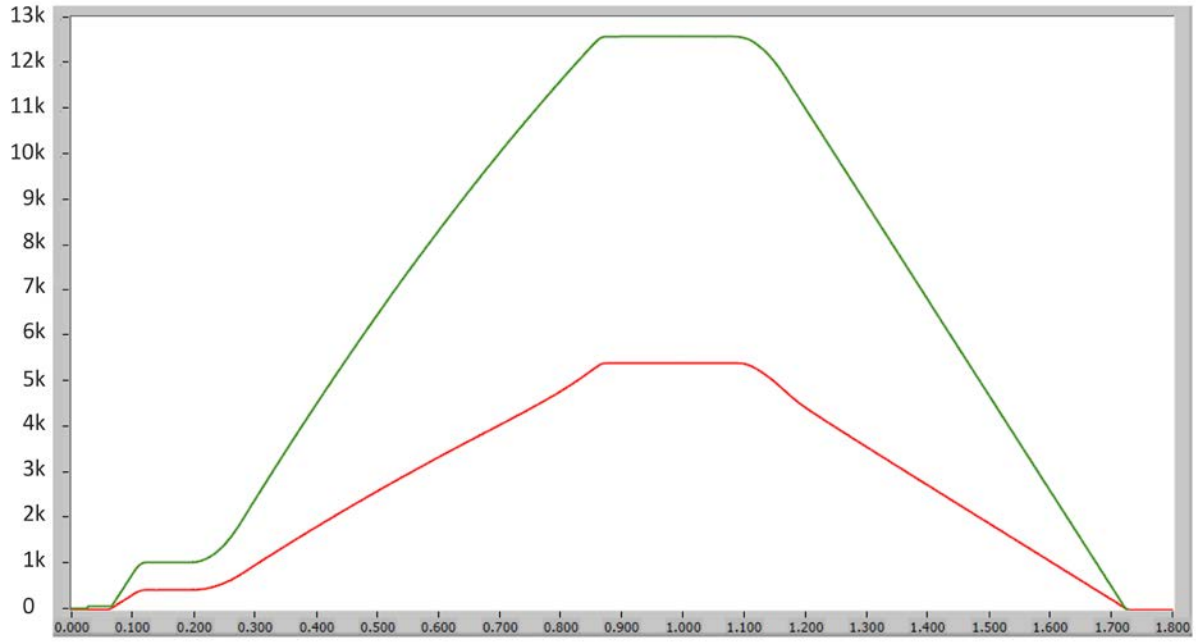


Fig. 7: Measurement of the magnetic field (green line in gauss) and circuit current (red line in amps) in the PS main magnets as a function of time in seconds. The magnetic field measurement is being regulated. The effect of the saturation of the iron yokes is visible in the form of the current, which accelerates at high field, even as the field is decelerating.

When regulating the magnetic field, the influence of the saturation is only a second-order effect, which can be neglected. This is the normal operating mode for the PS main magnet circuit; however, the regulator can switch between current and field regulation from cycle to cycle, and when current regulation is active, it must accommodate the change in the inductance.

Therefore, for current regulation, various strategies are possible.

– Ignore the effect of the saturation simply by reducing the bandwidth of the regulator to maintain stability even with the worst-case mismatch between the time constant of the circuit and the time constant expected by the regulator.

– Adjust the regulator parameters as a function of current. This is feasible for a classical PID regulator, but impractical for the RST algorithm, because it can be very time-consuming to calculate the RST coefficients and may even require offline computation using MATLAB (or equivalent).

– Hide the change in the inductance from the regulator by adjusting the voltage reference.

The third option is operating successfully at CERN using a surprisingly simple linear representation of the magnet inductance $L_m(I)$, as shown by the green line in Fig. 8. In this model, four parameters are used to characterize the inductance as a function of current: L, L_{sat}, I_{sat_start} and I_{sat_end}. Coincidentally, the form of this linear model (in green) is the same as the gain response on the Bode diagram shown in Fig. 2. Obviously, they are completely unrelated but it can be a source of confusion.

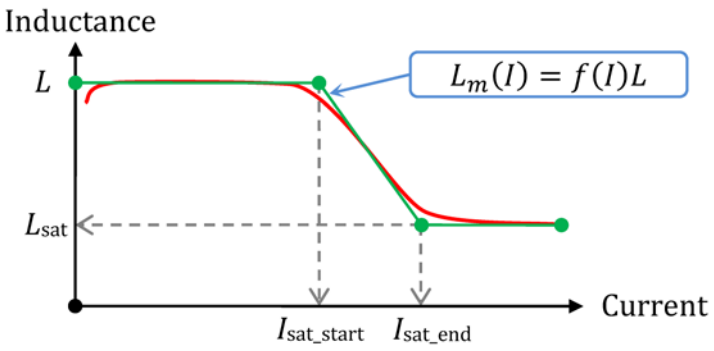


Fig. 8: Linear model for the reduction in the magnet inductance

The model is used to transform V_{ref} from the regulation algorithm into V_{ref_sat} that is sent to the voltage source (after limitation), in order to hide the saturation effect from the regulator. This is illustrated in Fig 9.

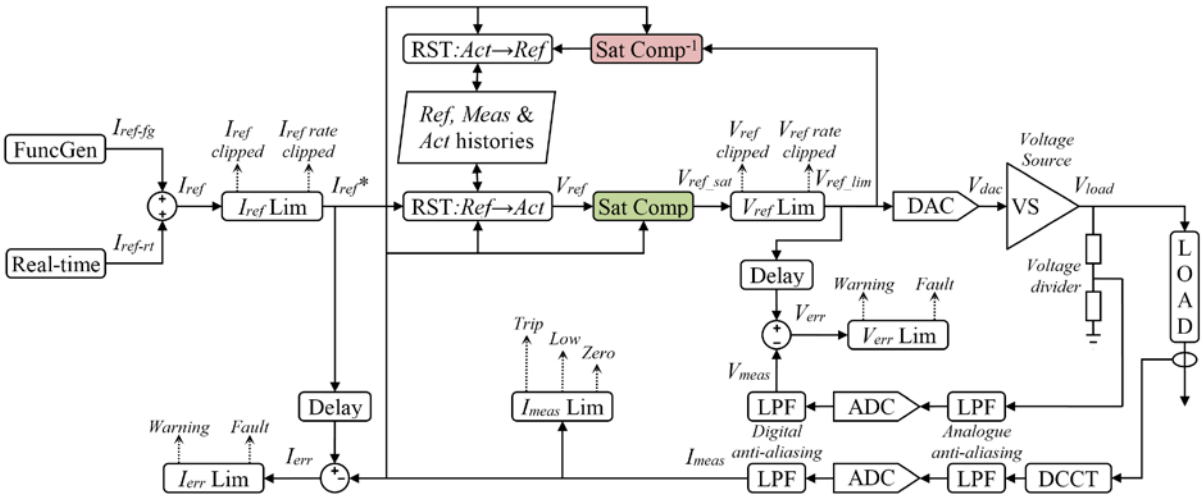


Fig. 9: Architecture of RST-based current regulation including saturation compensation (SatComp)

It is simple to show that $V_{\text{ref\_sat}}$ can be calculated from V_{ref}, I, and $f(I)$,

$$V_{\text{ref\_sat}} = \{1 - f(I)\}IR + f(I)V_{\text{ref}}\,, \tag{9}$$

where $f(I) = L_m(I)/L$ and R is the load resistance associated with DC operation,

$$R = R_s + \frac{R_p R_m}{R_p + R_m}\,. \tag{10}$$

Note that as the magnet saturates, $f(I)$ reduces from 1 and Eq. (9) mixes progressively less of V_{ref} and more of IR into $V_{\text{ref\_sat}}$. This reduces the influence of the feedback regulator and increases the feedforward contribution based on Ohms law. If $f(I)$ becomes too small, the performance of the regulator will be compromised. Experience has shown that regulation is still effective with $f(I)$ as low as 0.5.

Figure 9 shows how $V_{\text{ref\_sat}}$ passes through a limitation block that applies minimum, maximum and rate of change limits on the reference. The output, $V_{\text{ref\_lim}}$, is transmitted to the voltage source. In this case, it is assumed to have an analogue interface, so a digital–analogue converter (DAC) is used, but it could also be via a digital serial link if the voltage source requires it. As mentioned in Eq. (3), if the voltage reference is limited, the current reference stored in the RST history must be back-calculated from the voltage reference that is actually used. This means that the saturation compensation must be reversed, which is easy,

$$V_{\text{ref}} = \frac{V_{\text{ref\_sat}} - \{1 - f(I)\}IR}{f(I)}\,. \tag{11}$$

5 Controller integration

The quality of the integration of a converter controller into the wider accelerator control system can have a big impact on the reliability of the global system and the MTTR. In particular, effective analysis of powering failures depends upon having dependable logging and good tools for reviewing the logs.

5.1 Post-mortem logging

It is obviously essential to have access to important controller measurements in order to commission and optimize the regulation of a circuit. Furthermore, when a power converter trips, it can accelerate the analysis of the cause of the trip if the controller provides a log of the signals and events that occurred just before and after the time of the trip. This ‘post-mortem’ log can have two types of data:

- time series logs of important signals used in the regulation;
- time-stamped event data.

Both can be based on circular buffers. The duration of the time series logs will depend on the length of the log and the period of the sampling, while the duration of the event data will depend on how many events occurred during the period leading up to the trip. Figure 10 shows an example of an event data log from a controller in the LHC. It includes changes in state variables, diagnostics from the power converter, and commands from the upper levels of the control system.

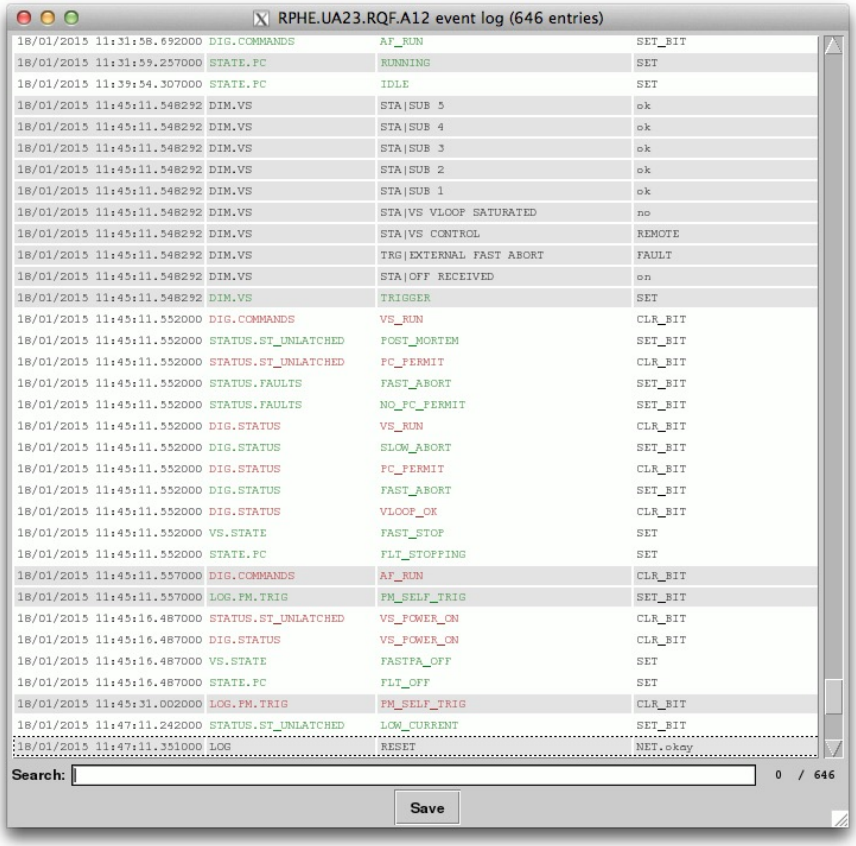


Fig. 10: Example of a post-mortem event log from the CERN LHC showing the trip of a main dipole circuit. The background grey bands indicate events that occurred simultaneously.

5.2 Simulation of the converter and circuit

No matter which approach is taken to regulation, it is a big advantage if the controller's software includes a simulation mode in which the power converter and load are simulated in real time. This allows upper levels of the control system to be developed and tested without needing to power the circuits. It also allows other parts of the controller software to be developed and tested without a power converter.

The simulation must be simple enough to execute in real time at the iteration rate of the controller's processor. If the circuit being modelled is basically resistive, then this iteration rate might be too slow to capture the dynamics of the load. The system is effectively under-sampled. When simulating offline, for example with MATLAB Simulink, the software can simply reduce the sampling period, but this is not possible for real-time software and the program must gracefully switch from a mode in which the dynamics of the load are modelled to a mode in which they are not. The same applies to the model of the voltage source, which may have a bandwidth that is too high to be modelled by the simulation.

The challenge of including a simulation mode is not completely trivial but it is absolutely worth the effort. Even a rudimentary simulation will be helpful.

6 Converter control libraries

Many of the issues related to RST regulation are treated in the CERN Converter Controls Libraries, which are open source and can be used freely. The website for the libraries is https://cern.ch/cclibs.

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Simulations

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Abstract
The complexity and cost of building and running high-power electrical systems make the use of simulations unavoidable. The simulations available today provide great understanding about how systems really operate. This paper helps the reader to gain an insight into simulation in the field of power converters for particle accelerators. Starting with the definition and basic principles of simulation, two simulation types, as well as their leading tools, are presented: analog and numerical simulations. Some practical applications of each simulation type are also considered. The final conclusion then summarizes the main important items to keep in mind before opting for a simulation tool or before performing a simulation.

Keywords
Simulation; power converters; analog simulations; numerical simulations.

1 What is simulation?

Simulation can be defined simply as an abstraction of reality, a representation of real-world activities. An even better definition would be that simulation is a procedure used to analyse physical systems which are too complex for theoretical considerations. However, simulation is performed by developing a model, and in turn a model constructs a framework to describe a physical system. In other words, simulation refers to the result of running a model. This means that one would not 'build a simulation'; rather, one would 'build a model', and then 'run a simulation'.

To illustrate the meaning of simulation, let us take an example: you have to perform some experiments on a physical system, for instance a car that hits a concrete wall at approximately 350 km/h. This experiment can be performed in two ways: either the physical system itself or a model of the physical system can be used. However, if the experiment needs to be repeated more than once a physical system may not be cost effective once cost and time-consuming factors are taken into account.

Using a cheaper physical model (e.g., an old car or other models of car with cheaper materials), or even better a mathematical model of your physical system, can minimize the cost and the time-consuming factors.

The experiment results from the mathematical model can be achieved by using either analytical methods for accurate results or simulation models for approximate results.

Therefore, on the one hand, a good understanding of your physical system will help you to build a good simulation model; on the other hand, a good simulation model will help you to optimize your real system. So, there is somehow a kind of correlation between a real system and its simulation model.

In brief, simulation is no more than a gross simplification of reality, because it includes only a few factors of the physical system. Simulation is only as good as the underlying assumptions. In other words, false assumptions mean false simulation models.

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2 Why simulation?

There may be several reasons why a simulation is appropriate. One of the main reasons is the fact that simulation allows experiments to be conducted without exposure to risk. In fact, a study of the real system can be too complicated, too expensive, or even too dangerous. Furthermore, simulation can be useful when the real system does not yet exist or is not understood. In addition, it may not be possible to observe the real system directly, or it could be working too fast (e.g., an electrical network) or too slow (e.g., geological processes) to be analysed directly. The last important point is that nowadays the complexity of systems in the field of power converters makes the use of simulation unavoidable.

2.1 Fields of application

Simulation is very versatile and suitable for applications in the field of engineering, physics, astrophysics, chemistry, biology, economics, social science, training, education, video games, and more. In this paper, only simulation for engineering applications, especially in the field of power converters for particle accelerators, will be taken into account.

2.2 Advantages of simulation

The biggest benefit of simulation is that time and cost are saved during the real-system implementation because designing, building, testing, redesigning, rebuilding, retesting, and so on could be very expensive in both time and money. In addition, simulation provides understanding about how systems really operate without building them. Moreover, simulations are repeatable and can be optimized at any time to give results that are not measurable with current technology.

2.3 Disadvantages of simulation

There are, however, some disadvantages of simulation of which the simulator should be aware. For instance, the simulation results could be completely wrong because of a few input data errors. Moreover, sometimes the results of complex simulations are difficult to understand and analyse. Apart from that, simulation cannot solve problems by itself, since a good simulation needs a basic understanding of the real system. Finally, building a good simulation tool can be very time consuming for the model constructor, and purchasing such a tool can be very expensive.

3 Principles of simulation

In the field of power converters for particle accelerators, simulation could be split up into two different types: analog simulation and numerical simulation. Which is used depends on the type of experiment that is to be performed.

On the one hand, analog simulation is summarized mathematically by a system of differential (or integral) equations. For this equation to be solved, a model of components and Kirchhoff's circuit laws must be put together. The system of equations is solved by using algebraic and arithmetic methods as the main technique for the entire model simulation.

On the other hand, for numerical simulation, after geometrical representation a mesh is created to divide an object into tiny elements which can be easily studied and recombined for the entire simulation system. Furthermore, the material properties and geometrical boundary conditions must be taken into consideration before solving the problem as a system of differential (or integral) equations. Here the numerical approximation is used as the main method to solve the equation system.

Generally, analog simulation is more appropriate for time-dependent systems, when the time can be precisely controlled. It is mainly used for circuit simulation. Numerical simulation is more suitable for space-dependent systems, where the space can be precisely controlled, and it is mainly

appropriate for field simulation. In other words, numerical simulation is useful when the evolution of the real system in space is required, whereas analog simulation is more convenient when the evolution of the real system in time has to be considered. Nevertheless, both analog and numerical simulations require some input data as starting values and some boundary conditions in order to perform the simulation. Both simulation types are independent, but could be used to analyse the same physical system.

Figure 1 shows one field of application for the analog simulation in which the time dependence is important: the current and voltage waveforms for an inductance circuit. Figure 2 illustrates a typical application for the numerical simulation: the magnetic field strength along a vertical cut plane. The result of the simulation is calculated at a certain point in space on the vertical cut plane.

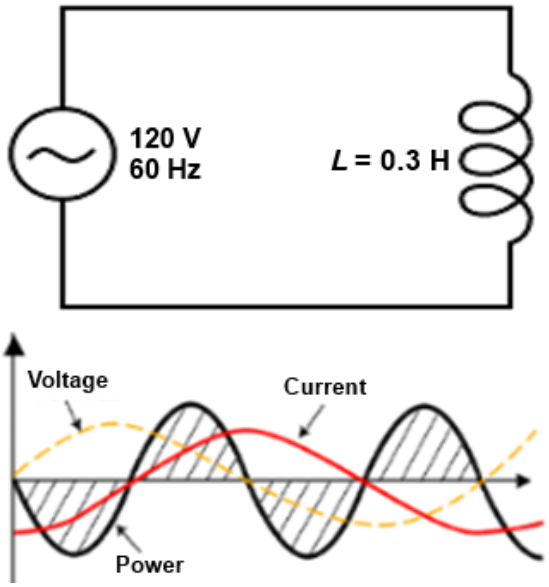


Fig. 1: Analog simulation: current and voltage waveforms for a pure inductance circuit

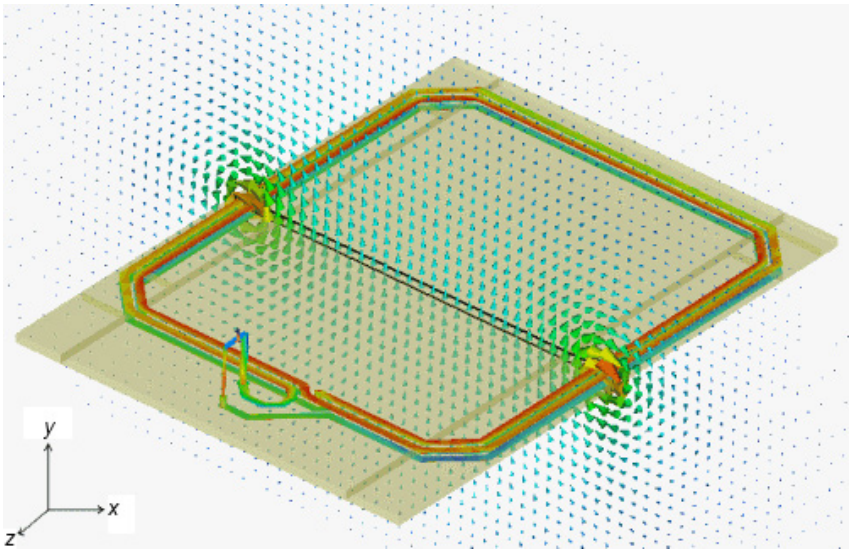


Fig. 2: Numerical simulation: surface current distribution of the coil and magnetic field strength along a vertical cut plane.

4 Types of simulation

Simulation, as already stated, can in general be split into two different types: analog and numerical. Now let us have a closer look at each type of simulation. Some practical applications of each simulation type will be considered.

4.1 Analog simulation

4.1.1 Analog simulation tools

We present some of the most utilized analog simulation tools in the field of power converters for particle accelerators.

4.1.1.1 PSpice (Personal Simulation Program with Integrated Circuit Emphasis)

PSpice is an analog and digital circuit simulation tool. It started as a simulation tool for low-power electronic circuits and it has been on the market for about 30 years. A large library of PSpice models for various electronic components exists. However, the representation of numerical blocks and controllers is difficult to achieve. The cost of a PSpice licence starts from €7000 for industry and from €3000 for universities. Student licences and demo versions are available, but with limited model sizes.

4.1.1.2 Matlab/Simulink/SimPowerSystems/PLECS

Matlab—a mathematical tool intended primarily for numerical computing—was first developed more than 40 years ago. However, optional toolboxes such as SimPowerSystems combined with Simulink allow the simulations of electrical power systems including power electronics. A Matlab licence combined with Simulink and SimPowerSystems starts from €8000 for industry and from €2000 for universities. Student licences and demo versions are available for a small amount, but they have limited model sizes. An additional toolbox, which can be combined with Matlab for the simulation of power electronics, is PLECS. This is a fast and reliable power toolbox for Matlab.

4.1.1.3 Simplorer

ANSYS Simplorer is a multidomain simulation tool for complex power electronic and electrically controlled systems. Simplorer basically integrates four modelling techniques (e.g., digital simulator, circuit simulator, block diagram, and tate machine) that can be used concurrently within the same schematic. Simplorer can be interfaced to many other simulation tools. A Simplorer licence starts from €3500 for universities. Student licences and demo versions are available, but with limited model sizes.

4.1.1.4 PSIM (PowerSim)

PSIM is one of the simulators that was developed 20 years ago specifically for power electronics, but it can be used to simulate any electronic circuit. PSIM is one of the fastest simulators for power electronics simulation, and therefore it is optimized for the tasks that arise in this field. This results in a faster simulation time. PSIM can be interfaced to Matlab/Simulink in order to use the full mathematical power of Matlab. A PSIM licence starts from €1700 for Industry and from €280 for universities. Student licences and demo versions are also available for a small amount, but with limited model sizes.

4.1.1.5 LTspice IV

LTspice IV is a freeware tool for analog circuit simulation, produced by Linear Technology Corporation. LTspice IV is considered as one of the best freeware tools available for circuit simulation. It started as a simulation tool for models to ease the simulation of switching regulators, but other models of components have been added for electrical circuits. LTspice IV is the most widely

distributed and utilized SPICE (Simulation Program with Integrated Circuit Emphasis) program in the industry.

4.1.1.6 CASPOC

This tool is designed for the simulation of power electronics and electrical drives. CASPOC is used in the design and simulation of complex power and control devices and systems. It is appropriate for multiphysics (e.g., Computational Fluid Dynamics, mechanical, thermal, or electromagnetic) control systems. CASPOC is the only simulator on the market with a circuit animation feature, which contains a 'freeze and go back' function. A freeware version of CASPOC is available; prices and conditions for industry or universities are unknown to the author.

4.1.2 Field of application 1: temperature simulation for the European XFEL at DESY Hamburg

At DESY Hamburg, the European X-ray Free-Electron Laser (XFEL) linear accelerator is currently under construction. Figure 3 shows the cross-sectional view of the tunnel for the particle acceleration part, the so-called XTL tunnel. Figure 4 presents the longitudinal view of the underground XFEL tunnels, with a total length of about 3.4 km, a depth from 6 m up to 38 m, and diameters of 5.2 m for the XTL tunnel and 4.5 m for the photon tunnels. Simulations were very helpful in fixing the required temperature profile for the XTL tunnel.

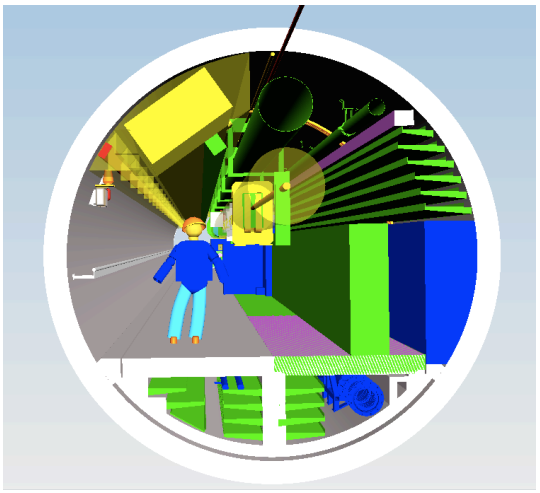


Fig. 3: Cross-sectional view of the 2.1 km XTL tunnel

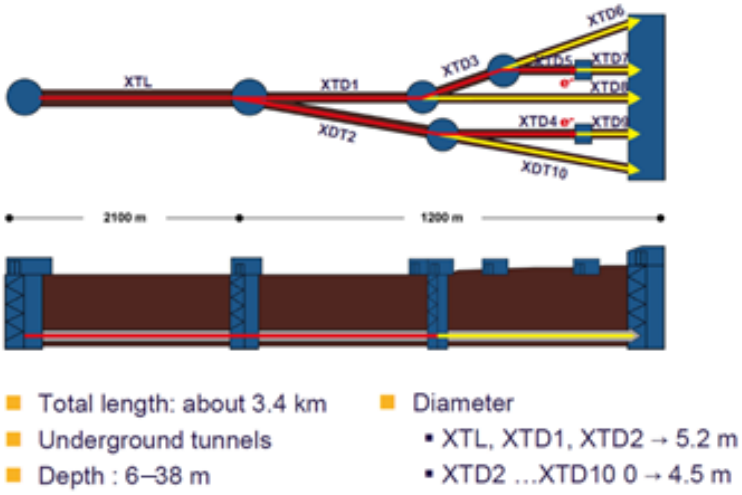


Fig. 4: Longitudinal view of the XFEL tunnels

4.1.2.1 Motivation

Many LLRF (Low Level Radio Frequency) signal cables whose transmission time is very sensitive to the temperature variation, are installed in the XTL tunnel. For a high-precision machine like XFEL, such effects are undesirable. In order to prevent the changes in propagation time of the LLRF signals, a stable temperature profile along the tunnel is required. This sensitive stability allows only a temperature variation in the range of ±1 K, even during different operational modes of the accelerator (e.g., maintenance days, limited access, or full operating time). Since the system does not yet exist and furthermore is very complex to analyse, using simulations was the best way to fix this special temperature requirement concerning the XTL tunnel.

Some simulations had already been done by means of Matlab for the steady-state temperature calculation. In addition, it should have been possible to perform transient analyses with a numerical simulation tool such as ANSYS CFX, but these cost too much in computing time and capacity due to the limited ANSYS CFX licences at DESY.

To achieve this goal despite this fact, the ANSYS Simplorer package was chosen for analog simulation. Two reasons motivated this choice. First, ANSYS Simplorer can handle complex multiphysics circuit systems with transient behaviour (e.g., electrical, thermal, electromechanical, electromagnetic, and/or hydraulic) quite easily. Second, it has a very stable simulation algorithm. Also, enough user licences were available in our department.

4.1.2.2 Proceeding

As a first step, several input parameters, such as the heat sources (e.g., lights, cables, waveguides, hot water pipes, pulse transformers, and matching networks and magnets) as well as the heat sinks (e.g., cold water pipes, the fact that the tunnel is underground) were investigated and the inlet temperature defined. In addition, knowledge of the geology of the ground, and previous experience with and temperature measurements in the former accelerator machine HERA, were helpful in understanding the real system and implementing a good and reliable simulation model.

The second step was to transform the physical components of the tunnel (e.g., heat sources, tunnel wall, or air) into the thermal circuit component (e.g., capacitance or resistance) model, and then to add the material properties to these components. However, some heat sources and heat sinks changed every 50 m along the accelerator tunnel. This meant that a new component model was necessary along every 50 m section in the tunnel to complete the entire simulation, as presented in Fig. 5. In this way the entire XTL tunnel was divided into several 50 m sections and was drawn as a model of a thermal circuit in the ANSYS Simplorer schematic. To simulate the transient temperature behaviour in the entire XTL tunnel, a total of 43 models were added in series, as shown in Fig. 6.

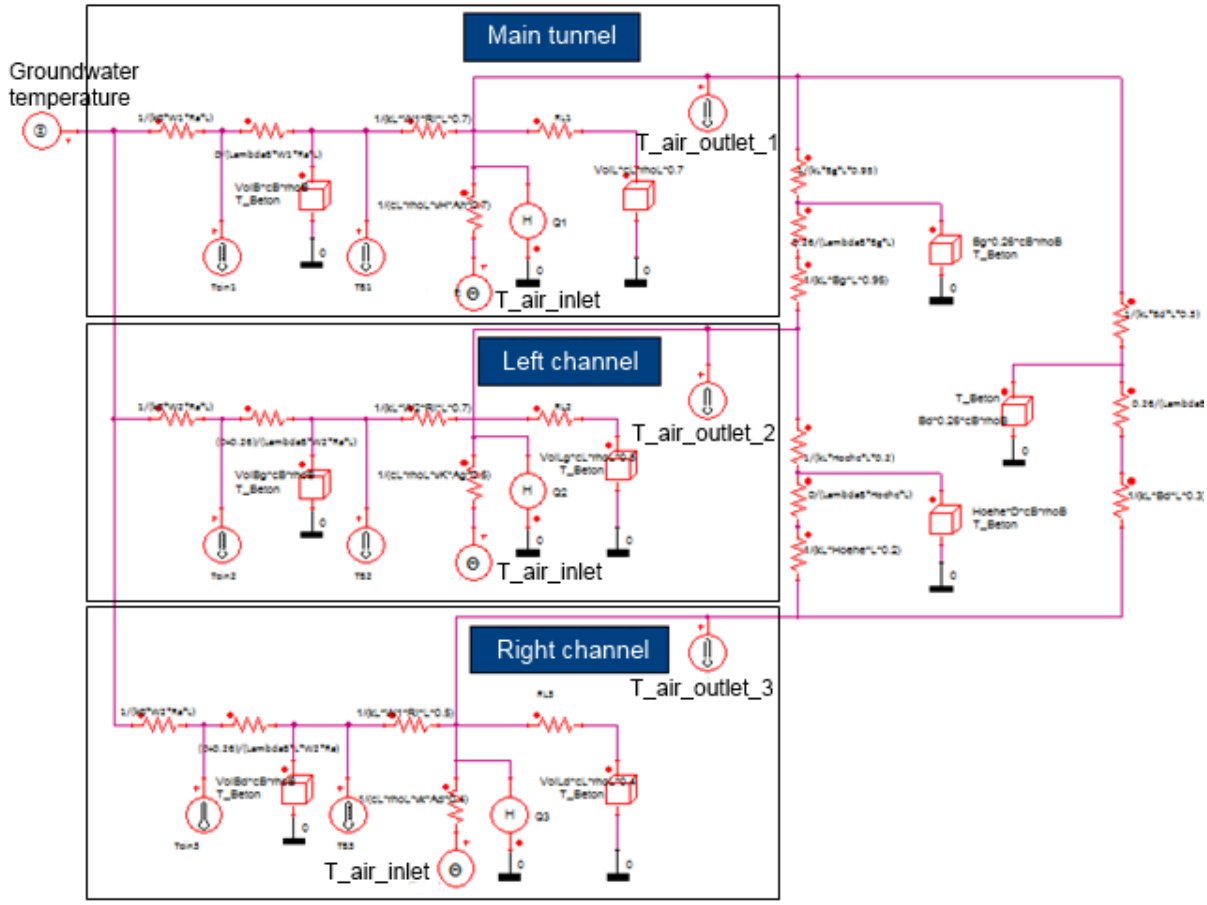


Fig. 5: Model of the 50 m XTL tunnel section as a thermal circuit in the schematic of ANSYS Simplorer

Fig. 6: The entire 2.1 km XTL tunnel with a total of 43 model components as a thermal circuit in the schematic of ANSYS Simplorer.

4.1.3 Simulation results

Figure 7 shows a photograph of the empty XTL tunnel at DESY with the lights as the only heat sources. After running the first simulation, several measurements were made in the empty physical tunnel to assist with further adjustments on the simulation model in order to obtain—on 12 March, 2013—the first plot of the temperature profile (see Fig. 8). This figure shows the measurement as well as the simulation for the steady-state temperature behaviour in the XTL tunnel. The underground

temperature around the tunnel during the measurement was about 11°C. This achievement is the outcome of about 6 months of simulation analyses as well as measurements in the empty XTL tunnel.

Therefore, the best way to fit the simulation results with the measurements is a good understanding of the real system. Furthermore, some measurements on the real system are necessary in order to perform the appropriate readjustments of the simulation model.

Fig. 7: The empty XTL tunnel at DESY Hamburg with the lights as the only heat sources

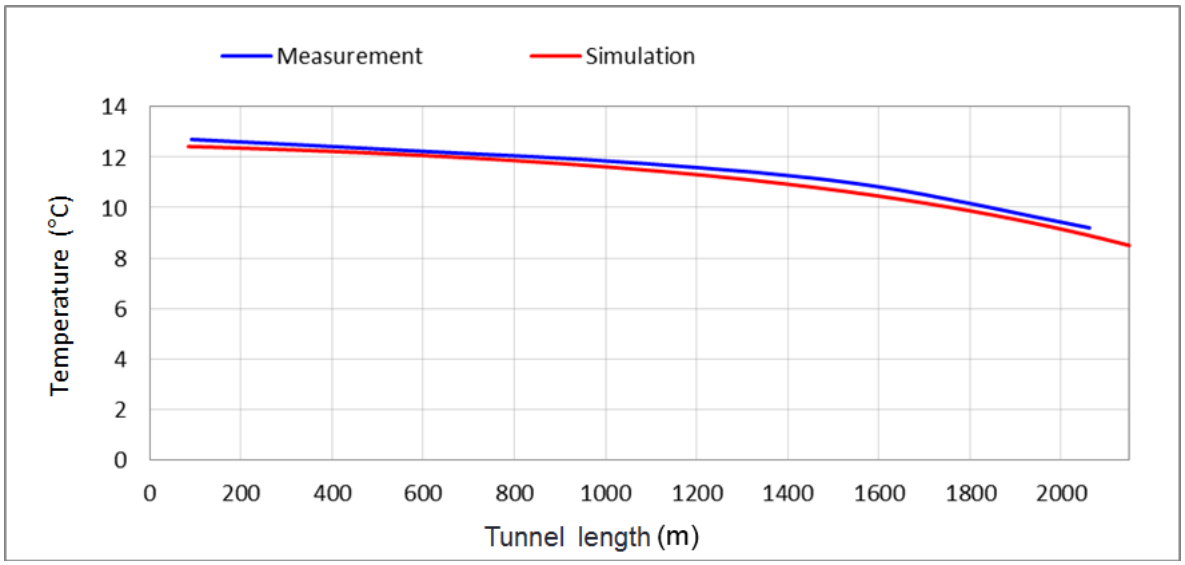


Fig. 8: Measurement of the temperature profile in the 2.1 km empty XTL tunnel on 12 March, 2013, compared with the simulation.

Since the simulation of the steady-state temperature behaviour in the empty XTL tunnel was satisfactory, the next step was to analyse the transient temperature behaviour once the tunnel was no

longer empty and during different operating modes of the XFEL accelerator machine. Table 1 displays how the most important heat sources are distributed in the three parts of the XTL tunnel: the main tunnel, the left cable channel, and the right cable channel. Table 1 also shows when the heat sources are in service (ON) or not (OFF) for two different operating modes of the machine: maintenance days and the full operating time. The goal now is to simulate the expected temperature profile along the XTL tunnel after a typical service day of about 10 h or after 10 days of full operating time.

Note that the air flows from the end (at about 2.1 km) to the beginning of the tunnel, so that the inlet temperature starts at the end of the tunnel. An inlet temperature of 23°C is chosen for all further temperature simulations.

Table 1: Distribution of the most important heat sources in the three parts of the XTL tunnel: the main tunnel, the left channel, and the right channel.

Heat sources in the XTL tunnel	Tunnel part	Operating time	Maintenance day
Pulse cables, left	Left channel	ON	OFF
Pulse cables, right	Right channel	ON	OFF
Medium voltage power cables	Main tunnel	ON	ON
Low voltage power cables	Left channel	ON	ON
Direct current power cables	Left channel	ON	OFF
Transformers	Main tunnel	ON	OFF
Impedance matching network	Main tunnel	ON	OFF
Magnets	Main tunnel	ON	OFF
30°C water pipe 1 (feed line)	Main tunnel	ON	ON
40°C water pipe 1 (outlet flow)	Main tunnel	ON	ON
20°C water pipe 2 (feed line)	Main tunnel	ON	ON
25°C water pipe 2 (outlet flow)	Main tunnel	ON	ON
20°C water pipe 3 (feed line)	Main tunnel	ON	ON
20°C water pipe 4 (feed line)	Right channel	ON	ON
20°C water pipe 5 (feed line)	Left channel	ON	ON
Electronic racks	Main tunnel	ON	ON
Waveguides	Main tunnel	ON	OFF
Light	Main tunnel	OFF	ON

Figure 9 shows the temperature profile over the time 50 m from the end of the XTL tunnel during a maintenance day. There are two points to note from this figure: first, the steady-state temperatures are reached after about a day of machine operating with values more or less the same as the inlet temperature. Second, after 10 days of full operation, the temperature values in the three tunnel parts change minimally—about 1.2°C when the accelerator is switched off for 10 h of maintenance. When the accelerator is switched on again for the full operating mode, the temperatures take more than a day to reach the steady-state values.

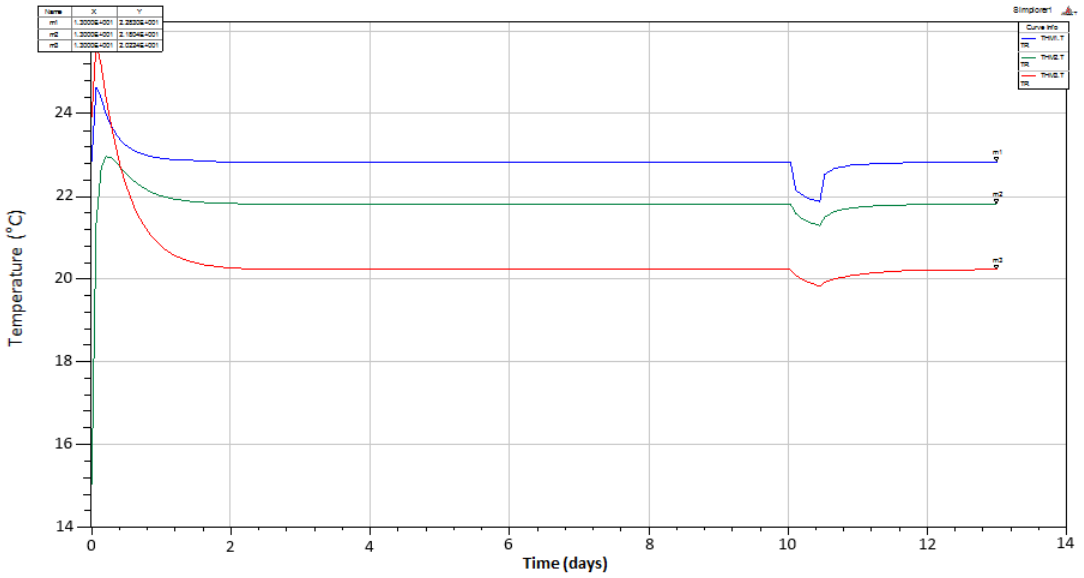


Fig. 9: The changes in temperature over time 50 m from the end of the the XTL tunnel (at about 2.1 km). Blue curve: temperature in the main tunnel; green curve: temperature in the left cables channel; red curve: temperature in the right cables channel.

The air became much warmer at the beginning of the tunnel (see Fig. 10), at about 2.1 km away from the position in Fig. 9. Two points should be also emphasized. First, the steady-state temperatures are reached after more than one day of machine operating at approximately 4°C above the inlet temperature. Second, after 10 days of full operation, the temperature values in the three tunnel parts drop by about 7°C after 10 h of maintenance. When the accelerator is switched on again for the full operating mode, the temperatures take more than two days to reach steady-state values.

In this manner the analog simulation provides understanding about how the XTL tunnel really operates. Moreover it was possible using the simulation to consider all the interactions between the heat sources and the heat sinks and finally determine the requirements for stable temperature behaviour in the tunnel during different machine operating modes.

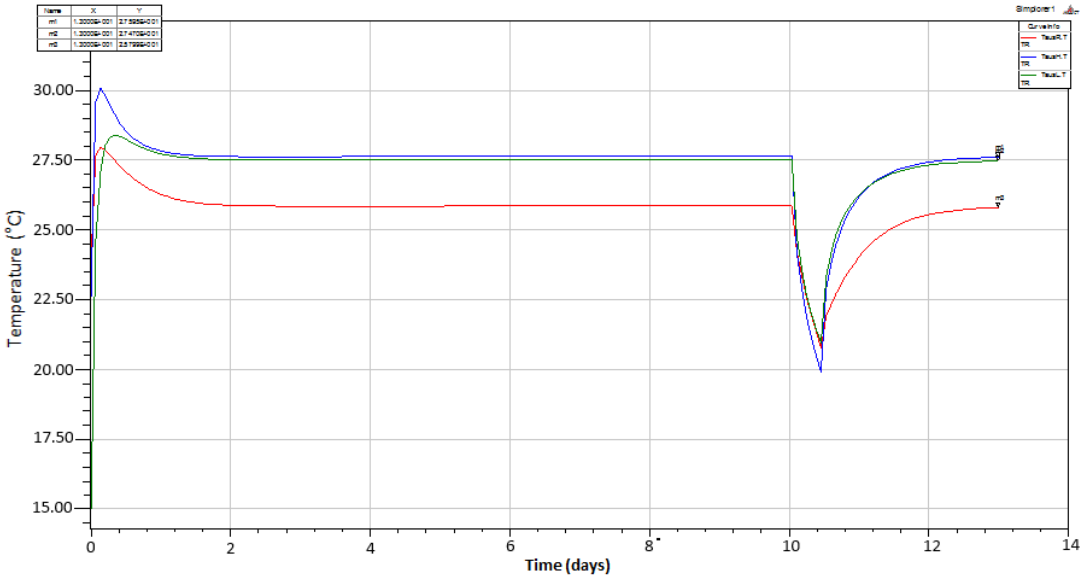


Fig. 10: The changes in temperature over time at about 2.1 km from the end of the XTL. Blue curve: temperature in the main tunnel; green curve: temperature in the left cables channel; red curve: temperature in the right cables channel.

4.1.4 Round up

The example shows that for simulation at least a basic understanding of the physical system is required. However, the simulation model should be as simple as possible, but should be complex enough to answer the questions asked. When possible, making measurements on the real system helps to optimize the model for accurate simulation results.

4.2 Numerical simulation

4.2.1 Numerical simulation methods

Numerical approximation methods are used to find the solution of numerical simulation problems. Some of the most used numerical methods are discussed in the following.

4.2.1.1 The finite difference method

The finite difference method (FDM) is the method used to approximate the solutions to differential equations using finite difference equations to approximate derivatives. The principle consists in approximating the differential operators by replacing the derivatives in the equations using differential quotients. The domain is partitioned in space and time, and approximations of the solutions are computed at the space or time points.

4.2.1.2 The moment method

The method of moments (MoM) is a numerical computational method of solving linear partial differential equations which have been formulated as integral equations. It can be applied in many areas of engineering and science, including fluid mechanics, acoustics, electromagnetics, fracture mechanics, and plasticity.

4.2.1.3 The finite element method

The finite element method (FEM) is used to find approximate solutions of partial differential equations (PDEs) and integral equations. The solution approach is based on either eliminating the time derivatives completely (steady-state problems) or rendering the PDE into an equivalent ordinary differential equation, which is then solved using standard techniques such as finite differences, etc. In solving PDEs, the primary challenge is to create an equation which approximates the equation to be studied, but which is numerically stable. The FEM is a good choice for solving PDEs over complex domains or when the desired precision varies over the entire domain.

4.2.1.4 The Monte Carlo method

The Monte Carlo method is based on repeated random sampling to obtain numerical results. The simulation typically runs many times over in order to obtain the distribution of an unknown probabilistic entity. The Monte Carlo method is often used in physical and mathematical problems, and is most useful when it is difficult or impossible to obtain a closed-form expression, or infeasible to apply a deterministic algorithm. Monte Carlo methods are mainly used in three distinct problem classes: optimization, numerical integration, and generation of draws from a probability distribution.

4.2.1.5 The method of lines

The method of lines is a general technique for solving PDEs by typically using finite difference relationships for the spatial derivatives and ordinary differential equations for the time derivatives.

4.2.2 Numerical simulation tools

The following tools are among the best known numerical simulation packages in the application field of power converters for particle accelerators.

4.2.2.1 Quickfield

Quickfield is based on finite element analysis and is developed and distributed by Tera Analysis Ltd. It is available as a commercial program or as a free program with limited functionality. Quickfield is a stable and fast package, which is mainly used for the simulation of electromagnetic fields. A licence starts from about €1200, depending on the version and the type of application. Therefore it is less expensive for research institutes.

4.2.2.2 ANSYS CFX

ANSYS Computational Fluid Dynamics (CFX) simulation software allows the simulation of fluid flow in a variety of applications. It is based on finite element analysis, which was developed by Dr John Swanson. His company, founded in 1970—SASI (Swanson Analysis Systems Inc.)—developed the first versions of ANSYS up to version 5.1. After the sale of the company in 1994 it was renamed ANSYS Inc. ANSYS CFX solutions are fully integrated into the ANSYS Workbench platform. Workbench integrates workflow needs as well as multiphysics functionality (fluid–structure interaction, electronic–fluid coupling, etc.). A student licence with reduced model sizes is available. Price and conditions for industry or research institutes are unknown to the author.

4.2.2.3 ANSYS HFSS

The HFSS (High Frequency Structure Simulator) is a finite element method tool for three-dimensional full-wave electromagnetic field simulation from ANSYS and is essential for the design of high-frequency component design (e.g., antenna design). Previously known as the Ansoft HFSS, Ansoft was later acquired by ANSYS. A licence starts from €20,800 for industry and from €14,000 for universities. A student licence with reduced model sizes is less expensive.

4.2.2.4 ANSYS MAXWELL 2D

Maxwell 2D is an electromagnetic simulation software program used to develop accurate virtual prototypes of electric machines, actuators, transformers, sensors, and other electromagnetic devices that can be represented in two dimensions. A student licence with reduced model sizes is available. Prices and conditions for industry or research institutes are unknown to the author.

4.2.2.5 FEKO

FEKO is a MoM tool developed by EM Software & Systems – S.A. (Pty) Ltd for electromagnetic simulation. FEKO has an online simulation service with the cost of usage per hour per core used, which includes FEKO licence fees.

4.2.2.6 CONCEPT-II

The CONCEPT-II software is an advanced electromagnetic field simulator for the numerical computation of radiation and scattering problems in the frequency domain. The code is based on the MoM and integral equations for the electric and magnetic fields. CONCEPT-II is developed by the Institute of Electromagnetic Theory at the Technical University of Hamburg–Harburg (TUHH) and can be used free of charge in academia. Price and conditions for industry are unknown to the author.

4.2.3 Field of application 2: grounding of HV power suppliers (modulators) for RF stations for the XFEL

Let's consider now an example of application for the numerical simulation. The European X-ray Free-Electron Laser (XFEL) linear accelerator at DESY Hamburg requires 29 RF stations capable of 10 MW RF power each for electron acceleration in the XTL section. The RF power for the XFEL linear acceleration is generated by klystrons which are installed in the underground XTL tunnel, close to the accelerator modules. The klystrons are powered by HV pulses from modulators which are located in the modulator hall (XHM), above ground on the DESY site. Each modulator is connected to the pulse transformer at the klystron by means of a long triaxial cable and pulses up to 12 kV and 2 kA with a duration of 1.7 ms and a nominal repetition rate of 10 Hz. The grounding simulations of these modulators assist in greater understanding of some EMC effects occurring during commissioning.

Figure 11 shows a combination of devices connected from the transformer to the modulator. HV racks distribute the power among the 29 modulators and the HV racks. The modulators are interconnected by a system of protection earth, grounding, and power cables, which are three-phase cables without a neutral conductor.

Fig. 11: Combination of devices comprising the modulator system in the hall

4.2.3.1 Motivation

Measurements taken after installing and commissioning the first modulator showed some electromagnetic interference which was not understood. The sources of a 50 Hz high current of more than 50 A peak to peak, measured on the PE conductor were unknown. Faults in the insulation of the power cables and PE conductor had already been excluded after insulation measurements were made. The main suspect was the EMI current induced from the power cables.

The goal was to perform simulations to confirm the suspicions and finally to find a solution for the optimization of the grounding system of the 29 modulators. To achieve this, Quickfield was chosen from the tools for numerical simulation for several reasons. Quickfield is very easy to learn and offers the useful possibility of combining electrical circuits with field simulations. In other words, geometrical models from the numerical simulation could be easily transformed as electrical circuits in the same schematic of Quickfield. Moreover it is a multiphysics tool—very stable and very fast with various analysis types (e.g., a.c., d.c., and transient electromagnetics, electrostatics, steady-state and transient heat transfer, stress analysis). The main disadvantage is that only basic components for electrical circuit analysis (e.g., resistors, capacitors, inductors, diodes, voltage sources, and current sources) are available in the library of Quickfield components.

4.2.3.2 Technical data for the modulator

The technical data for the modulator is given in Table 2 and Fig. 12 shows the overview of the modulator hall at DESY Hamburg.

Table 2: Technical data for the modulator

Number of modulators	29
Output voltage	0–12 kV
Output current	0–2 kA
Average output power	max. 380 kW
Maximum pulse power	16.8 MW
Pulse duration	0.2–1.7 ms
Pulse repetition rate	1–30 Hz

Fig. 12: Overview of the modulator hall

4.2.3.3 Proceeding

Figure 13 shows an overview of the grounding schematic of the modulators connected as a TNS (Terre Neutre Séparé) system, with PE (protective earth) and N (Neutral) conductor separated from the transformer grounding point. The neutral conductor between the HV racks and the modulators is not required because of the symmetrical properties of the modulators as loads. The cable length between the modulator and the HV racks is about 30 m. The schematic of Fig. 13 was translated as a space-dependent system in Quickfield for field simulation analysis. The field simulation was used to visualize the influence of the electromagnetic field propagation around the power cables. First, the

geometry of the power cable systems and surrounding devices (e.g., cable trays, PE conductors) was drawn to build a model for the numerical simulation that is as accurate as possible. Then the geometrical models were transformed into electrical circuit components for further electrical circuit analysis.

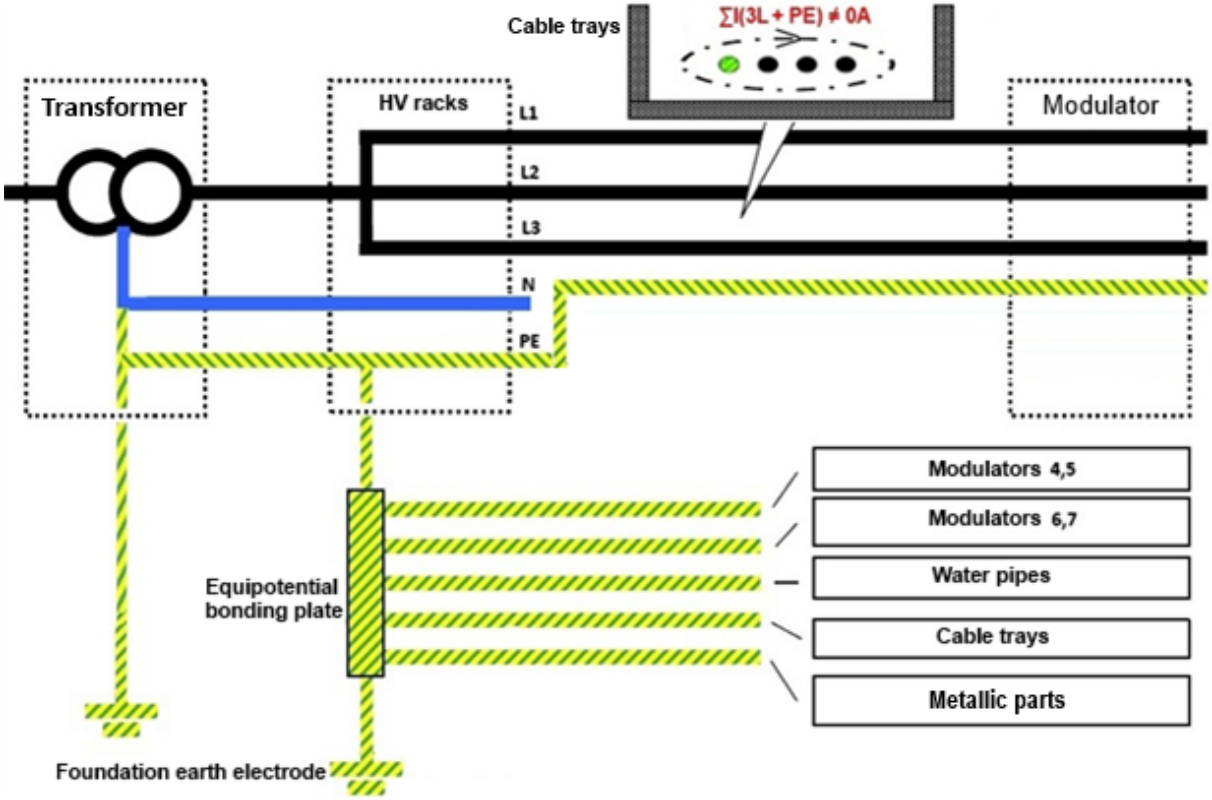


Fig. 13: Overview of the grounding schematic of the modulators

4.2.4 Simulation results

Figures 14–19 show the simulation results in three different cases: when the PE conductor is near to, between, or about 25 cm away from the power cables. These results will then be compared with the measurements.

4.2.4.1 PE conductor near to one of the three power cables

Figure 14 (left) shows the magnetic field and the current density field simulation. The electrical circuit schematic from the field simulation can be observed on the right. Fig. 15 illustrates the measurement for simulations results verification. The effective (rms) of the current on the PE conductor between both figures is almost the same. This means the good accuracy of the simulation model compared to the real system. The simulation analysis demonstrates that the power conductors induce uncompensated annoying currents on the PE conductor and the cable trays around. The inducted current on the PE conductor is up to 10% of the power conductors current, which is not desirable for a high precisely accelerator machine like the European XFEL. Then the high PE conductor current could flow through the ground and finally disturb the electrons acceleration in the machine. Furthermore that current could interfere as noise signal for the machine beam monitoring. Further simulations will show how to reduce the inducted current in the PE conductor.

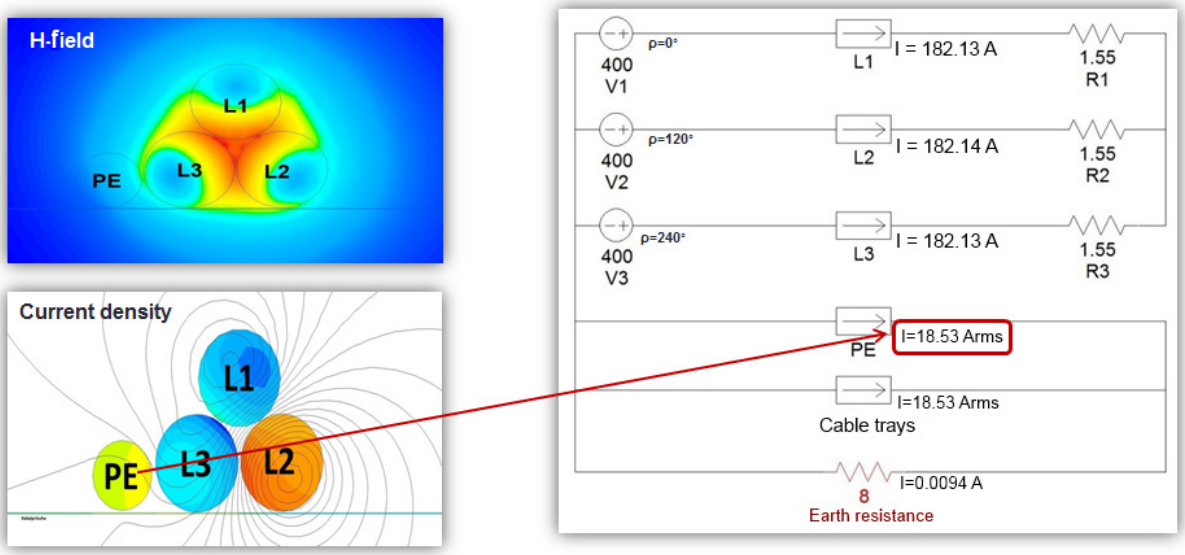


Fig. 14: Simulation with the PE conductor near to one of the three power cables

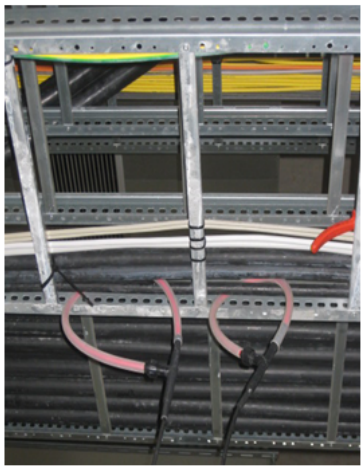
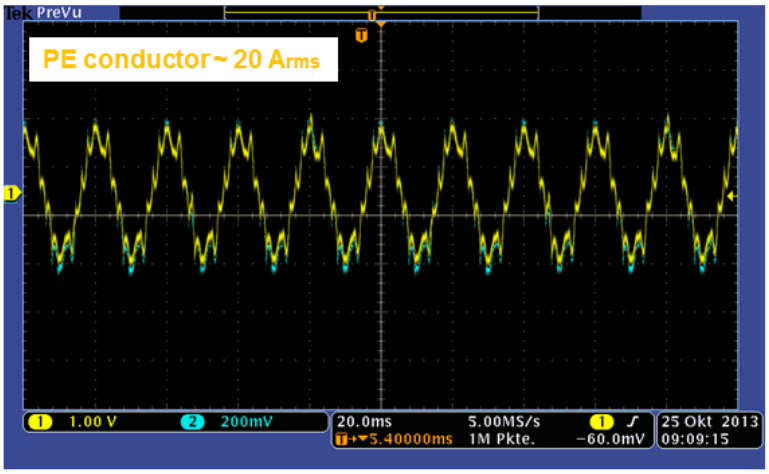
Picture	Measurement
	
Voltage of modulator = 10 kV, pulse repetition = 10 Hz, pulse length = 1000 µs	

Fig. 15: Measurement with the PE conductor near to one of the three power cables

4.2.4.2 PE conductor between the power cables

Figure 16 illustrates the results of simulation when the PE conductor is between the three power cables. The current on the PE conductor is greatly reduced, from about 20 A_{pp} to about 6 A_{pp}, because the electromagnetic fields between the power cables cancel each other out. The H-field and the current density simulation in Fig. 16, as well as the measurement shown in Fig. 17, confirm this. The difference in value of the PE conductor current in the simulation and that in the measurement is because it is difficult to fix the PE conductor exactly in the middle of the three power cables. The blue sine wave in Fig. 17 represents the uncompensated current measured around the three-phase power cables.

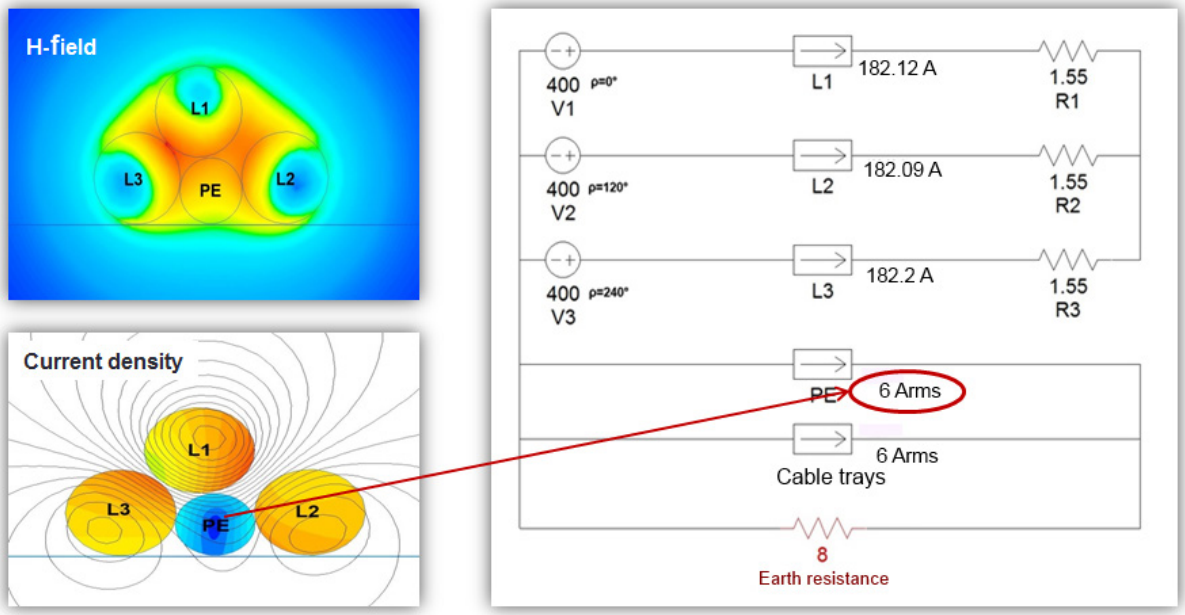


Fig. 16: Simulation with the PE conductor between the power cables

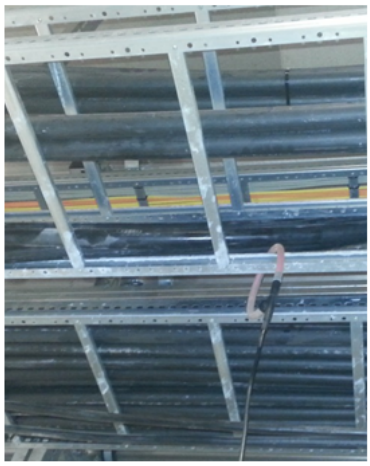
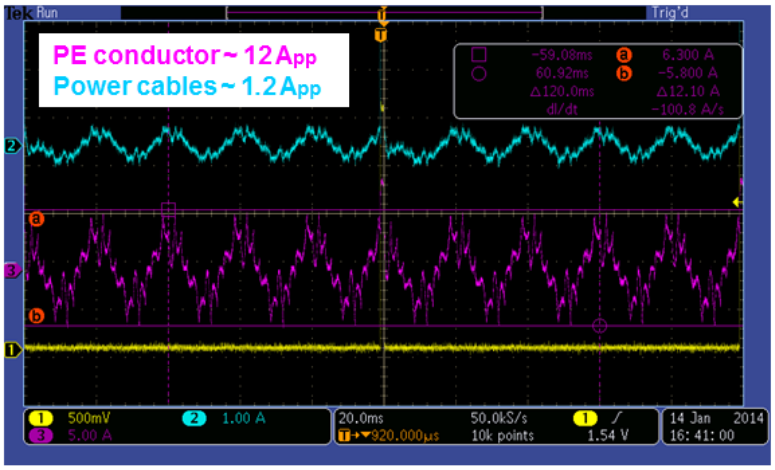
Picture	Measurement
	
Voltage of modulator = 10 kV, pulse repetition = 10 Hz, pulse length = 1000 µs	

Fig. 17: Measurement with the PE conductor between the power cables

4.2.4.3 PE conductor about 25 cm away from the power cables

Figure 18 shows the results of the simulation when the PE conductor is fixed on the cable tray about 25 cm away from the three power cables. The current in the PE conductor is now greatly reduced, to about 2.8 A_{pp} because the strength of the electromagnetic field decreases further away from the power cables. The simulation results in Fig. 18, as well as the measurement in Fig. 19, demonstrate this. The blue sine wave in Fig. 19 represents the uncompensated current measured around the three-phase power lines.

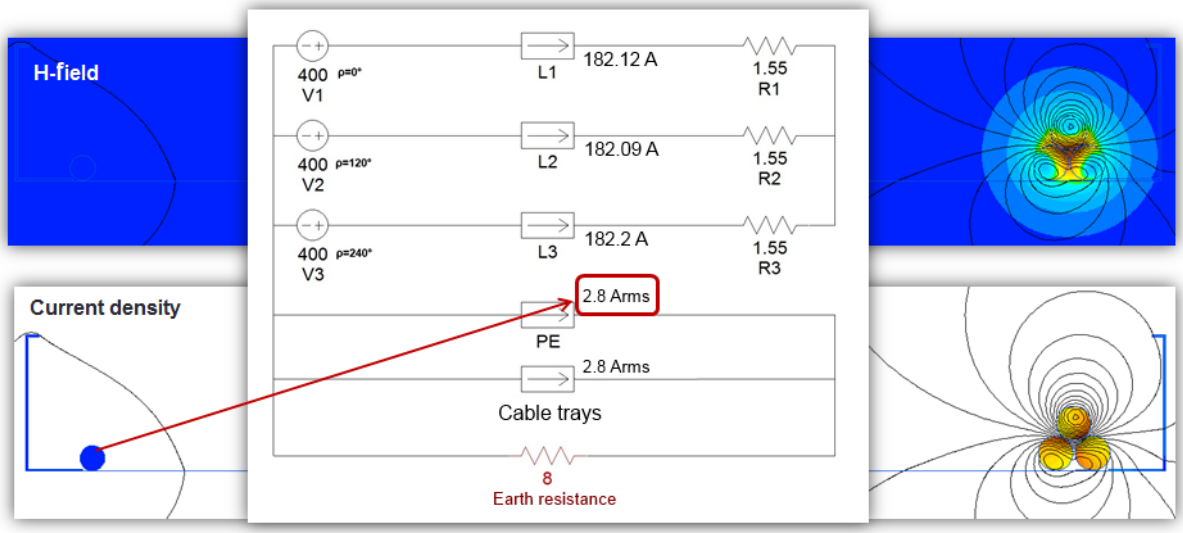


Fig. 18: Simulation with the PE conductor about 25 m away from the power cables

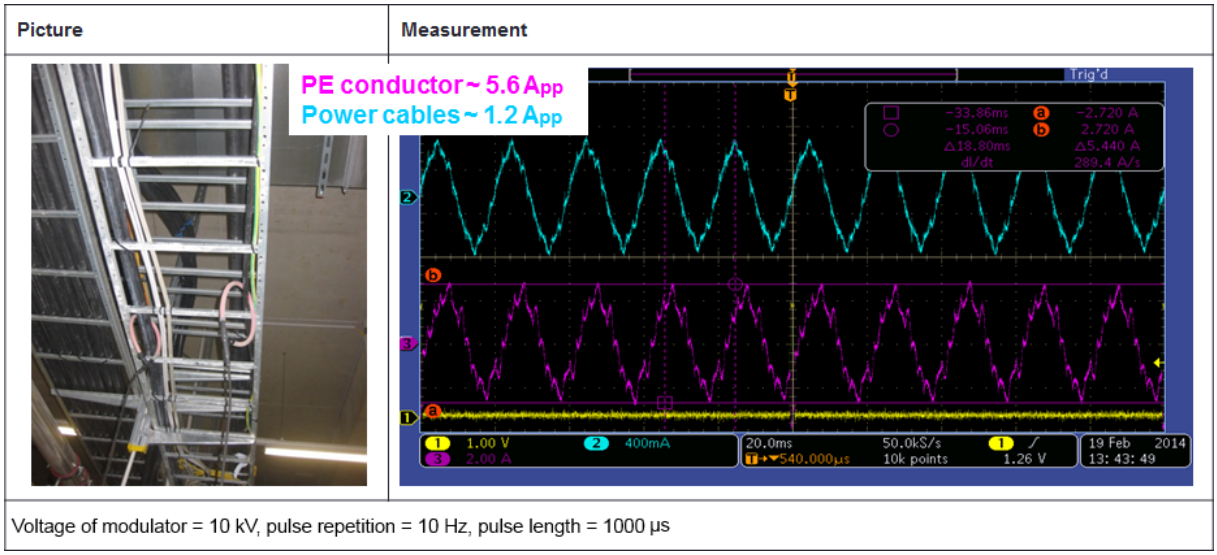


Fig. 19: Measurement with the PE conductor about 25 cm away from the power cables

4.2.5 Roundup

Simulations, supported by measurements, help in finding a advantageous grounding system for the modulators by allowing a choice of cables with better EMI rejection properties as well as optimizing the cabling for the grounding. In addition, simulations eliminate the costs of making modifications after installation.

4.3 Conclusion

4.3.1 Challenges in the world of simulation

Despite the huge improvements realized by building simulation tools in over the past few years, further improvements are welcome. Engineers can probably expand this list, but the following improvements in the world of simulation are still desirable for some simulation packages:

a) more intuitive software design to make the usage even easier;

b) faster models for lower simulation time;

c) models and results transfer between different simulation tools and operating systems;

d) better user support and extended online help;

e) lower licence costs.

4.3.2 Expectations for a good simulation tool

Some basic expectations for a good simulation tool comprise:

a) comfortable and intuitive schematic design;

b) easy interpretation of the error messages;

c) robust execution of the simulation;

d) simulation result formats which can be exported to other programs for further analysis;

e) good user support from the manufacturer;

f) portability of models from one program version to the following ones.

4.3.3 Checklist before opting for a simulation tool

There are many powerful simulation tools available, all of which have some advantages and disadvantages. A few guidelines useful for selecting a simulation tool that will meet your needs are listed in the following.

1) Before expending any effort researching simulation tools, the organization should commit to investing both the necessary money and staff time into purchasing and learning how to use a simulation software program. Depending on the type of simulation tool selected, the price for a single licence can be very expensive.

2) Perhaps the most important step in selecting simulation software is to state clearly the problem (or class of problems) that you would like to address. This must include a general statement about what you would like the simulation tool to do.

3) Because simulation is such a powerful tool, a wide variety of approaches and tools exist to assist in understanding complex systems and to support decision making. Before trying to survey all the available tools, you must first decide upon the general type of tool that you require (e.g., analog or numerical simulation).

4) This step involves developing a set of functional requirements that you would like the software tool to have. Note that requirements specify what the simulation software will do, not how. They should be as concise as possible (e.g., should be able to support a Monte Carlo simulation, a.c., d.c., transient, etc.).

5) An evaluation version of each product should eventually be obtained to test the software. Although this is necessary, it can be time consuming, since there will be a learning curve associated with each product.

4.3.4 Important points to achieve accurate simulation results

Regardless of the chosen type of simulation, accurate output results always depend on the following.

1) The simulation model should be as simple as possible—complex enough only to answer the questions asked.

2) A basic understanding of the real system is necessary. The expectation that the simulation tool will be 100% correct is wrong, and a lot of time can be spent realizing that.

3) The interrelation between the simulation model and the real system will help you to build an accurate model and to determine if the simulation results fit the physical system.

A famous quotation states: "Those who can, do. Those who cannot, simulate." But nowadays the complexity of power systems makes the basic understanding of the real system before simulation indispensable. Simulation does not replace understanding.

Acknowledgements

I wish to thank H.J. Eckoldt for the helpful discussions we had and for the enlightening comments on the present topic. My thanks also go to all my MKK colleagues, who have encouraged me after presenting this topic.

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Power Converters for Accelerators

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Abstract
Particle accelerators use a great variety of power converters for energizing their sub-systems; while the total number of power converters usually depends on the size of the accelerator or combination of accelerators (including the experimental setup), the characteristics of power converters depend on their loads and on the particle physics requirements: this paper aims to provide an overview of the magnet power converters in use in several facilities worldwide.

Keywords
Particle accelerators; magnet power converters; requirements; comparison.

1 Introduction

According to some recent statistics (2011) [1], there are about 30 000 particle accelerators operating in the world, mostly used for industrial (20 000) and medical (10 000) purposes. Scientific research applications are a small fraction of the total [2], as can be seen in Fig. 1 (data extracted from Ref. [3]).

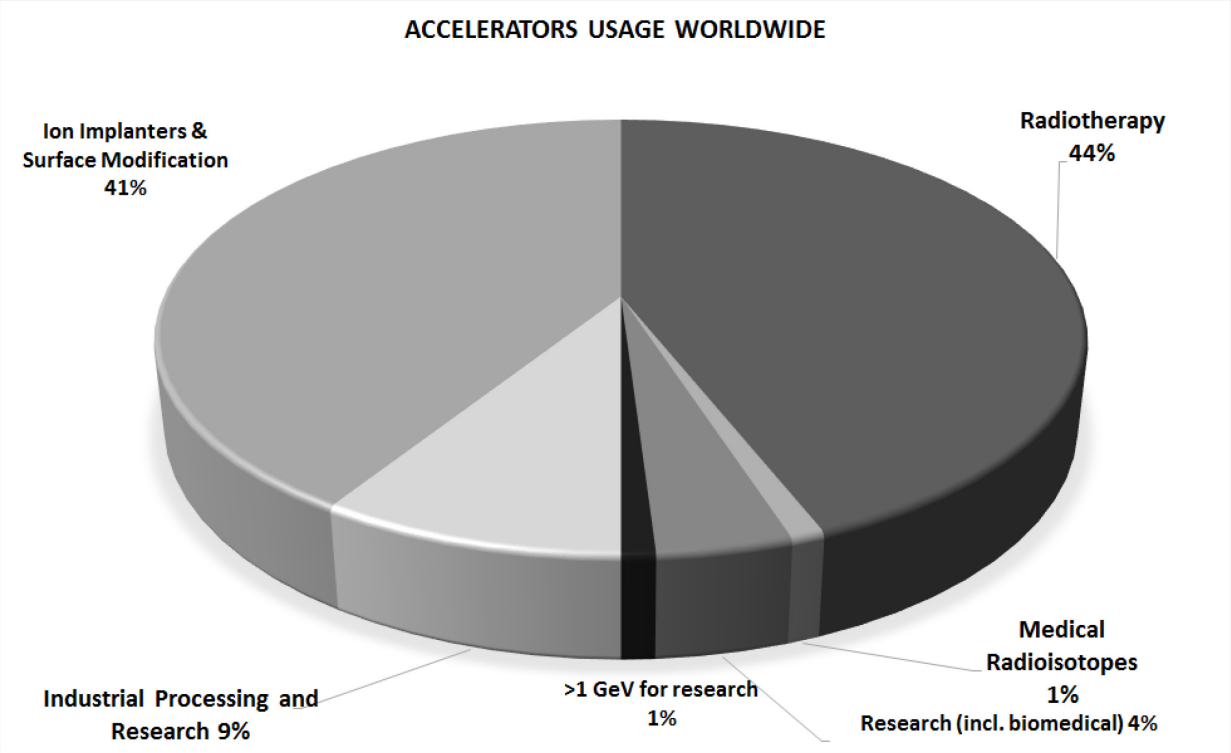


Fig. 1: Accelerators usage worldwide (2011)

http://dx.doi.org/10.5170/CERN-2015-003.415

Compared to the other applications, particle accelerators for scientific research quite often require ‘close-to-the-edge’ technologies and custom-designed equipment. Such devices (or solutions derived/inspired from them) can also find uses in industrial or medical applications.

1.1 Aim of this paper

The subsystems of accelerators, either a relatively small piece of equipment or a large structure, require a variety of power converters of different type, size, and performance. To somewhat limit the vastness of the field, only the accelerators related to scientific applications will be considered here.

During the specialized CAS course on power converters in 2004, H.-J. Eckoldt presented a lecture entitled ‘Different power supplies for different machines’. In his paper [4], focused on magnet power converters, he provided a good overview of technologies, topologies, and magnet connections to power converters in special applications, with many examples of solutions adopted by several facilities worldwide.

In this paper, I will try to integrate Eckoldt’s work, by presenting a comparison of the requirements of power converters (PC) for magnets, according to the different applications for particle accelerators (PA).

2 Particle accelerators

Several sources report the history of particle accelerators (see, for example, Ref. [5]). The first artificial source of accelerated ‘high’ energy particles (or, better, particles with energies higher than those obtainable from natural sources) is the accelerator constructed by J.D. Cockcroft and E.T.S. Walton in 1930 at the Cavendish Laboratory in Cambridge, England. It has to be noted that the researcher, Walton himself, as shown in Fig. 2, was sitting extremely close to the interaction point between particles and target (radiation issues were still to be investigated…).

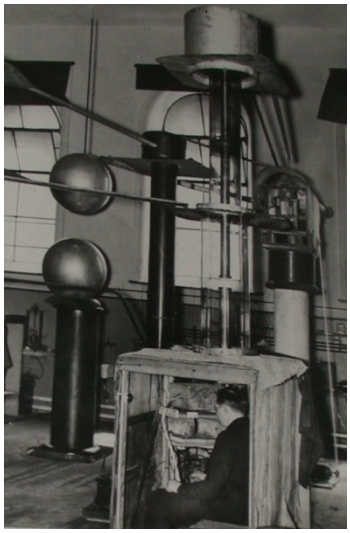


Fig. 2: Photograph of the first Cockroft-Walton machine, 1932 (Credit: Cavendish Laboratory, University of Cambridge).

The Cockroft-Walton machine was an electrostatic device, based on a voltage multiplier structure. Almost in parallel (1931), accelerators based on RF oscillators appeared: the linear accelerator (D. Sloan and E.O. Lawrence, starting from the work of R. Wideröe and G. Ising) and the first circular machine, the cyclotron, invented by E.O. Lawrence; see Figs. 3 and 4.

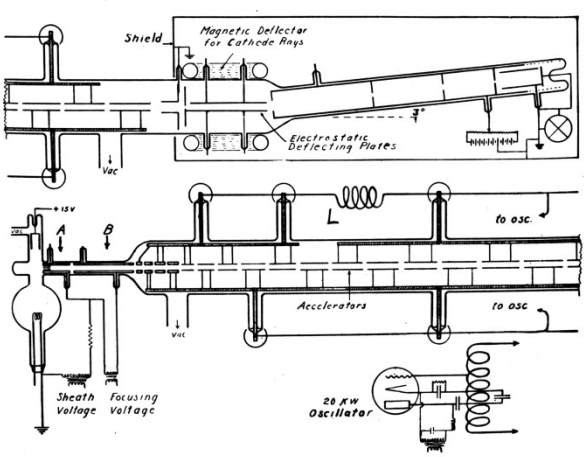


Fig. 3: Diagram of Sloan-Lawrence linear accelerator, (Credit: Lawrence Berkeley National Laboratory)

Fig. 4: E.O. Lawrence and his 5-inch cyclotron, the first successful cyclotron built by Lawrence and his graduate student M. Stanley Livingston, (Credit: Lawrence Berkeley National Laboratory).

These machines, along with the betatron and synchrotron, are the 'common ancestors' of the modern accelerators; and power converters played a key role since the very beginning.

2.1 Particle accelerator classification

One could organize the PA types in various ways. For the purposes of this paper, I consider the following structure:

- 'linear' or 'open', like LINACs or FELs;
- 'circular' or 'closed', like cyclotrons or synchrotrons.

The specific application is also an important criterion that is relevant for the required characteristics of the power converters:

- high energy physics colliders (HEP-C);
- ion sources/cancer therapy (IS/CT);
- neutron sources (NS);
- light sources (LS).

Independently from the structure—open or closed—and from the specific field of application there are some common actions between the different types of PA:

- production of particles;
- acceleration (increasing the energy) of particles;
- 'handling' of particles;
- measure the energy of particles.

2.2 Particle accelerators and power converters

The actions mentioned above are performed using specialized and dedicated equipment or complete subsystems that use power converters whose output could either be a current or a voltage; AC, DC or pulsed; high current, high voltage or both; low power—watts or kW, or high power—hundreds of kW or MW.

As anticipated in the Introduction, for several reasons magnet power converters are the object of this paper, beyond the obvious requirements of 'limiting' the field:

- in my opinion, the world of magnet power converters is fascinating[1];
- magnets are everywhere in a PA (magnetic lenses on guns, focusing coils on klystrons, solenoids on accelerating structures, magnets and coils, compensation or correcting coils on insertion devices, spectrometers, etc.);
- magnets can be normally conducting (warm) or superconducting (cold);
- magnets can be DC operated, AC operated (often with 'exotic' waveforms) or 'pulsed'.

2.2.1 The role of magnet power converters

Particle physicists (or 'machine physicists') study and define the characteristics of the particle beams according to the application (e.g. collider or light source). During and especially after the 'acceleration phases' of the particles, magnetic fields are normally used to 'shape' and drive the particle beams. Consequently, the characteristics of the magnetic fields have a great influence on the 'good quality' of the particle beams.

When electromagnets are used, there are two major issues to consider: the electromechanical design (materials, profile of the poles, shape of the coils, etc.), and the excitation current (ripple or harmonic content, stability, reproducibility, etc.). The power converters energizing the magnets play a key role in matching the required performance of the accelerator.

2.2.2 Physics, magnetics, power, control, plant: a system

A particle accelerator is a complex system: its performance also depends upon environmental constraints, like the stability of the ambient temperature where it is installed as well as the temperature of the rooms/galleries where the equipment—power converters, diagnostic electronics, etc.—are located.

Energy considerations—in particular for large facilities—have become strategic issues (see, for example, Refs. [6] and [7]). Magnets and the associated power converter designs are strictly interconnected activities, along with the specifications of the cables connecting them. Adopting a proper cross-section for the cables reduces the voltage drop on the cables, the output power required from the power converters and—from an operational point of view—allows for the reduction of costs.

[1]Once, when asked about my job at Elettra, I answered: "I'm providing particle physicists a tool to manipulate with micrometric precision, without any contact, almost immaterial and invisible particles travelling close to the speed of light".

Any watts dissipated in the magnet, power converter and cables are paid for twice: once from the mains to provide them and once from the cooling plant to remove them. Installation issues are also to be considered. Figure 5 summarizes some of the relevant interconnections among the different 'players'.

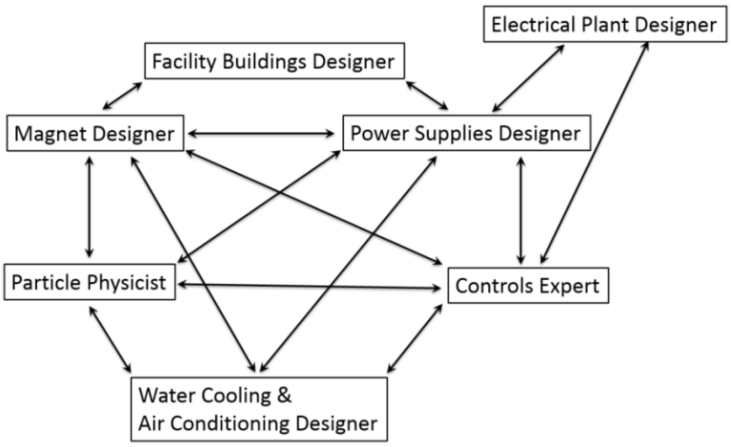


Fig. 5: Magnet, power converter, control, plant: a system

2.2.3 Some definitions

Before starting a detailed comparison of the characteristics required by the different applications among PAs, I want to recall some useful definitions.

2.2.3.1 Current stability

Current stability is a measure of long-term drift (a percentage of full-scale), over several hours at fixed line, load and temperature, after a warm-up period. Figure 6 shows a real-life example [8] of a stability test over more than 7 hours on a magnet power converter (750 A, 25 V) currently in use with the FERMI FEL source (see, for example, Refs. [9, 10]) at the Elettra Laboratory.

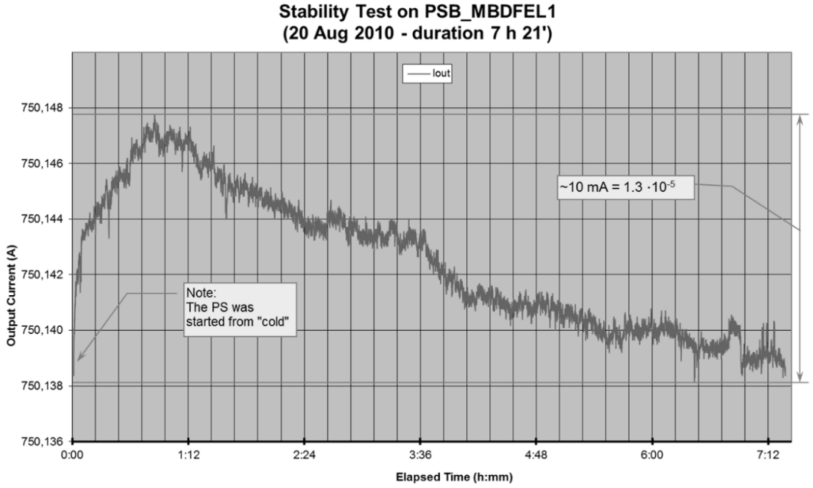


Fig. 6: Example of current stability test

2.2.3.2 Current ripple

This is noise on the output current specified as a percentage of the full scale. The frequency spectrum depends on the technology adopted and frequency of commutation of the switches.

2.2.3.3 Resolution (set and read-back)

This is the smallest possible steps for adjustment of the current set point or the current read-back, specified as a percentage of the full scale or number of bits.

2.2.3.4 Reproducibility

Reproducibility of the actual output current, for the same current set point (at different times) of a desired output value under constant conditions is specified as a percentage of the full scale.

2.2.3.5 Accuracy (set and read-back)

Accuracy is a measure of how close the actual output current is to the current set point or to the current read-back, specified as a percentage of the full scale.

3 Particle accelerators and magnet power converters

In the following sections I will describe many examples of magnet power converters in use in facilities worldwide, according to my classification as described in Section 2.1. Most of the information is derived from private communications and openly available sources, such as proceedings of particle accelerator conferences (see Ref. [11] for a complete list) or the web sites of the facilities. Images shown in the following sections have been taken from the facilities' web sites or free/open internet image banks through the courtesy of each facility. I have reported the photo credits, when available and required, in the captions.

The particle accelerators for scientific research applications are a small fraction of the total, nevertheless they are sufficiently numerous and the variety of power converter in use is so big to force me to limit the number of examples. I therefore apologize if when reading this paper you do not find your facility.

The examples refer to operational facilities or facilities under construction (at the time of writing) and the dates by their names indicate the start of commissioning/operation. I have tried to structure tables as uniformly as possible but there are differences between them due to the variety of formats adopted in the various documents and sources in describing the power converters and the available data. When not explicitly indicated, I have gathered the data reported via private communications.

3.1 High energy physics colliders (HEP-C)

The facilities in this field of applications are characterized by very high particle energies, in the Tera electronVolt (TeV) region) and very large dimensions (kilometres in circumference). There is a large use of superconducting magnets (and conventional ones, too); a very large number of magnet power converters of all types: high current, high voltage or both; low power—watts or kW—or high power—hundreds of kW or MW.

3.1.1 LHC (CERN, Switzerland, 2008 to 2009)

The LHC is the largest accelerator—actually a complex of accelerators, see Fig. 7—featuring several 'world records':

- highest particle energy, 7 TeV (3.5 TeV + 3.5 TeV);
- largest structure (27 km in circumference);
- largest cryogenic system in the world and one of the coldest places on Earth, main magnets operating at a temperature of 1.9 K (−271.3°C) [12];

– largest number of superconducting magnets (~9600);
– and more…

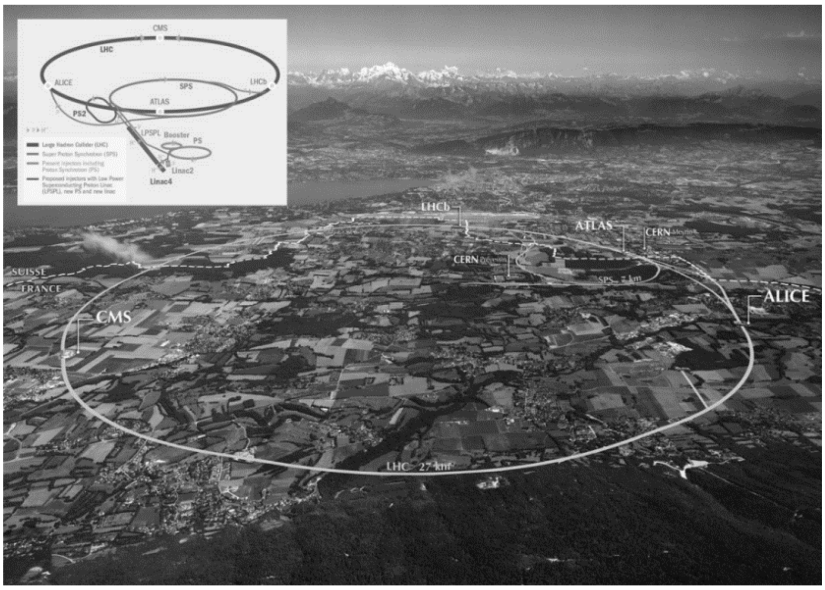


Fig. 7: The LHC (credit: CERN)

There are more than 1700 magnet power converters, either unipolar or bipolar (two- or four-quadrant), with currents as high as 13 kA. The technologies adopted are both thyristor rectifiers (silicon-controlled rectifiers - SCR) and switch mode (SM) with insulated-gate bipolar transistors (IGBTs) or metal oxide semiconductor field-effect transistors (MOSFETs). For large output current power converters, smaller units are connected in parallel. The power converters (PCs) are custom-made one, often collaborating with industries in developing the PCs. Since almost all PCs are located underground and are not easily accessible for maintenance and repair, reliability is a key parameter. Table 1 summarizes some of the characteristics of the magnet power converters for LHC.

Table 1: Summary of LHC magnet power converters

Power converter type	**Quantity**	**Switch type**[2]	**½ hour stability [ppm]**
MB [13 kA, ±190 V]	8	SCR	3
MQ [13 kA, 18 V]	16	SM	3
Inner triplet [5–7 kA, 8 V]	16	SM	5
IPD and IPQ [4–6 kA, 8 V]	174	SM	5
600 A type 1 [±0.6 kA/±10 V]	400	SM	10
600 A type 2 [±0.6 kA/±40 V]	37	SM	10
120 A [±120 A/±10 V]	290	SM	50
Orbit correctors [±60 A/±8 V]	752	SM	50
Warm magnets [1 kA/450–950 V]	16	SCR	20

[2] SCR – Thyristor bridge; SM – Switched Mode

3.2 Ion sources

Ion sources (IS) facilities requires a low particle energy (hundreds of MeV). The dimensions are in the order of hundreds of metres. The accelerators can be of different types (cyclotrons or LINACs), also in particular configurations. Since both superconducting and conventional magnets are used, there is a large variety and number of power converters.

3.2.1 FRIB (USA, under construction)

Citing the official web page of FRIB [13], it "will provide intense beams of rare isotopes—shortlived nuclei no longer found on Earth. FRIB will enable scientists to make discoveries about the properties of these rare isotopes in order to better understand the physics of nuclei, nuclear astrophysics, fundamental interactions, and applications for society. As the next-generation accelerator for conducting rare isotope experiments, FRIB will allow scientists to advance their search for answers to fundamental questions about nuclear structure, the origin of the elements in the cosmos, and the forces that shaped the evolution of the universe."

The layout is shown in Fig. 8. The facility uses linear accelerators organized in a 'paperclip' (or 'folded LINAC') structure to save space.

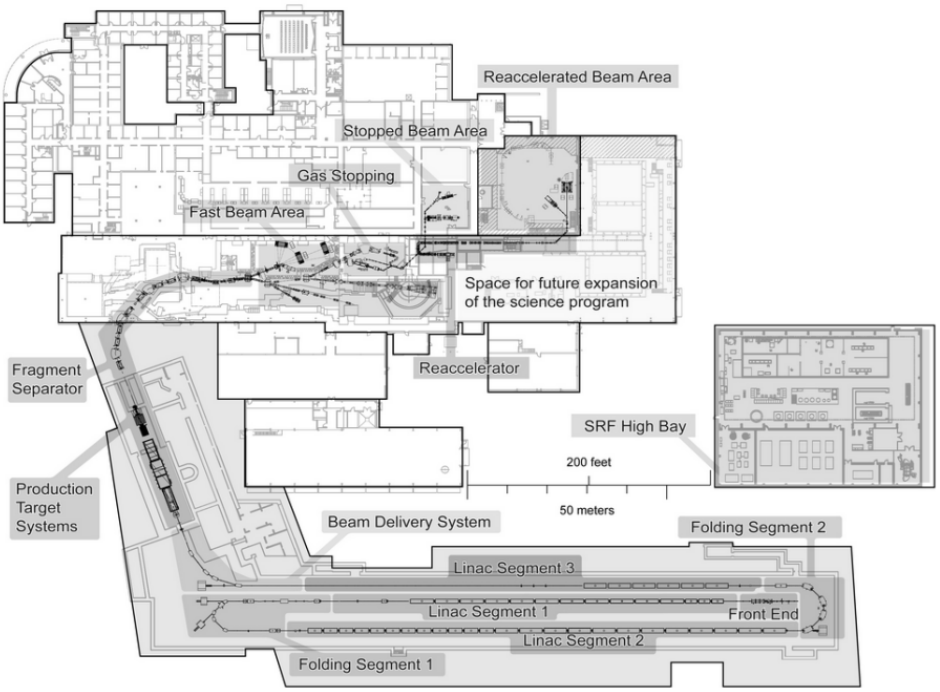


Fig. 8: FRIB layout (Credit: FRIB-MSU)

There is a large variety of magnetic—normal and superconducting—and electrostatic elements (dipoles and quadrupoles) to act on the particles, requiring either high voltages or high currents. From the power converter point of view, this translates in a mix of one quadrant (1-Q), two quadrant (2-Q) and four quadrant (4-Q) power converters (see Tables 2 and 3).

Table 2: FRIB electrostatic element power converters

Quantity	I_{out} [mA]	V_{out} [kV]	Long-term stability [ppm]	Ripple [ppm]	Accuracy [ppm]	Resolution [ppm]
11	1–60	1–100	±100–±500	100–200	1000	500

Table 3: FRIB magnetic element power converters

Quantity	I_{out} [A]	V_{out} [V]	Long-term stability [ppm]	Ripple [ppm]	Accuracy [ppm]	Resolution [ppm]
194	2–3500	6–600	±200–±1000	50–400	2500–4000	20–200

The relatively 'relaxed' parameters of some power converters allow the adoption of commercial units (so-called commercial-off-the-shelf (COTS), a solution that has some advantages in terms of costs, availability, reliability (units are produced in hundreds, over the years), maintenance and spares.

3.3 Cancer therapy

The centres for cancer therapy (CT) are, at the same time, an accelerator facility and a clinical facility: quite different environments, where technical, scientific, medical and psychological aspects coexist and have to be considered at the same time. This type of facility requires a low particle energy (hundreds of MeV). The dimensions are relatively small, in the order of tens of metres. The accelerators can be of different types (cyclotrons or synchrotrons). The power converters are of different types (SCR, PWM, linear) and their main requirements are high reliability (e.g. avoiding failures during treatment of patients) and minimization of repair time.

3.3.1 PROSCAN (PSI, Switzerland, 2007)

PROSCAN is a cyclotron-based facility for proton therapy within the Paul Scherrer Institute (PSI) in Villigen (see, for example, Ref. [14]); the layout is shown in Fig. 9. The proton beamlines are used for eye radiotherapy and deep-seated tumours. The proton source is the 250 MeV COMET cyclotron; its installation is shown in Fig. 10.

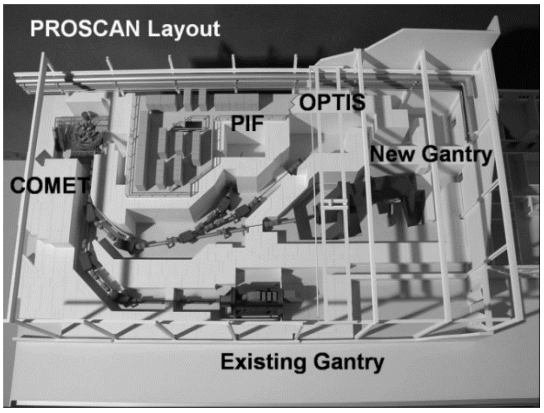


Fig. 9: PROSCAN Layout (Credit: PSI)

Fig. 10: The COMET cyclotron under construction in 2004 (Credit: PSI)

There are about 100 magnet power converters. They are all four-quadrant pulse-width modulation (PWM) type, and the main focus is on dynamics with tight requirements on d*i*/d*t* and regulation delays. Table 4 summarizes the parameters of the PROSCAN magnet power converters.

Table 4: PROSCAN power converters

Type	I_{out} [A]	V_{out} [V]	Long-term stability [ppm]	Ripple [ppm]	Reproducibility [ppm]	Accuracy [ppm]	d*i*/d*t* [A/s]
IGBT	500	350	100	50	100	500	125
IGBT	220	320		1000		1 000	11 000
IGBT	220	285	15	15	100	500	100
IGBT	150	175		1000		1 000	40 000
IGBT	150	90	100	50	100	500	100
MOSFET	50	50	500	100	500	500	
MOSFET	10	24	500	100	500	500	

3.3.2 CNAO (Italy, 2010 to 2012)

CNAO is a synchrotron accelerator (about 80 metres in circumference) where carbon ions or protons are accelerated and then driven to the treatment room. The protons are accelerated to 250 MeV while the carbon ions are accelerated to 480 MeV. Figure 11 shows the synchrotron ring.

Fig. 11: CNAO synchrotron (Credit: CNAO)

Table 5 summarizes the characteristics of the more than 200 magnet power converters [15]. It has to be noted that there are high voltage and high current requirements at the same time—requiring the adoption of a mixed technology: thyristor (SCR) bridges with switched mode active filtering on the DC side of the bridges [16], and high reproducibility.

Table 5: CNAO power converters

Magnet	Type	I_{out} [A]	V_{out} [V]	Long-term stability [ppm]	Ripple [ppm]	Reproducibility [ppm]	Resolution [ppm]
Dipole	SCR+SM AF	3000	±1600	±5	±5	±2.5	±5
Dipole	SCR+SM AF	3000	±110	±25	±25	±13	±25
Dipole	SCR+SM AF	2500	±450	±5	±5	±2.5	±5
Dipole	PWM	±550	±660	±200	±100	±100	±60
Dipole	PWM	±30–300	±20–±35	±50–±500	±50–±250	±25–±500	±50–±1000
Quadropole + sextupole	PWM	150–650	±17–±65	±50–±100	±50–±100	±25–±50	±50–±100
Corrector	Linear	±30–±150	±15–±30	±500	±250	±500	±1000

3.3.3 MedAustron (Austria, under construction)

MedAustron uses a synchrotron accelerator (about 80 metres in circumference) with a LINAC pre-accelerator for the ions. Proton or carbon ions are accelerated and then driven to the treatment rooms. The protons are accelerated up to 250 MeV (800 MeV for non-clinical research) while the carbon ions are accelerated up to 400 MeV [17]. Figure 12 shows the facility building and its layout.

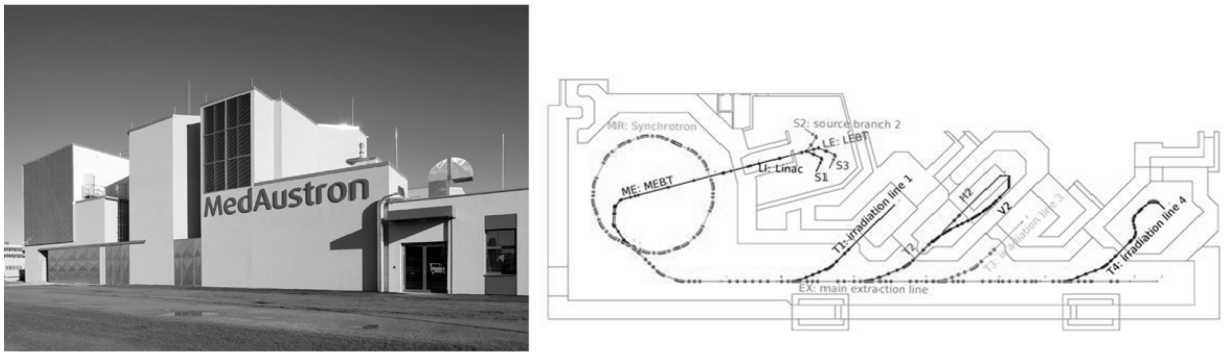


Fig. 12: MedAustron view and layout (Credit: MedAustron)

There are more than 200, four-quadrant, PWM power converters, operating at 0.5 Hz, with peak output power up to 4.5 MW. The precision range is between 10 ppm to 100 ppm. The power converters were specified to and provided by the manufacturers as voltage sources, while the high-precision current regulation system was designed and provided in collaboration by CERN and MedAustron [18].

3.4 Neutron sources

The production of neutrons from neutron sources (NS) requires linear or circular accelerators, of mid to low energy (0.8 GeV to 2.5 GeV) whose dimensions are in the order of some hundred metres or less. Neutrons are generated via spallation (a simple and clear description of the principle is given in Ref. [19]).

3.4.1 ISIS (RAL, UK, 1985)

ISIS [20] is a neutron source located in the Rutherford Appleton Laboratory (RAL) in the UK. It is based on a 800 MeV proton accelerator comprising a LINAC pre-accelerator and a synchrotron (165 m circumference) operated at 50 Hz, see Fig. 13.

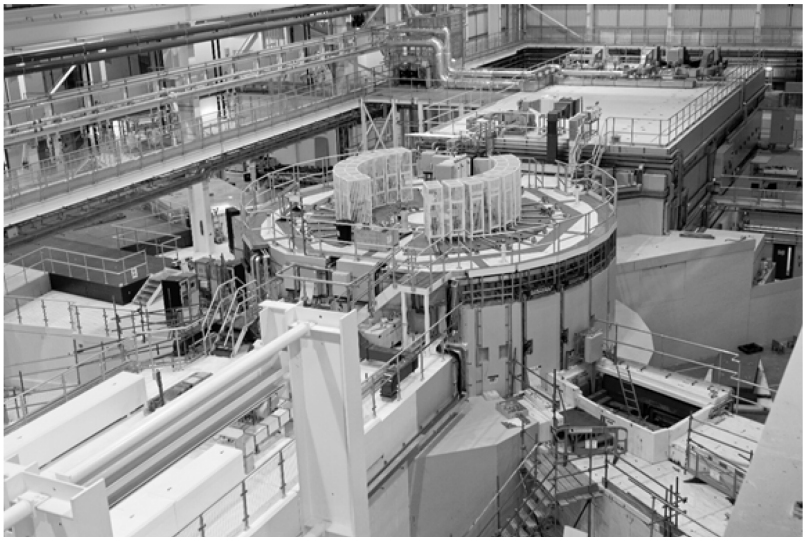


Fig. 13: ISIS (Credit: RAL, ISIS)

Operation at such a 'high' frequency, 50 Hz, imposes the adoption of a special configuration for the magnets and the associated power converters, the 'White circuit', from the name of the inventor (the original paper is Ref. [21]). At ISIS it consists of a 1 MJ resonant circuit with a DC bias power converter (660 A) and 4 × 300 kVA AC power converters, connected to a string of 10 chokes [22, 23], see Fig. 14. The rated secondary AC rms voltage is 14.4 kV at 1022 A.

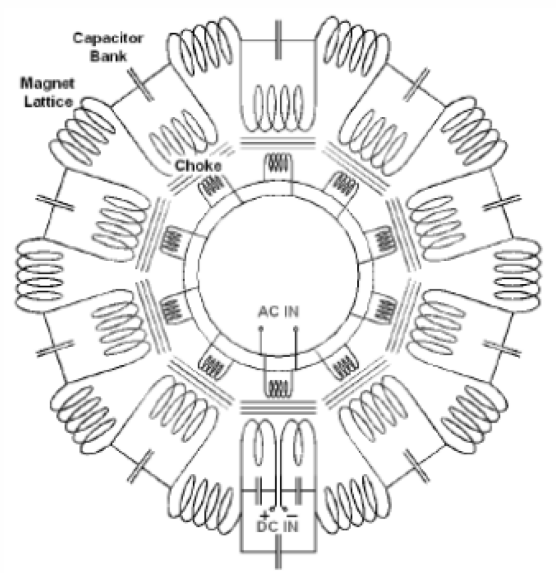


Fig. 14: ISIS White circuit layout from Ref. [22]

3.5 Light sources

Light sources (LS) utilize electrons to generate synchrotron radiation as a tool for research and are, usually, user-dedicated facilities (within an extremely vast literature, the properties of synchrotron radiation are described, in an unconventional but effective way, in Ref. [24]). They can be either 'circular'—the so-called 'storage rings'—or 'linear'—also known as the free electron laser (FEL).

Storage rings operate in the 1.5 GeV to 8 GeV range; they have dimensions of some hundreds of metres up to a few kilometres. They adopt either normal or superconducting magnets and—in particular for the most recent facilities—most of the magnets are individually energized, requiring a large number of power converters.

FELs operate at 1.5 GeV up to 20 GeV; the dimensions are ranging from some hundreds of metres up to a few kilometres; they use normal or superconducting magnets and they require a large number of power converters.

In the following paragraphs, I have briefly summarized the characteristics of the main magnet power converters of storage rings (SR, Sections 3.5.1 to 3.5.10) and free electron lasers (FEL, Sections 3.5.11 to 3.5.14). The year in parentheses by the name indicates the first stored electron beam or first electron beam along the whole structure.

3.5.1 Elettra (Italy, first e-beam 1993)

Elettra is a 'double energy facility': it regularly operates for users at 2.0 GeV (75% of the allocated beamtime) and 2.4 GeV (25% of the allocated beamtime) [25]. The storage ring circumference is 264 m and there are about 300 DC power converters adopting thyristor bridges for the main magnets and transistor-based bipolar linear topology for correctors [26, 27]. Table 6 summarizes the magnet power converters, while Fig. 15 is an aerial view of the storage ring building.

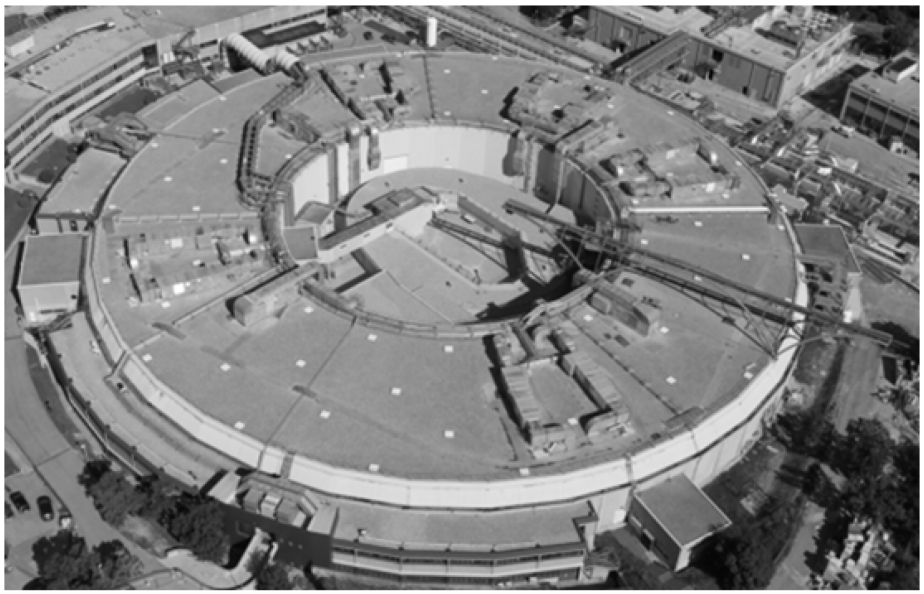


Fig. 15: Aerial view of the Elettra storage ring building (Credit: Elettra Sincrotrone Trieste)

Table 6: Elettra power converters

Magnet	I_{out} **[A]**	V_{out} **[V]**	**Long-term stability [ppm]**	**Ripple [ppm]**	**Resolution [ppm]**	**Type**
Dipole SR	2000	560	±200	±40	16	SCR
Quadrupole SR	300	560	±200	±40	16	SCR
Sextupole SR	300	560	±200	±40	16	SCR
Corrector SR	±16	±80	±500	±50	16	Bipolar linear

3.5.2 APS (USA, first e-beam 1995)

The Advanced Photon Source (APS) operates for users at 7 GeV [28]. The storage ring circumference is 1100 m and there are more than 1100 DC power converters adopting either thyristor bridges or PWM techniques. Table 7 summarizes the magnet power converters, while Fig. 16 is an aerial view of the facility.

Fig. 16: Aerial view of APS (photograph Tigerhill Studio, Argonne National Laboratory)

Table 7: APS power converters

Magnet	I_{out} **[A]**	V_{out} **[V]**	**Long-term stability [ppm]**	**Ripple [ppm]**	**Resolution [ppm]**
Dipole SR	550	750	±30	±40	16
Quadrupole SR	500	20	±60	±800	16
Sextupole SR	250	25	±300	±200	16
Corrector SR	±150	±20	±30	±1000	16

3.5.3 LNLS (Brazil, first e-beam 1997)

The UVX machine at LNLS operates for users at 1.37 GeV. The storage ring circumference is 93 m and there are about 200 power converters (DC and AC for the booster) adopting either thyristor bridges or PWM techniques [29]. Table 8 summarizes the magnet power converters, while Fig. 17 is a view of the UVX.

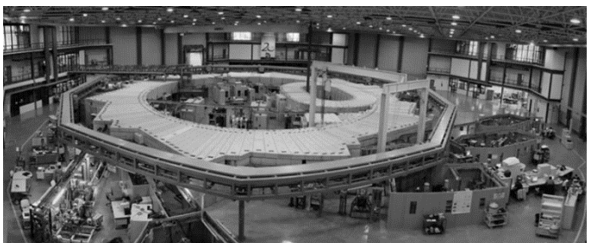


Fig. 17: View of UVX (Credit: LNLS)

Table 8: UVX (LNLS) power converters

Magnet	I_{out} **[A]**	V_{out} **[V]**	**Long-term stability [ppm]**	**Ripple [ppm]**	**Resolution [ppm]**	Type
Dipole SR	300	950	±100	±70	16	SCR
Quadruple + sextupole SR	10–220	10–45	±1000–±100	±1000–±100	16	SCR
Corrector SR	±10	±10	±1000	±100	16	Bipolar linear

3.5.4 SLS (PSI, Switzerland, first e-beam 2000)

The Swiss Light Source (SLS) operates for users at 2.4 GeV [30]. The storage ring circumference is 288 m and there are about 640 DC power converters. This is the first facility adopting an in-house developed fully digital regulation and control for the magnet power converters. Table 9 summarizes the magnet power converters, while Fig. 18 is a panoramic view inside the facility building.

Fig. 18: View of SLS (Credit: PSI)

Table 9: SLS (PSI) power converters

Magnet	I_{out} [A]	V_{out} [V]	Long-term stability [ppm]	Ripple [ppm]	Resolution [bit]	Accuracy [ppm]
Dipole SR	500	880	100	15	16	100
Quadruple + sextupole SR	70–140	35–145	100	40–100	16	100
Bipolar SR	±7	±24	100	15	18	1000

3.5.5 SSRL-SPEAR3 (USA, first e-beam 2003)

SPEAR3 operates for users at 3.0 GeV [31]. The storage ring circumference is 234 m and there are about 250 DC power converters, including the transfer lines. The large power converters adopt both thyristor or diode bridges and PWM; while the small power converters are PWM [32, 33]. Table 10 summarizes the magnet power converters.

Table 10: SPEAR3 (SSRL) power converters

Magnet	I_{out} [A]	V_{out} [V]	Long-term stability [ppm]	Type
Dipole SR	800	1200	20	12p SCR bridge + PWM
Quadruple SR	100	100–700	100	12p diode bridge + PWM/PWM
Sextupole SR	225	600	100	12p diode bridge + PWM/PWM
Corrector SR	±30	±50		PWM
Dipole TL	500	45	100	PWM
Quadruple TL	60	80	100	PWM

3.5.6 Soleil (France, first e-beam 2006)

Soleil operates for users at 2.75 GeV. The storage ring circumference is 354 m and there are about 350 DC power converters, including the transfer lines. The adopted technologies are 12-pulse bridge with PWM output stage for dipole and sextupole power converters and PWM for quadrupoles and correctors [34]. Table 11 summarizes the magnet power converters, while Fig. 19 is a panoramic view of the facility site.

Fig. 19: View of Soleil (Credit: Soleil)

Table 11: Soleil power converters

Magnet	I_{out} **[A]**	V_{out} **[V]**	**Long-term stability [ppm]**	**Resolution [ppm]**
Dipole SR	580	610	10	10
Quadruple + sextupole SR	250–350	14–140	20–50	5–50
Corrector SR	±7–±14	±3.5–±14	20–50	2–30
Dipole TL	250–580	20–80	50–100	60–100
Quadrupole TL	10–275	9–10	50–100	20–60
Corrector TL	±1.5–±10	±2.5–±9	100–500	60–100

3.5.7 Diamond (UK, first e-beam 2006)

Diamond Light Source (DLS) operates for users at 3.0 GeV. The storage ring circumference is 560 m and there are about 1000 DC power converters [35]. The adopted technology is PWM with digital regulation. Table 12 summarizes the magnet power converters, while Fig. 20 is a panoramic view of the facility site.

Fig. 20: View of Diamond (Credit: DLS)

Table 12: Diamond power converters

Magnet	I_{out} [A]	V_{out} [V]	Long-term stability [ppm]	Ripple [ppm]	Resolution [ppm]	Reproducibility [ppm]	Bandwidth [Hz]
Dipole SR	1500	530	±10	±10	4	10	DC
Quadruple + sextupole SR	100–350	17–41	±10	±10	4	10	DC
Corrector SR	±5	±20			4	10	50

3.5.8 ALBA (Spain, first e-beam 2010)

ALBA operates for users at 3.0 GeV. The storage ring circumference is 267 m and there are about 400 power converters (including those for the booster-based injector) [36]. The adopted technology is PWM with digital regulation. Table 13 summarizes the magnet power converters, while Fig. 21 is an aerial view of the facility site.

Fig. 21: View of ALBA (Credit: ALBA)

Table 13: ALBA power converters

Magnet	I_{out} [A]	V_{out} [V]	Long-term stability [ppm]	Ripple [ppm]	Resolution [ppm]
Dipole SR	600	750	±10	10	5
Quadrupole SR	200–225	15–25	±10	10	5
Sextupole SR	215	100–350	±50	50	15
Corrector SR	±12	±60	±20	10	5
Dipole TL	12–180	12–60	±15	15	15
Quadrupole TL	15–170	15–20	±15	15	15
Corrector TL	±2–±6	±2–±10	±100		100

3.5.9 PETRA III (DESY, Germany, first e-beam 2010)

PETRA started as an electron-positron collider during the 1980s, then it was used as the pre-accelerator for the high-energy HERA ring. After the closing of the latter, PETRA has been converted into a light source, with the construction of experimental halls for hosting photon beam lines [37]. With its circumference of 2.3 km, PETRA III is one of the largest storage rings in the world. The magnet power converters adopt different technologies and topologies (there are White circuits for the ramped magnets) with a mix of analog and digital regulation.

Figure 22 shows an aerial view of the facility and Table 14 reports the characteristics of the main magnet power supplies.

Fig. 22: PETRA III aerial view (Credit: DESY)

Table 14: PETRA III power converters

Magnet	I_{out} **[A]**	V_{out} **[V]**	**Ripple [V_{out} rms]**	**Accuracy [ppm]**	**Resolution [bit]**	**Type**
TL to PETRA	200–400	60–120	2–3	100	16	
Dipole AC	1004	1330		10	20	White circuit
Dipole DC	520	1560		10	20	White circuit
Quadrupole	650	250		10	20	White circuit
Sextupole	200	85		10	20	White circuit
Dipole PETRA	600	300	3	100 (30)	18	SCR
Quadruple + sextupole PETRA	200–600	60–120	2–3	100 (10)	20	PWM
Corrector PETRA	±5–±55	±40–±60	2–3	500 (10)	20	PWM

3.5.10 MaxIV (Sweden, under construction in 2014)

At the time of writing, MaxIV is under construction [38]. It is the most advanced circular light source, adopting innovative solutions, in particular for the magnets. The main storage ring (528 m in circumference) will operate at 3.0 GeV. A full-energy LINAC is the injector; and an intermediate, smaller storage ring, operating at 1.5 GeV, will be also part of the facility. Overall, about 1000 magnet power converters will be installed.

Figure 23 shows the construction of the main ring building while Table 15 reports the characteristics of the magnet power supplies for the MaxIV 3.0 GeV main ring.

Fig. 23: MaxIV under construction (Credit: MaxLab)

Table 15: MaxIV main ring power converters

Magnet (3 GeV)	**I_{out} [A]**	**V_{out} [V]**	**Long-term stability [ppm]**	**Ripple [ppm]**	**Resolution [ppm]**	**Accuracy [ppm]**
Main dipole	450–750	145–210	±10	±10	16	±100
Dipole strip	175	44–80	±1000	±1000	16	±1000
Quadrupole	44–85	9–44	±100	±10.0	16	±1000
Sextupole	66–86	8–20	±100	±100	16	±1000
Octupole	58–217	45–104	±100	±100	16	±1000
Corrector SR	±5	±8	±25	±25	18	

3.5.11 LCLS (SLAC, USA, first e-beam 2009)

The final 1000 m of the 2.7 km-long SLAC LINAC are the accelerator for the Linac Coherent Light Source (LCLS), currently (2014), "the world's most powerful X-ray laser" [39], providing electrons at 13.6 GeV [40].

The magnet power converters parameters for the injector are reported in Table 16 [41]. Figure 24 shows some of the FEL undulators.

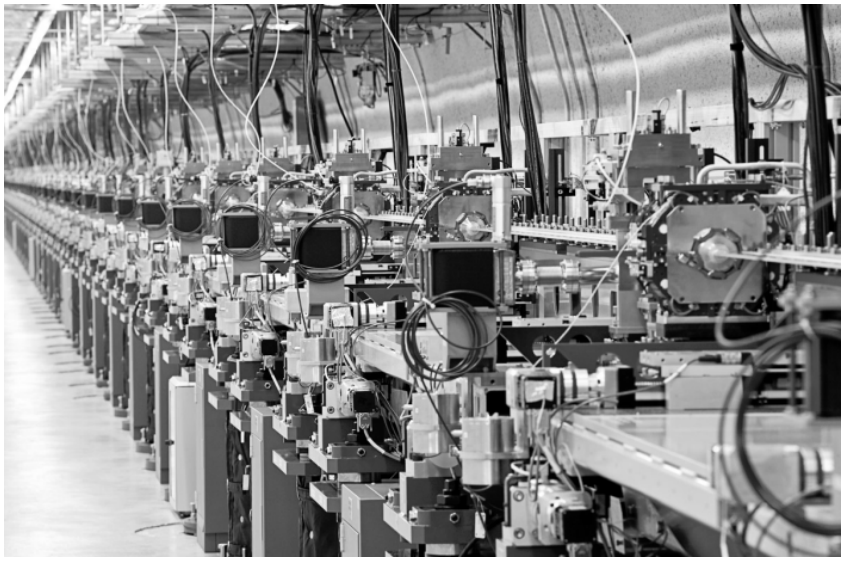


Fig. 24: Undulators at LCLS (Credit: LCLS-SLAC)

Table 16: LCLS power converters

Magnet	I_{out} [A]	V_{out} [V]	Long-term stability [ppm]	Ripple [ppm]
Intermediate PC	Up to 375	Up to 200	100 rms	100 rms
Corrector	±6–±30	±40	400 rms	30 rms

3.5.12 FERMI (Italy, first e-beam 2011)

After the construction and commissioning of the booster-based full injector for the Elettra storage ring in 2008, the 1 GeV LINAC and its plants have been re-used as part of the FERMI FEL source (360 m overall length). The construction of FERMI was completed in 2010, without affecting Elettra operation for external users, notwithstanding the proximity of the two sources, as can be seen in Fig. 25 (FERMI is the line stretching from the bottom to the top of the image on the left-hand side, almost tangential to Elettra's circular building). The energy of the electrons is 1.5 GeV and there are two undulators lines: FEL-1 to generate light in the vacuum UV (VUV) region (down to 20 nm), on the right-hand side in Fig. 27; FEL-2 provide light in the X-ray region between 20 to 4 nm (the undulators are on the left-hand side in Fig. 26) [42].

Fig. 25: Aerial view of FERMI and Elettra (Credit: Elettra Sincrotrone Trieste)

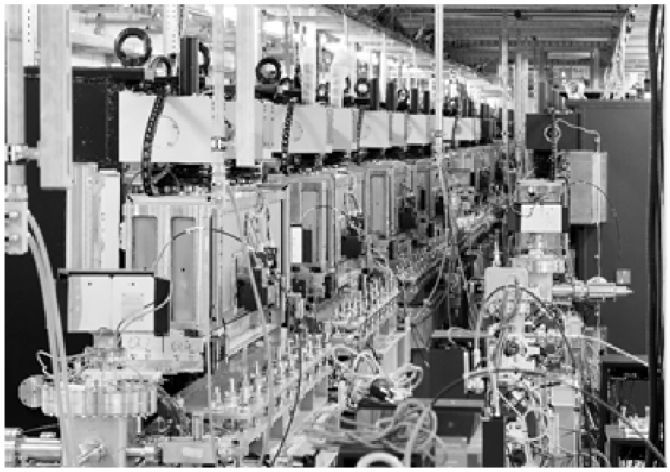


Fig. 26: FERMI undulators for FEL-1 (right) and FEL-2 (left) (Credit: Elettra Sincrotrone Trieste)

There are 37 different types of magnets and coils, supplied by 17 different types of DC power converters (~400 in total). A close collaboration between the magnet and the power converter teams could optimize the design, allowing the use of two types (in-house design) of power converters for 88% of the magnets. All power converters are of the PWM type and are custom-made and of commercial manufacture (COTS) and based on an internal design (bipolar ±5 A and ±20 A). Table 17 reports the characteristics for the magnet power converters [8, 43].

Table 17: FERMI power converters

Magnet	I_{out} **[A]**	V_{out} **[V]**	**Long-term stability [ppm]**	**Ripple [ppm]**	**Resolution [bit]**
Dipole	50–750	15–55	500	100	16
Quadrupole	5–100	10–30	25–500	10–100	16
Corrector	±5–±20	±10–±20	25–30	10–15	16

3.5.13 SwissFEL (PSI, Switzerland, under construction in 2014)

SwissFEL is the new source under construction (2014) at the Paul Scherrer Institut [44]. It is a free electron laser operating with electrons with a maximum energy of 5.8 GeV. The overall length is 740 m and there are ~600 magnet power converters. A feedback system involving correctors for the compensation of slow drifts is planned. Table 18 presents the main characteristics for the power converters.

Table 18: SwissFEL power converters

Type	I_{out} **[A]**	V_{out} **[V]**	**Ripple (10 Hz–30 kHz) [ppm]**
1-Quadrant IGBT	220	40–100	50
4-Quadrant IGBT	±150–±200	±40–±1100	3.5–50
4-Quadrant MOSFET	±10–±50	±10–±20	10–100

3.5.14 European XFEL (DESY, Germany, under construction in 2014)

The European XFEL will stretch underground for about 3.4 km, accelerating electrons at 17.5 GeV (up to 20 GeV) with a superconducting LINAC [45]. The power converter will adopt different technologies and topologies, with digital regulation (analog for correctors).

Figure 27 shows the position of the European XFEL while Table 19 summarizes the parameters of the magnet power converter.

Fig. 27: XFEL position (Credit: European XFEL)

Table 19: European XFEL power converters

Magnet	I_{out} **[A]**	V_{out} **[V]**	**Ripple [V_{out} rms]**	**Accuracy [ppm]**	**Resolution [bit]**	**Type**
Main	600–800	200–350	1% fs	100	20	SCR
Chopper	200–600	60–120	1.5–3	100	20	PWM
Small main	5–10	40–60	2–3	100	20	PWM
Corrector	±5–±10	±40–±60	2–3	100	20	PWM

3.6 Booster synchrotrons and light sources

In modern 'circular' light sources, a gun, usually followed by a LINAC, emits and pre-accelerates the electrons, and then a 'booster synchrotron' increases their energy. There are exceptions, such as MaxIV [38], but normally a relatively small ring (compared to the main or storage ring) is used to ramp up the electrons to working energy. The booster usually operate at frequencies of 1–12 Hz. The current in the magnets—always positive, never changing sign—follows a sinusoidal waveform with a DC offset. Due to the inductance of the load and the cycling frequency, the power converters have to operate in two-quadrant mode for the output voltage, up to several kV.

From 1956 to 1998, the basic magnet/power converter structure for generating similar current/voltage waveforms has been the White circuit [21]. In 1998, at the EP2 Conference at ESRF, Grenoble, the PSI power converter team presented their design for the dipole power converter for the Swiss Light Source [46]. This solution adopted a digitally controlled and regulated, 1 MW peak, PWM power converter operating at 3 Hz, at a comparably 'low voltage', i.e. below 1 kV, providing the required current waveform to the magnets directly, without any resonating circuit. The cycling frequency is 'low'—below 5 Hz—but one of the main advantages is the possibility of generating non-sinusoidal waveforms for better matching the particle optics requirements [47] (the White circuit can only provide sinusoidal waveforms).

In the sections below I will provide a few examples of the power converters for booster magnets, before and after 1998, starting with the last installed White circuit in a European light source, BESSY II at the Helmholtz-Zentrum Berlin (HZB).

3.6.1 BESSY II (HZB, Germany, first e-beam 1998)

The structure of a White circuit is shown in Fig. 28, while the parameters for the White circuit power converters are summarized in Table 20 [48].

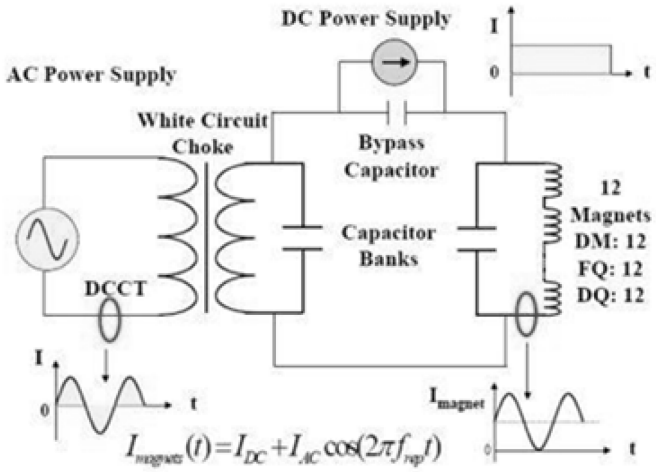


Fig. 28: White circuit schematics

Table 20: BESSY II White circuit power converters

Magnet	I_{out} [A]	V_{out} [V]	Long-term stability [ppm]	Peak values on magnet circuit at 10 Hz
Dipole AC	778	311		
Dipole DC	1375	120	±20	2277 A / 3112 V
Quadrupole AC	200	184		
Quadrupole DC	340	70	±20	492 A / 527 V

3.6.2 SLS (PSI, Switzerland, first e-beam 2000)

The SLS booster is the first implementation of a direct connection of power converters to the magnets. This is also the first example of digital control and regulation for the power converters. The working frequency is 3 Hz, the energy ramping is from 100 MeV to 2.7 GeV and there is one power converter for the dipoles [46]. Table 21 summarizes the main characteristics for the power converters.

Table 21: SLS booster power converters

Magnet	I_{out} [A]	V_{out} [V]	Long-term stability [ppm]	Ripple [ppm]
Dipole	950	±1000	100	10
Quadrupole	140	±120	100	100

3.6.3 LNLS (Brazil, first e-beam 2001)

The booster for UVX can be used also as a storage ring, at an intermediate energy. The repetition rate is 1 pulse every 6 s, ramping the energy of the electrons from 120 MeV up to 500 MeV. Table 22 reports the main parameters for the LNLS booster magnet power converter [49].

Table 22: LNLS booster power converters

Magnet	I_{out} [A]	V_{out} [V]	Short-term stability [ppm]	Ripple [mA]
Dipole	300	420	10	±120
Quadrupole	10	21	10	±10
Sextupole	10	26	10	±10
Corrector	±5–±6	±10	10	±1

3.6.4 Soleil (France, first e-beam 2001)

The Soleil booster has a repetition rate of 3 Hz, ramping the energy of the electrons from 100 MeV to 2.75 GeV. Due to the inductance of the magnets, in order to keep the peak voltage of the power converters below 1 kV, allowing the adoption of low-voltage techniques and rules, two separated power converters energize the dipole, with an 'twisted' connection of the coils, as reported in Fig. 29. Table 23 reports the main parameters for the magnet power converter of the Soleil booster [34].

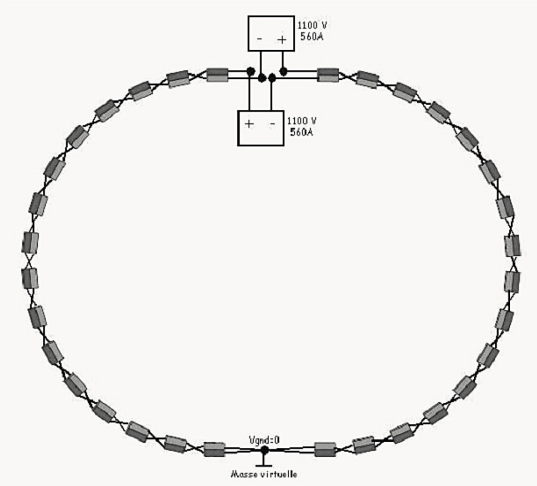


Fig. 29: Dipole magnet arrangement in the Soleil booster

Table 23: Soleil booster power converters

Magnet	I_{out} [A]	V_{out} [V]	Accuracy [ppm]	Number of PCs
Dipole	±580	±1000	50	2
Quadrupole	±250	±450	50	2
Sextupole	±30	±30	50	2
Corrector	±1.5	±2.5	50	44

3.6.5 Diamond (UK, first e-beam 2005)

The Diamond booster has a repetition rate of 3 Hz (5 Hz maximum), ramping the energy of the electrons from 100 MeV to 3 GeV. In this case, the dipole string was not split and there is only one power converter. Due to the inductance of the dipoles, the peak voltage is 2 kV, forcing the adoption of mid-voltage techniques and rules. The design of the power converters is modular, with redundancy, allowing continuity of operation even in the case of a single module failure.

Table 24 reports the main parameters for the Diamond booster magnet power converters [50].

Table 24: Diamond booster power converters

Magnet	I_{out} [A]	V_{out} [V]	Reproducibility [ppm]	Resolution [ppm]	Number of PCs
Dipole	1000	±2000	±50	±4	1
Quadrupole	200	±421	±50	±4	2
Sextupole	20	±60			2

3.6.6 Elettra (Italy, first e-beam 2007 to 2008)

A 1.0 GeV LINAC was the original injector for the Elettra storage ring. Between 2005 and 2007 a new full-energy injector was constructed and commissioned, without affecting the operations of the light sources for users [51]. Since March 2008 the 2.5 GeV booster, fed by a 100 MeV LINAC, is the full-energy injector for Elettra. Since 2010 Elettra operates in the so-called 'top-up' mode, keeping the current in the storage ring constant [25].

The Elettra booster has a circumference of 114 m, operates at 3 Hz, and, in a similar fashion to Soleil, there are two dipole magnet power converters, feeding the coils of the magnets separately, as shown in Fig. 30. An example of the actual current waveforms is given in Fig. 31. Table 25 summarizes the power converter parameters [52].

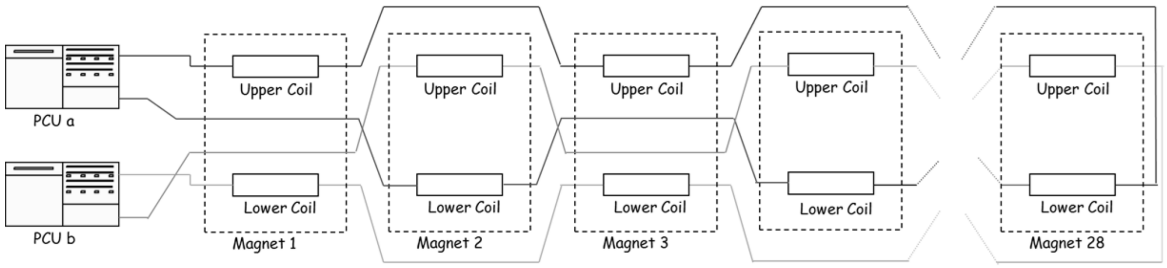
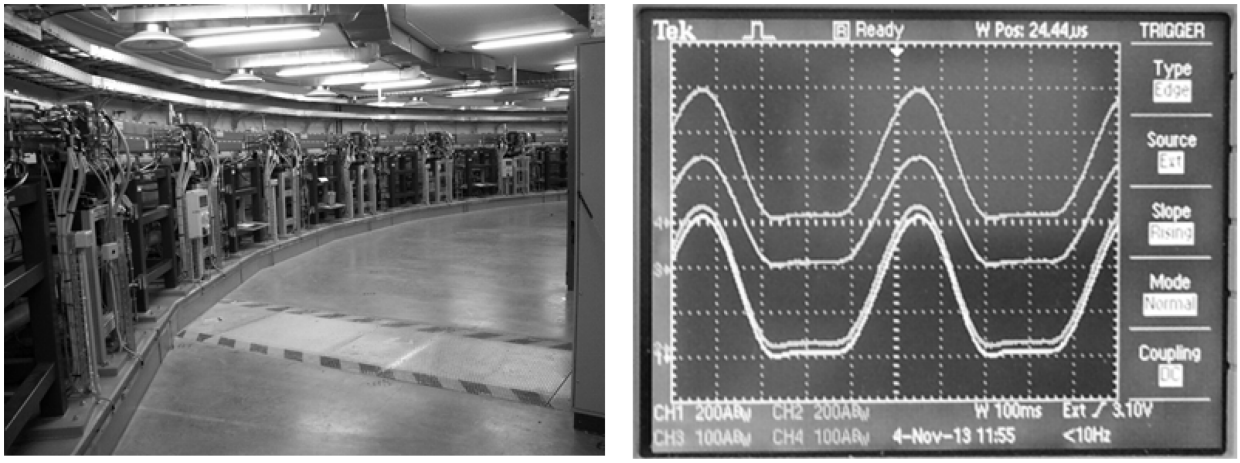


Fig. 30: Dipole magnet arrangement for the Elettra booster



(a) (b)

Fig. 31: View of (a) the Elettra booster; (b) output current waveforms in the magnets. In (b) from top to bottom: quadrupole QD (100 A/division), quadrupole QF (100 A/division), dipoles 1 and 2 (200 A/division).

Table 25: Elettra booster power converters

Magnet	I_{out} [A]	V_{out} [V]	Stability [ppm]	Number of PCs
Dipole	±800	±1000	±5	2
Quadrupole	±400	±400	±50	2
Sextupole	±20	±35	±50	2
Corrector	±20	±50	±50	22

3.6.7 ALBA (Spain, first e-beam 2010)

The booster of ALBA has a repetition rate of 3 Hz, ramping the energy of the electrons from 100 MeV to 3 GeV. Also in this case, in a fashion similar to Soleil and Elettra, two separated power converters energize the dipole, with a 'twisted' connection of the coils

Table 26 reports the main parameters for the magnet power converter of the ALBA booster [53].

Table 26: ALBA booster power converters

Magnet	I_{out} [A]	V_{out} [V]	Stability [ppm]	Resolution [ppm]	Reproducibility [ppm]	Number of PCs
Dipole	±750	±1000	±15	5	±50	2
Quadrupole	±180	±120–±750	±15	5	±50	4
Sextupole	±8	±70	±50	15	±100	2
Corrector	±6	±12	±50	15	±100	72

4 Remarks and conclusions

In this paper, I have collected some examples of magnet power converters from quite a vast world of particle accelerators. It is quite straightforward that there are different requirements among particle accelerators for different applications. Maximum output current, its stability, its reproducibility, its accuracy and its dynamics (di/dt) are some of the most variable parameters. There are also significant differences among particle accelerators that have the same applications, according to the accelerator's type and age.

New technologies, both in the power converter field (components, low-level/local control) and in the feedback and remote control systems at a higher level, are also sources of change. In particular, new technologies allow extremely effective actions on the particle beam, like beam-based alignment (BBA) techniques for both circular ('multi-turn') machine and linear ('single-pass') ones[3]. The implementation of feedback systems—either on the 'orbit' or on the 'trajectory'—also benefits from new developments involving particle beam position monitors (BPM), very fast electronics, high computational power and a combination corrector magnet/power converter for compensating drift or oscillation of the particle beam with a bandwidth as large as possible.

3 The bibliography on BBA is quite vast: a simple search in the JACoW database [11] returned 64 results for titles containing the words 'beam-based alignment'

4.1 Storage ring correctors for light sources

As an example, in Table 27 I have collected the relevant data for the power converters for corrector magnets of the storage rings of eight synchrotron light sources. Two critical aspects of the corrector power converter assure smooth behaviour near 0 A: the so-called 'zero crossing' (0 A is a normal working point) and bandwidth. Bipolar, linear solutions can fulfil these requirements; the main drawback is poor efficiency. Such power supplies are still in use, at least at Elettra, and have been integrated into local and global 'fast feedback' system for stabilizing the particle beam (see, for example, Refs. [54, 55]).

A clear step was evident after 2000 with the adoption of PWM techniques for correctors, introducing digital regulation and a higher resolution. The output current is smaller, compared to the previous cases, because of an optimized design of the system magnet/power converter for the purpose and the characteristics of the accelerator (e.g. smaller transverse beam size, allowing a smaller gap in the magnet).

Table 27: Storage ring corrector power converters

Facility (first year of operation)	Beam energy [GeV]	I_{out} [A]	V_{out} [V]	Long-term stability [ppm]	Ripple [ppm]	Resolution [bit]	Type
Elettra (1993)	2.4	±16	±80	±500	±50	16	Bipolar linear
APS (1995)	7	±150	±20	±30	±1000	13	
LNLS (1997)	1.37	±10	±10	±1000	±100	16	Bipolar linear
SLS (2000)	2.4	±7	±24	100	15	18	PWM
Soleil (2006)	2.75	±7–±14	±3.5–±14	20–50		16–18	PWM
DLS (2006)	3	±5	±20			18	PWM
ALBA (2010)	3	±12	±60	±20	10	18	PWM
Max IV (…)	3	±5	±8	±25	±25	18	PWM

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I also wish to thank the following companies for having provided me—anonymously, for reasons of confidentiality—material on the power supplies they have built for particle accelerators: Bruker/SigmaPhi Electronics, EEI and OCEM.

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As reported in the JACoW section on the IPAC 2012 web site (http://www.ipac12.org/jacow.htm), *"In 1996, the Joint Accelerator Conferences Website, JACoW was set up for the publication of EPAC and PAC conference proceedings. As this PAC/EPAC collaboration got underway, it was joined by APAC for its first conference in 1998. Today, sixteen conference series are members of the JACoW*

Collaboration: BIW, COOL, CYCLOTRONS, DIPAC, ECRIS, FEL, HIAT, ICALEPCS, ICAP, ICFA ABDW, IPAC, LINAC, NA-PAC, PCaPAC, RuPAC and SRF".

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Synchrotron light facilities: http://www.lightsources.org/regions

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Putting it into Practice

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Abstract
This paper presents the latest trends in the powering of particle accelerators. A series of solutions is proposed for responding to the challenges of high performance machines. This paper covers the domains of magnetic field uncertainty, power converter control, and energy saving. This list is not exhaustive, but it does correspond to the latest innovations in the field of powering particle accelerators.

Keywords
Magnet Power supply; power electronics; power converter control.

1 Introduction

Particle accelerators are very challenging machines in terms of powering. Many solutions had to be found to operate these machines at the required level of performance. Thanks to the experience accumulated, synchrotron performance is well above that of the first designs of the 1950s. For example, the PS machine, built in 1957 at CERN, was designed for an intensity per pulse of 10^{10} protons and, after 50 years and with many upgrades, in 2013 reached 3×10^{13} protons [1]. Power performance acts directly on the global performance of the synchrotron. The stability and reproducibility of the power converters are crucial for beam performance; this explains why particle accelerators need high-precision power converters. This paper will underline some important parameters regarding machine performance and describes the associated solutions put into place.

2 Magnetic field uncertainty

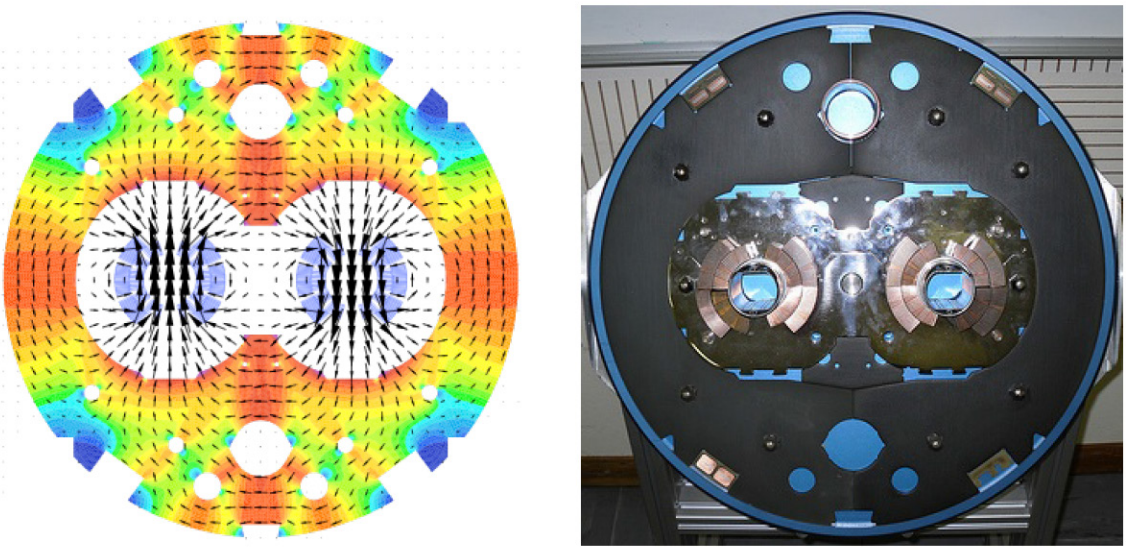
Magnetic field uncertainty generates many difficulties when operating a machine, especially when the machine is working with different beam energies. The magnetic field is very difficult to measure at an order of magnitude of 10^{-4}, which unfortunately is mandatory for the control of particle accelerators. The classical way to control the magnetic field is to measure the DC current delivered by power converters. Based on these measurements, the operators can determine the beam energy. In most synchrotrons, all of the magnets (dipole, quadrupole, sextupole, and correctors) are current controlled, and the beam energy is controlled by the dipole magnet current. The stability of the magnet current and its reproducibility are very important for beam control and stability. For example, a machine can suffer from tune spread due to current ripple in the quadrupole magnets. Magnetic modelling is also a key technique to improving predictions, see Fig. 1.

2.1 Circuit layout

The first solution to ease the operation of synchrotrons is to connect in series all of the magnets by family (dipole, quadrupole, or sextupole). Thank to this layout, the magnetic field is expected to be identical for all of the magnets of any one family, which suppresses the uncertainty of the magnetic field, depending upon their position inside the machine. The impedance of the circuits is also more inductive, which helps to reduce the current ripple. However, in some cases this layout isn't possible due to the size of the machine (as for the LHC) or due to the rigidity introduced in the beam optics (as

http://dx.doi.org/10.5170/CERN-2015-003.445

for light sources). In these cases the quality of current measurement and current control has to be even better, to obtain the required performance for the machine [2].

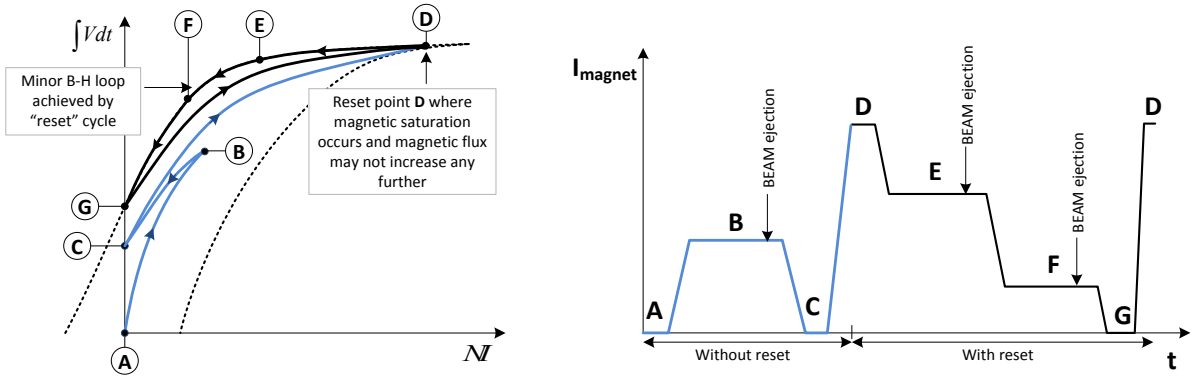


(a) (b)

Fig. 1: (a) Magnetic field in a dipole magnet; (b) and cross-section through a LHC dipole

2.2 Degauss and pre-cycle

All magnets need a proper pre-cycling to have reproducible behaviour, i.e. to provide the same field at the same level of current. Depending on the type of magnet, the type of pre-cycle stems from different physical phenomena, and reproducibility can be obtained through different pre-cycle strategies [3]. For a predicable magnetic field value, it is imperative to follow a specific path on the magnetization curves so that any cycle will arrive at a predictable and repeatable value despite the hysteresis in flux changes. Figure 2 explains how the magnets can be driven to always operate on a known magnetization curve. The idea is to use the magnetization curve from a stable point; and the only stable point is when the magnet is saturated. All degauss cycles need to go to the maximum current to start the prediction from a constant point.



(a) (b)

Fig. 2: (a) The magnetic flux intensity versus magnetic flux density in a typical magnet; (b) evolving as the magnet current is varied following a typical waveform. Operation without the reset cycle is in blue. The desired 'predictable' operation around a minor B-H loop is in black.

Different types of pre-cycles can be executed. For magnets that always operate at the same beam energy, the classical five pre-cycles can be executed, see Fig. 3. This is the case for beam transfer lines with fixed energy and the LHC warm magnets.

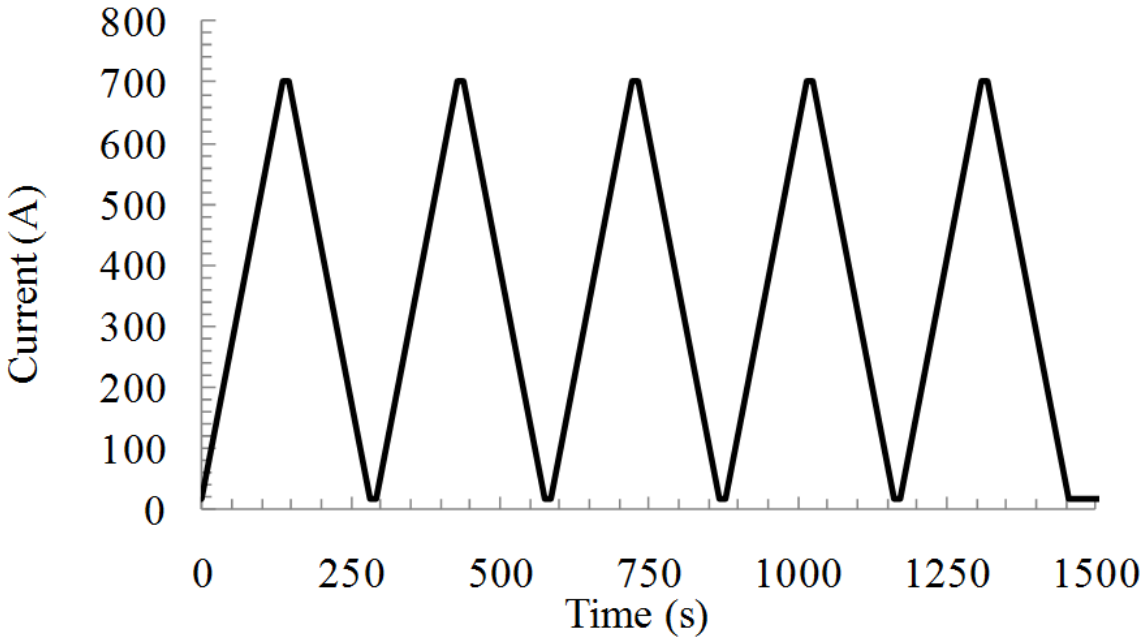


Fig. 3: Pre-cycles for LHC warm magnets

When, a transfer line is used at different beam energies, pre-cycles can't always be executed between changes due to time limitations. The degauss is then much more complex and needs advanced techniques. The solution implemented at CERN is to power the magnet at the maximum current for some cycles and then ramp down the current to the nominal value of the beam energy, see Fig. 4.

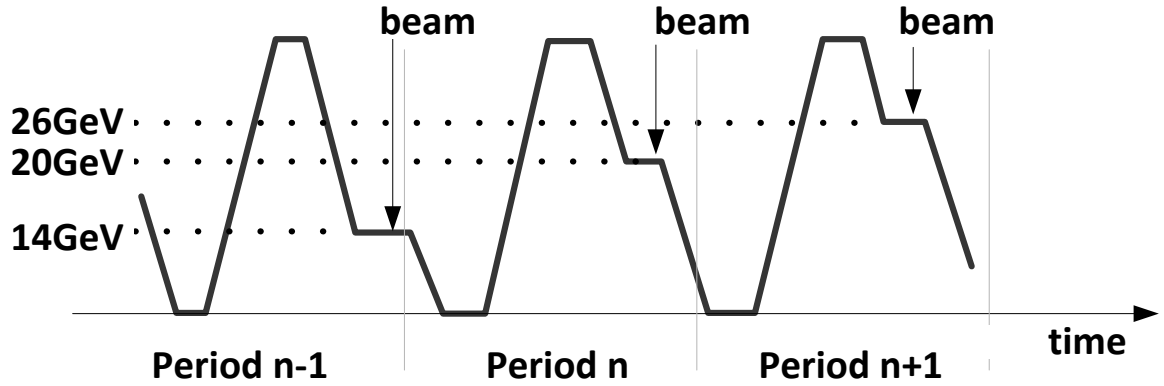


Fig. 4: Degauss technique for transfer lines with different beam energies

When the power converters are bipolar in current, the pre-cycle can be done by using an oscillation current shape that allows resetting to zero the magnetic field, see Fig. 5. This is important for corrector magnets for which control is based on the beam position measurement. This kind of pre-cycle is also used for large experimental magnets.

The physical phenomena are even more complex for superconducting magnets. The classical magnetic hysteresis is also present in this case but, in addition, two other phenomena play an important role in magnetic field control. These phenomena are the decay amplitude and snapback, and they are due to the properties of superconducting cables. In this case, a special pre-cycle has to be defined for the LHC main dipoles, see Fig. 6 [4]. In the case of superconducting magnets, pre-cycle is

mandatory but is not sufficient to obtain a good control of the magnetic field. The decay and snapback phenomena are so special that a complex model of the magnetic field needs to be built to obtain a good level of prediction [5].

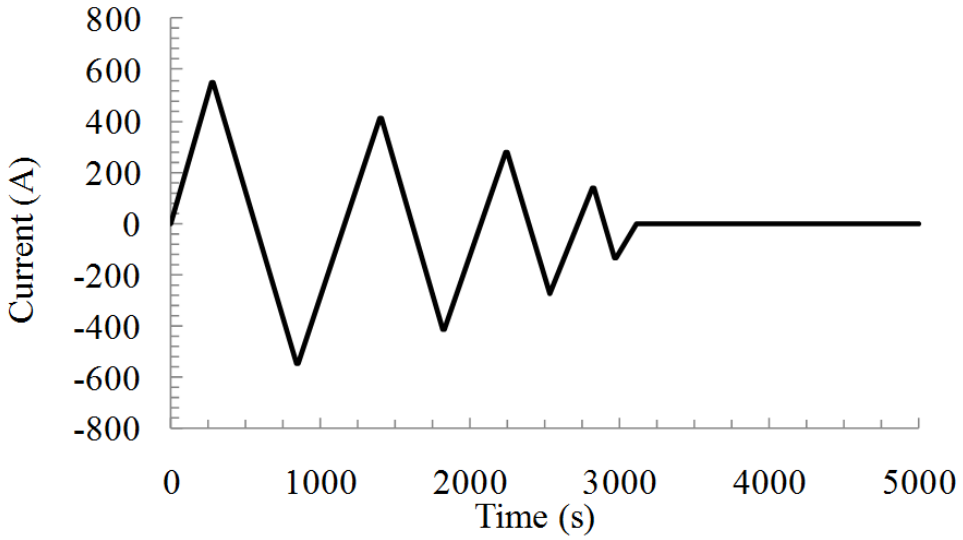


Fig. 5: Degauss cycle for corrector magnets

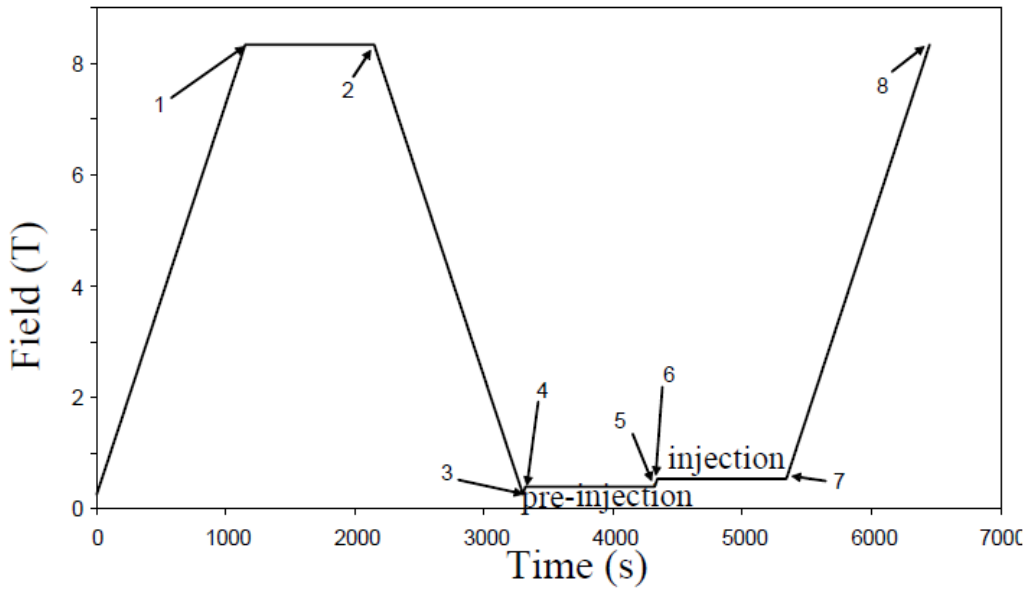


Fig. 6: LHC pre-cycle of main dipole magnets

2.3 Magnetic field model

LHC operation requires a prediction of the currents for the magnet circuits. These settings are based on a parametric model whose coefficients are obtained from a synthesis of the information available from magnetic field measurements (both room temperature and 1.9 K or 4.2 K). This set of equations, together with the coefficients estimated from measurements, are integrated in a tool at CERN called the Field Description for the LHC (or FiDeL). The aim is to provide the integral transfer function (integral magnetic field versus current) in a form suitable for inversion (current versus integral magnetic field) for each circuit in the LHC [6]. In addition, for the main ring magnets FiDeL provides a prediction of the field errors to be used to set the corrector circuits. FiDeL is implemented in the LHC control system to steer the beam, see Fig. 7. A lot of measurement needs to be done to set up

such a tool, but this type of tool is mandatory for the operation of complex and large particle accelerators.

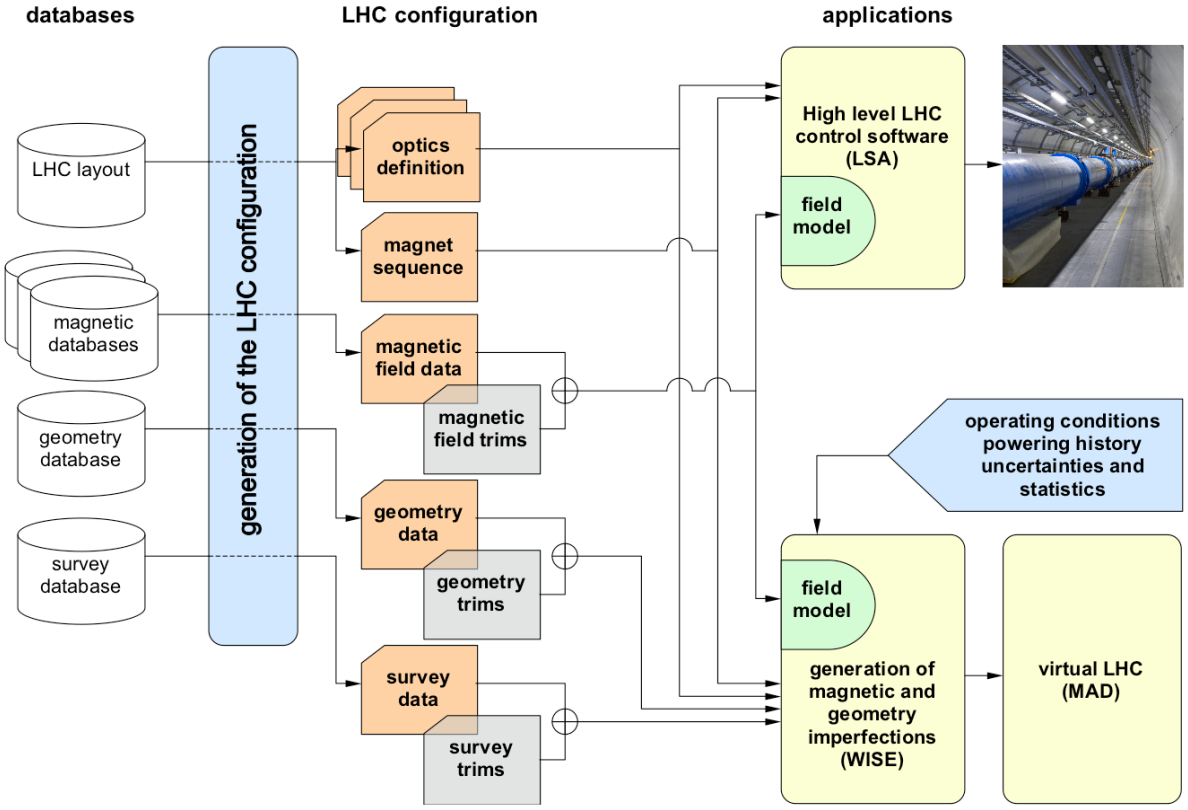


Fig. 7: LHC control architecture including FiDeL

The modelling of warm magnets with the same quality of prediction is ongoing at CERN, and it will help the setting up of smaller machines [7].

2.4 Magnetic field control

Most of the particle accelerators are current controlled. This is due to the difficulty of measuring in real time the magnetic field of the magnet with the correct level of accuracy. However, since the 1970s this idea has been considered and an additional reference magnet has been added in series with the dipole outside the machine for magnetic transducer instrumentation. This has been the case at CERN for the PS, PSB, and SPS machines. Magnetic field monitoring measurements were made to help with diagnostics during operation.

The PS B-train system is based upon a set of search coils that allow the measurement of the instantaneous field from the coil output voltage. The initial value is provided by a field marker that outputs a trigger pulse when the field reaches a preset level during the pre-injection ramp, thus signalling the start of the integration, see Fig. 8 [8]. In 2008 and for the first time, the PS accelerator was controlled in magnetic field. The magnetic field measurement was connected to the control of the main magnet power system and the regulation was done using this measurement, see Fig. 9 [9]. The global performances are above the expectations due to the improvement of the reproducibility of the machine, which is multi-beam energy.

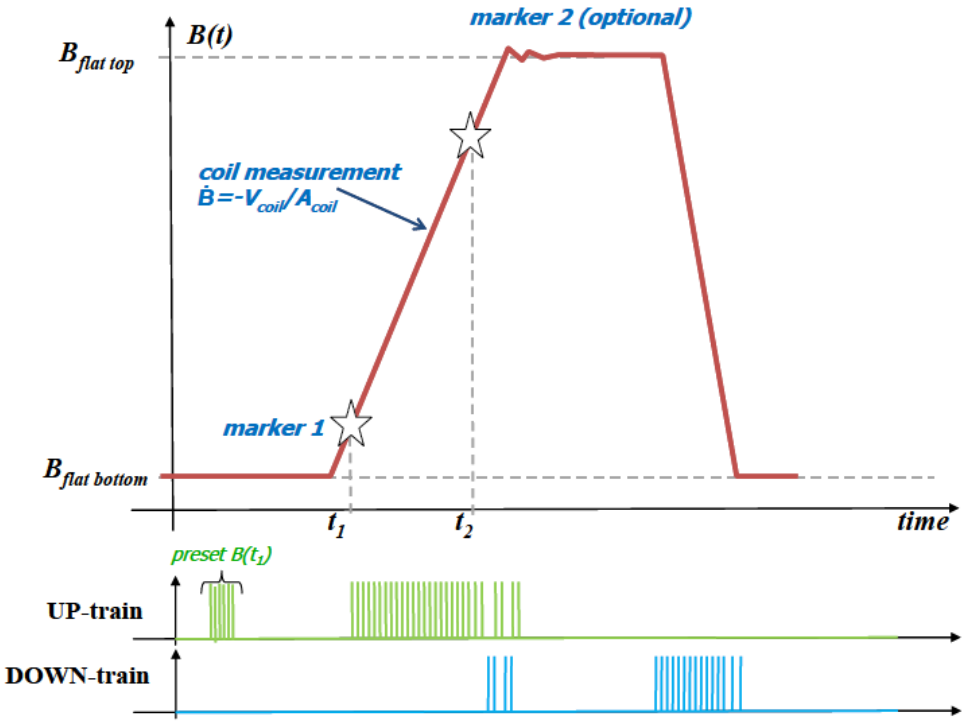


Fig. 8: Magnetic cycle with two field markers for the recovery of offset and (optionally) gain errors. A pulse on each one of the two trains represents a ±0.1 G field increment.

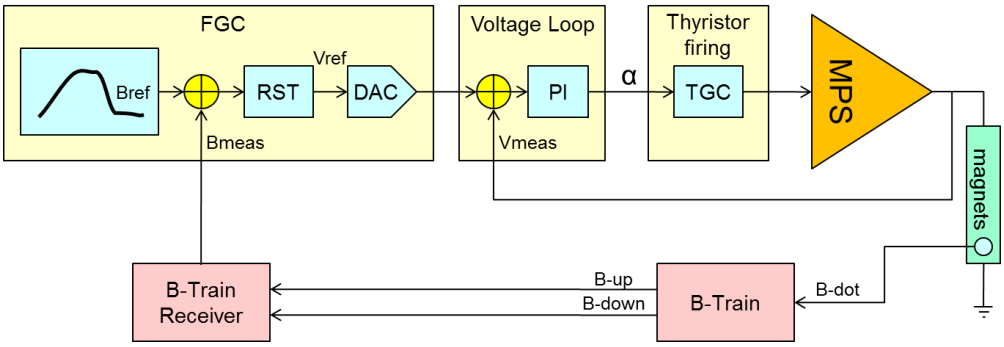


Fig. 9: B-field control principle

2.5 Orbit feedback system

In some machines, the stability of the beam is critical. It is true for synchrotron light sources such as the LHC, where the presence of two beams, both of high intensity as well as high particle energies, requires excellent control of particle losses inside a superconducting environment, provided by the LHC cleaning and machine protection system [10]. The performance and function of these systems depends critically on the stability of the beam and may eventually limit LHC performance. Environmental and accelerator-inherent sources, as well as the failure of magnets and their power converters, may perturb and reduce beam stability and may consequently lead to an increase in particle losses inside the cryogenic mass. In order to counteract these disturbances, control of the key beam parameters – orbit, tune, energy, coupling, and chromaticity – are an integral part of LHC operation. Since manual correction of these parameters may reach its limit with respect to the required precision and expected timescales, the LHC is the first proton collider that requires feedback control systems for safe and reliable machine operation. The sources of orbit and energy perturbations can be grouped into environmental sources, machine-inherent sources, and machine element failures. The slowest

perturbation due to ground motion, tides, and temperature fluctuations in the tunnel can reach 200 µm within 10 hours. These orbit perturbations exceed the required beam stability by one order of magnitude. The LHC cleaning system, imposing one of the tightest constraints on beam stability, requires a beam stability in the range of about 15−25 µm at the location of the collimator jaws. The solution implemented for the LHC is an automated orbit feedback system. It is based on the readings from 1056 beam position monitors (BPMs) that are distributed over the machine; a central global feedback controller calculates new deflection strengths for the more than 1060 orbit corrector magnets (CODs) that correct the orbit and momentum around their references, see Fig. 10. In the LHC the orbit feedback system acts mainly at a low frequency (below 50 Hz), see Fig. 11.

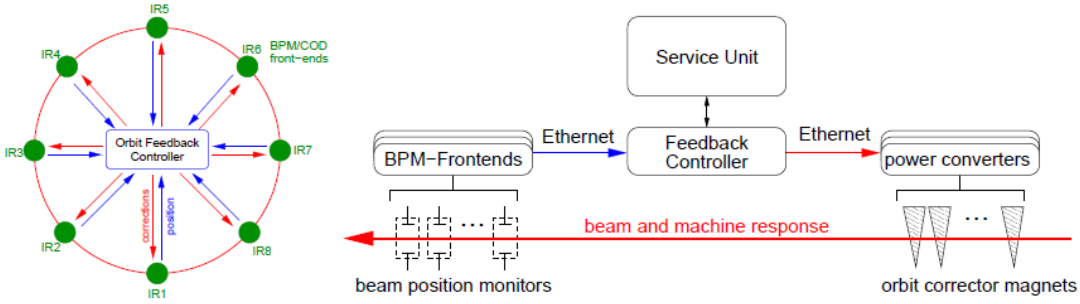


Fig. 10: Principle of the LHC orbit feedback system

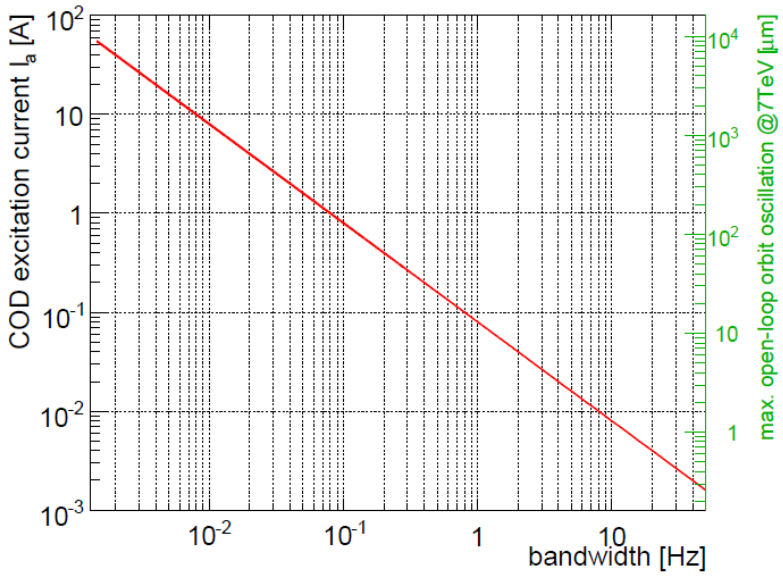


Fig. 11: Open-loop bandwidth of the ±60A converter powering the LHC COD magnets. The maximum sinusoidal current amplitude is plotted as a function of bandwidth. The corresponding maximum orbit excursion prediction in the arc driven by the MCB magnet at β = 180 m is given on the right-hand scale.

3 Power converter control

The control of particle accelerator power converters is one of the most challenging parts and requires special technology. Firstly, it requires high-precision control well above the industrial standard; secondly, all of the power converters for one machine need to be perfectly synchronized (typically with a maximum of 100 µs jitter). However, no standard controls are available on the market to control power converters. For slow applications, many bus protocols may be used (RS422, Ethernet, etc.). For applications that require synchronization, different options could be selected but,

unfortunately, no industrial standard control fulfils the requirement of particle accelerators. CERN developed its own controller, called a function generator and controller (FGC), which is a dedicated controller embedded in every power converter [11]. This controller is responsible for function generation (current versus time), current regulation, and power converter state monitoring and control. All of the FGCs are connected to a gateway through a fieldbus, which can be WORLDFIP or Ethernet for the latest generation of FGC. This is needed to link the IP technical network of the machine with the fieldbus segments. Each gateway includes a timing receiver interface, connected to the general machine timing network. This provides the gateways with accurate date/time and millisecond-level machine events. It also generates precise timing pulses to synchronize the WorldFIP interface or to send synchronization timing to the embedded electronics. Each gateway drives a single segment with a maximum of 64 FGCs, see Fig. 12.

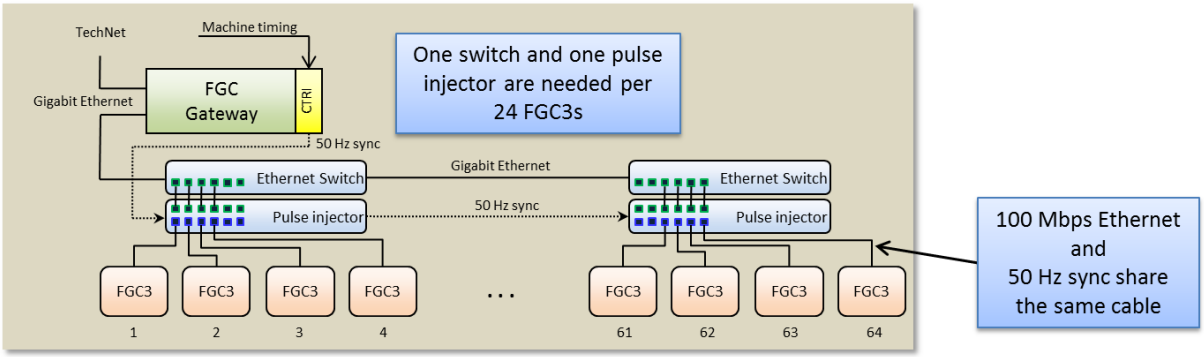


Fig. 12: Power converter control architecture at CERN

A key task for each FGC is current regulation. The power part is controlled as a voltage source and the current regulation is done by the FGC. For the LHC, many circuits have very large time constants (many hours) and yet require a very high accuracy, and this can only be achieved with digital regulation. This was the main reason to include a second processor in the design. It operates as a coprocessor for the main microcontroller, performing the real-time tasks of function generation, digital filtering, and current regulation. Thanks to this standardized embedded controller, the software running in all FGCs is the same; only the parameters of the circuits need to be set. The current control algorithm is based on a RST controller, see Fig. 13 [12].

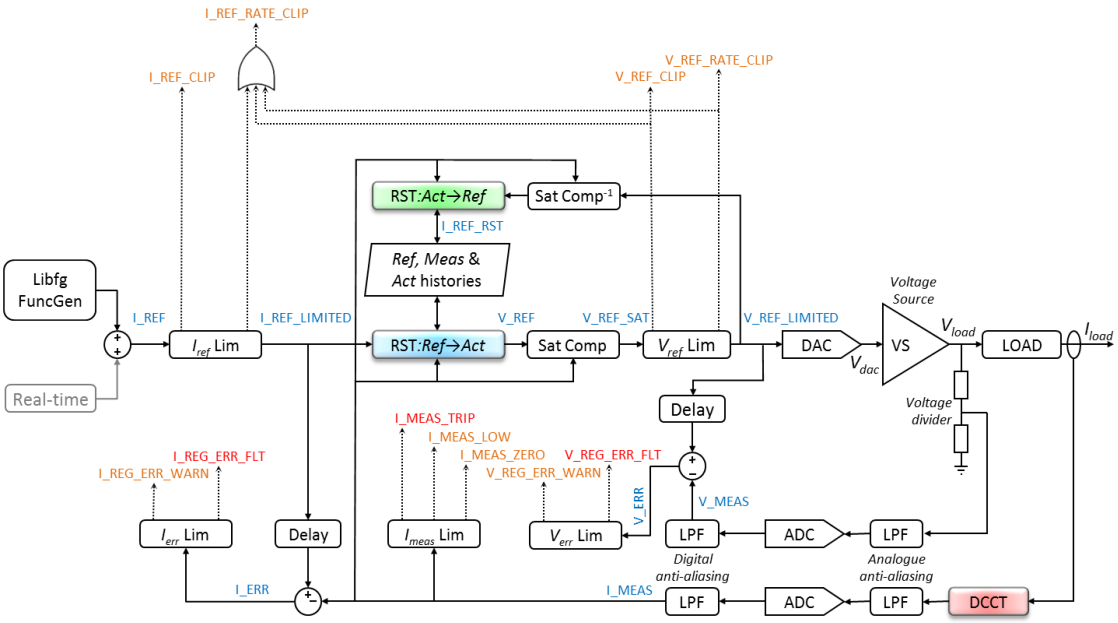


Fig. 13: FGC current control architecture

4 Control of nested circuits

The control of nested circuits can be challenging. It is particularly true when a change in the current from one power converter generates a perturbation seen by another. In this case, the two power converters are coupled by the load and a special control system has to be designed to stabilize the system. This is the case for the LHC inner triplet magnets, which need three power converters to power four magnets. The control strategy that has been developed is based on a decoupling loop by state feedback control and with three outer independent RST digital current loops, see Fig. 14 [13].

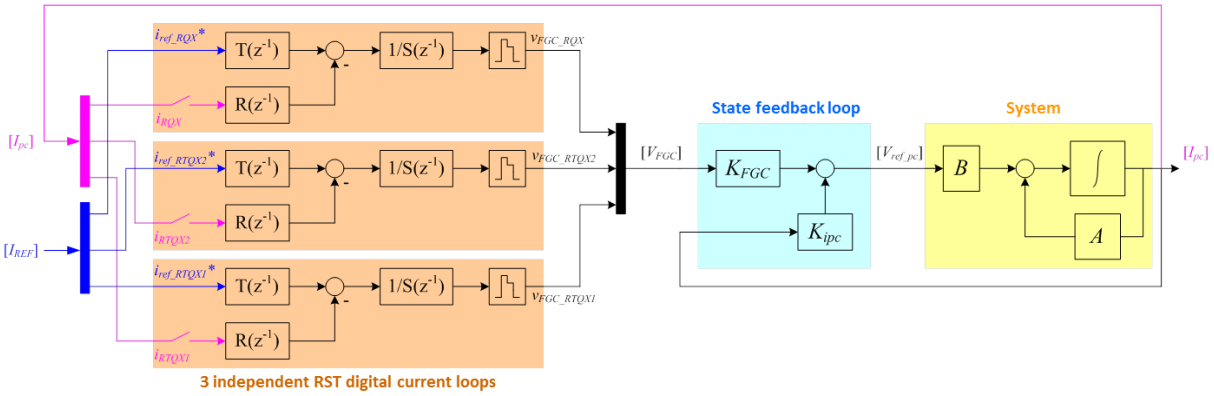


Fig. 14: Control strategy for nested circuits

Thank to this control strategy, each power converters can be controlled independently without affecting the stability of the others. The current stability of each power converter stays in the same range as for a single circuit. This decoupling technique eases the operation of nested circuits and it suppresses the need forexpertise while operating such a system.

5 Energy saving

Energy consumption is a major concern when operating particle accelerators. Magnets are the main consumer and they must be designed to limit their running costs. At the level of power converters, the efficiency is the main criteria to measure the performance of energy conversion. At the level of the machine, the method of powering the magnets has a huge impact on energy consumption. CERN has developed a new concept to save energy, which is described below.

5.1 Pulsing magnets

One of the easiest ways to save energy is to power magnets only when the beam is present inside. This isn't always the case as the easiest way to power a magnet is to keep the current constant all of the time. Moreover, a magnet with a solid yoke can only be powered with a constant current. This solution was widespread as this type of magnet is cheaper than those that are laminated. A classic sight in old facilities are magnets with solid yokes for experimental areas or transfer lines. In these cases, the energy consumption is very high when compared to the real requirement. Energy saving can be evaluated using the ratio of the period of the beam to the repetition time of the beam, see Fig. 15.

A study was done at CERN with the EAST area, where it was demonstrated that electricity consumption could be reduced by 95% by pulsing the magnets [14]. In this case, the beam flat top duration is up to 500 ms and the repetition rate is a few cycles per minute. The power converter types are classical AC/DC converters with enough DC voltage to ramp up the current before the beam's arrival. The return of energy also has to be considered carefully, depending upon the power converter technology.

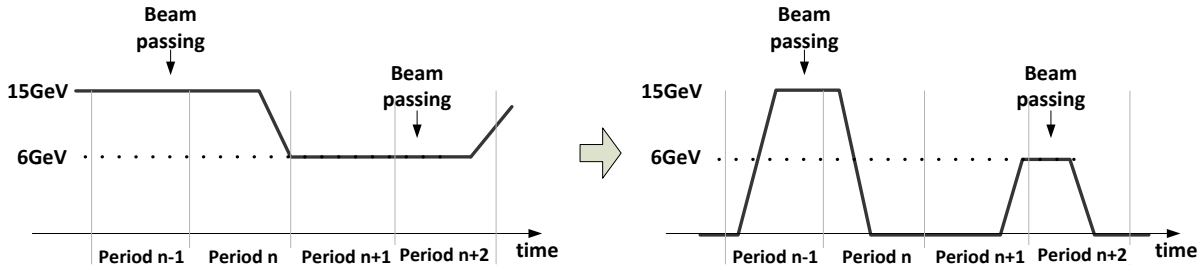


Fig. 15: DC operation and pulsed operation

5.2 Fast pulsed converters

In the case of linacs, the beam presence in the magnets is in the order of a few milliseconds with a repetition frequency of a few hertz. For example, the beam pulse length is 1.2 ms for Linac4 at CERN with a repetition time of 1.2 s. The beam presence duty cycle is then less than 1%, which leads to an over-consumption if the magnets are powered in DC. A new type of converter was developed at CERN to provide fast trapezoidal current pulses using a high-power insulated-gate bipolar transistor (IGBT) module in its resistive region to regulate the magnet current, see Fig. 16 [15]. Thanks to the pulsed operation, the power converters can be much smaller, and the electricity consumption and cooling capacity requirements are reduced drastically.

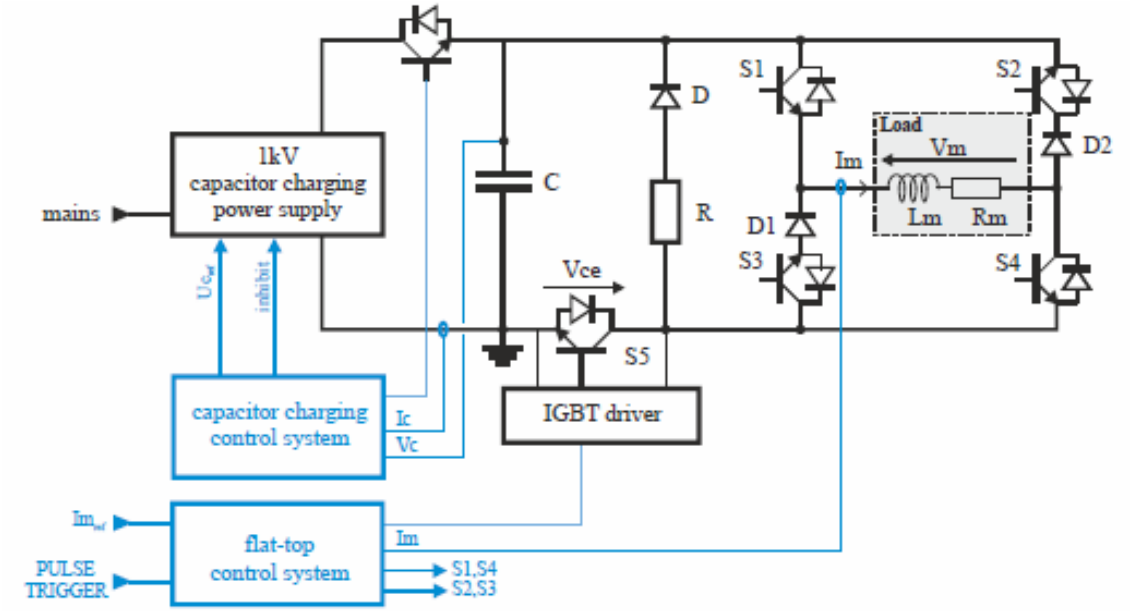


Fig. 16: Fast pulsed converter topology

5.3 Energy management

Particle accelerators are often characterized by a strong and modulated power demand, which is sometimes incompatible with the power available from the grid. Therefore, large facilities for short-term energy storage have been used, traditionally based on rotating machines. A new concept was introduced at CERN to reduce the power taken from the grid and to limit it to a strict minimum, see Fig. 17. The idea is to store locally energy and to exchange it with the magnets during each cycle [16]. Only the magnets' losses are taken from the grid. Peak power is provided from local energy storage. As particle accelerators are doing thousands of cycles per year, the only possible solution to store energy is within capacitors. Only capacitors can execute millions of charge cycles [17]. The latest optimization was to reduce the power taken from the grid to below the maximum dissipated power in the magnets by anticipating the power demand in each cycle, see Fig. 18.

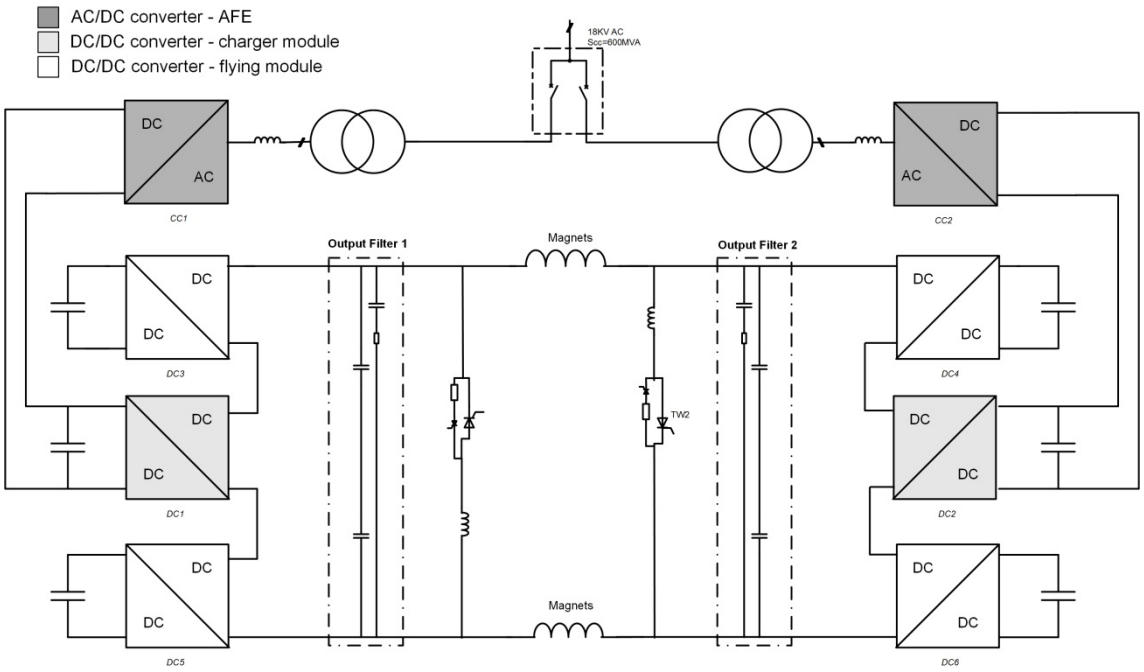


Fig. 17: Power converter topology with capacitor energy storage

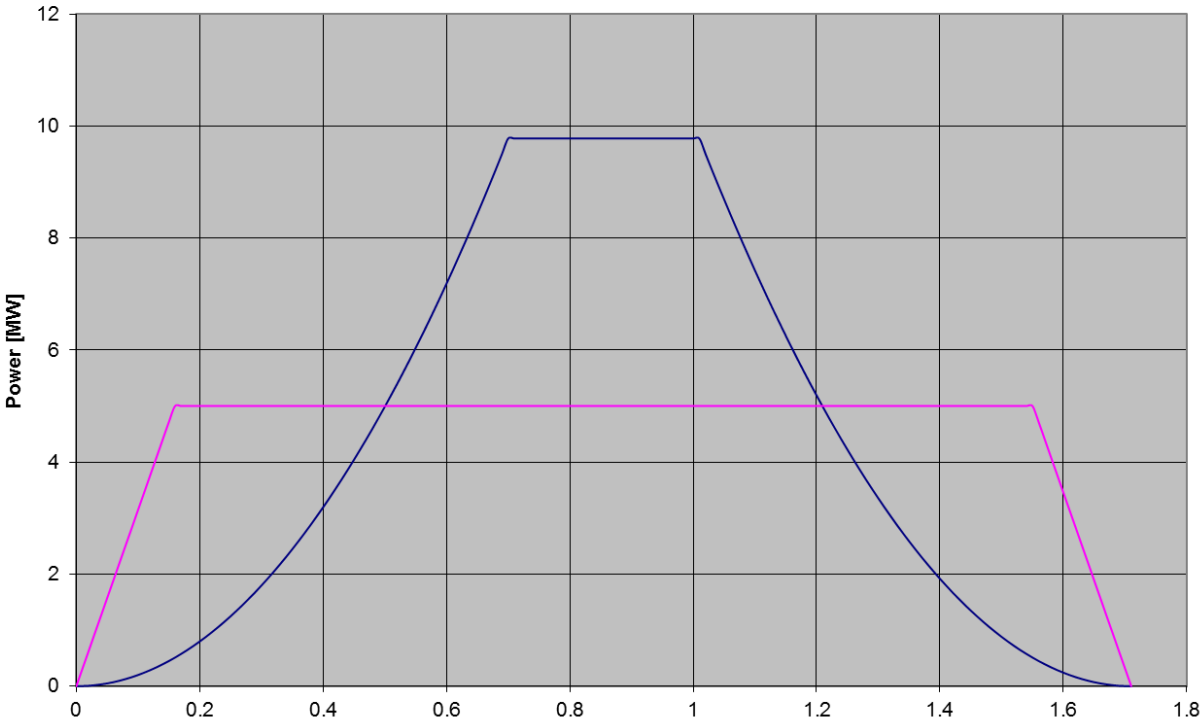


Fig. 18: Optimization of power taken from the grid. Blue is the resistive losses of the magnets during a cycle; magenta is the power taken from the grid.

This new concept was introduced at CERN with the power system of the PS accelerator (POPS). It has been in operation since 2011, and has demonstrated its feasibility. However, the stress on the capacitors that are used for energy storage needs to be considered carefully. The discharge cycles, even without any reverse voltage, can degrade the film metallization due to partial discharges. These phenomena need to be taken into account when sizing the capacitor banks [18].

6 Summary

This paper presents the latest trends for particle accelerator powering regarding magnetic field uncertainty, power converter control, and energy-saving. These parameters need to be taken into account at the very beginning of any project as they have a major impact on the cost and performance of a machine. They require a system-level approach before the design of power converters, and this can lead to new power converter concepts, like that presented in this paper for saving energy.

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