6 Impact of radiation on electronics and opto-electronics

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In this chapter we will present the results of the impact of radiation on electronics and opto-electronics for two of the LHC experiments during Run 1 and Run 2. ATLAS results are presented in Section 6.1; CMS in Section 6.2. In Section 6.3 we will present a comparison between the two experiments, highlighting operational guidelines and proposing solutions to build the electronics and opto-electronics of the future LHC experiments.

6.1 ATLAS

Radiation effects from TID on the IBL front-end electronics will be described in Section 6.1.1; SEU/SET effects from highly ionizing particles in IBL and SCT detectors will be shown in Section 6.1.2 whilst impact on opto-electronics from SCT will be described in Section 6.1.3. Finally, results from TRT electronics will be presented in Section 6.1.4.

6.1.1 TID effects in the IBL front-end chip

The IBL consists of 14 carbon fibre staves instrumented along 64 cm, 2 cm wide, and tilted in ϕ by 14° surrounding the beam pipe at a mean radius of 33 mm from the beam axis and providing a pseudo-rapidity coverage of ± 3. Each stave, with integrated CO_2 cooling, is equipped with 32 front-end chips bump bonded to silicon sensors. The IBL detector was designed to be operational until the end of the LHC Run 3, where the total integrated luminosity was expected to reach 300 fb^{-1}. The detector components are qualified to work up to 250 Mrad of TID.

This chapter should be cited as: Impact of radiation on electronics and opto-electronics, Eds. M. Bindi, E. Butz, DOI: 10.23731/CYRM-2021-001.87, in: Radiation effects in the LHC experiments: Impact on detector performance and operation, Ed. I. Dawson,
CERN Yellow Reports: Monographs, CERN-2021-001, DOI: 10.23731/CYRM-2021-001, p. 87.

The IBL front-end chip, namely FE-I4B [1], was designed in 130 nm CMOS technology which features an array of 80×336 pixels with a pixel size of $50 \times 250\,\mu m^2$. Each pixel contains an independent, free running amplification stage with adjustable shaping, followed by a discriminator with independently adjustable threshold. The FE-I4B keeps track of the time-over-threshold (ToT) of each discriminator with 4-bit resolution, in counts of an external supplied clock of 40 MHz frequency. The FE-I4B operates by feeding the common power supply to analogue signal amplifiers and digital signal-process circuits, referred to as the low-voltage (LV) power supply and the clock input.

6.1.1.1 Observations during 2015 data taking

During the first year of the IBL operation in 2015, a significant increase of the LV current of the front-end chip and a detuning of its parameters (threshold and time-over-threshold) have been observed in relation to the received TID.

The average LV current of the IBL module groups (serving four FE-I4B chips) during data taking was stable at a value of 1.6–1.7 A until the middle of September 2015. Then, the current started to rise up significantly (see Fig. 71), and the change of the current during the period September–November 2015 was even more than 0.2 A within a single LHC fill, depending on the luminosity and duration of the fill. Due to safety concerns, after $\sim 2\,fb^{-1}$ of integrated luminosity corresponding to ~ 580 krad of TID, the IBL was switched off in early October 2015. The detector was kept off during two LHC fills for a total of $\sim 240\,pb^{-1}$ of integrated luminosity, corresponding to ~ 70 krad irradiation from the LHC beam. A complete return to the baseline of the LV currents was observed when the detector was powered up again. However, as soon as the LHC beam irradiation restarted with the detector being powered, the raising behaviour of the LV current appeared again with similar characteristics.

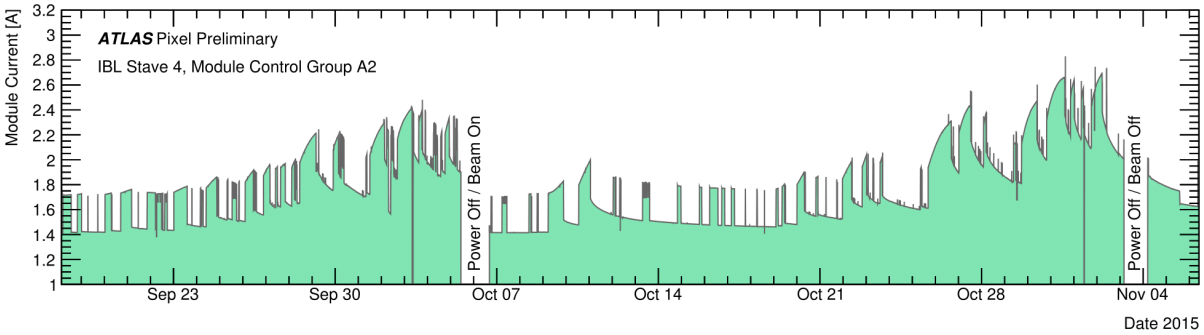


Fig. 71: LV current drift of an IBL module group (serving four FE-I4B chips) during 2015 data taking. There are two levels of the current depending on the front-end configuration: STANDBY (lower level, with pre-amplifiers off) and READY (higher level, with pre-amplifiers on). There are two long power-off periods on October 5–6 (with the LHC beam ON) and November 3–4 (during a LHC technical stop).

With the increase of the LV current, the temperature of IBL modules also changes (see Fig. 72). In addition, as shown for example in Fig. 73, the calibration of the FE-I4B chips for the analogue discriminator threshold and the target ToT drifted rapidly despite a frequent update of the calibration.

The increase of the LV current of the FE-I4B chip and the drifting of its tuning parameters were traced back to the generation of a leakage current in NMOS transistors induced by radiation. The radiation induces positive charges that are quickly trapped into the shallow-trench-isolation (STI) oxide at the edge of the transistor. Their accumulation builds up an electric field sufficient to open a source-drain channel where the leakage current flows. If the accumulation of positive charges is relatively fast, the formation of interface states is a slower process. The negative charges trapped into interface states start to compete with the oxide-trapped charges with a delay. This is what gives origin to the TID effect at low dose [3] which is discussed in more detail in Section 2.2.1.

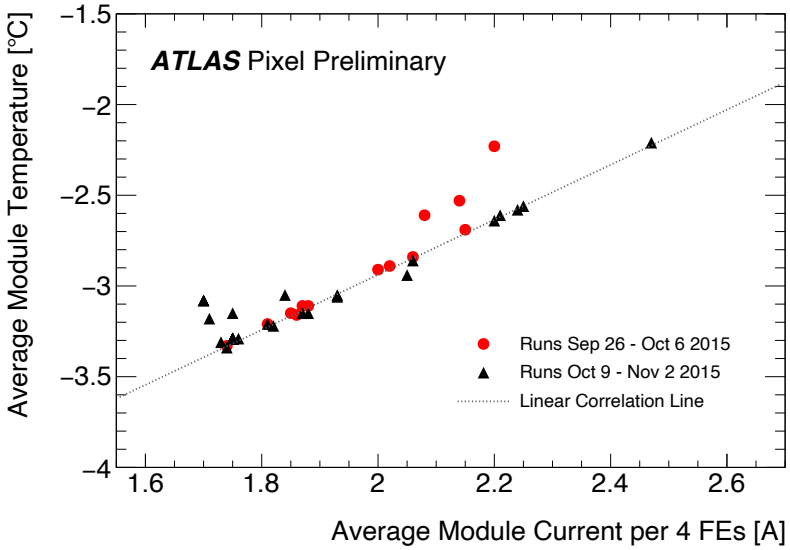


Fig. 72: Performance of the IBL modules during high luminosity proton–proton collision runs from September to November 2015, separated into the periods before (red circles) and after (black triangles) the long power-off on October 6. The average IBL module current (4 FE-I4B) is displayed against the average module temperature [2] and compared to a linear dependence.

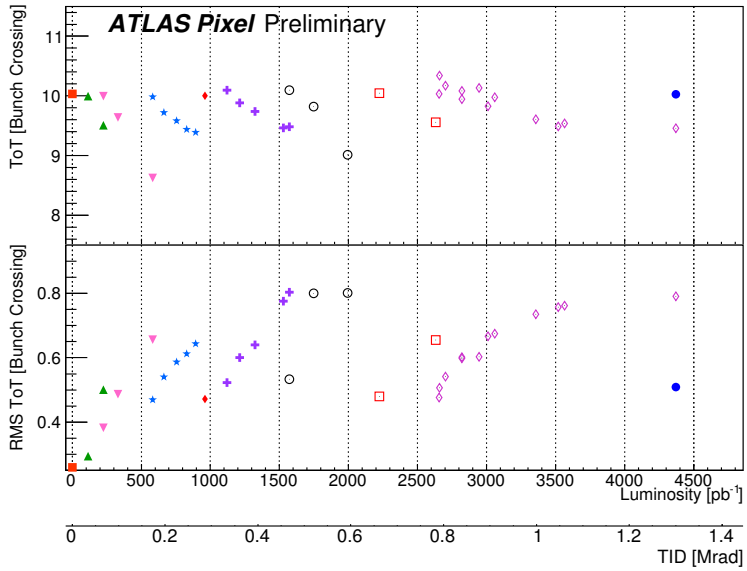


Fig. 73: The time-over-threshold (ToT) and its RMS as a function of the integrated luminosity or TID [2]. The detector was regularly retuned, and each marker type corresponds to a single tuning of the detector.

6.1.1.2 Irradiation test results

Dedicated laboratory measurements [4] of irradiated single transistors in 130 nm CMOS commercial technologies showed that the increase of the leakage current reaches its peak value between 1 Mrad and 3 Mrad. For higher TID the current decreases to a value close to the pre-irradiated one.

To reproduce and analyse the effects described above during the IBL operation, several irradiations and electrical tests were performed [2]. Since the current increase in NMOS transistors depends on dose rate and temperature, measurements under different temperature and dose rate conditions have been

carried out to qualify this dependency.

The first irradiation test aimed at measuring the boundary current (at a given temperature and dose rate) that the chip always approaches after annealing periods and re-irradiation. Figure 74 shows the increase of the current consumption of a single FE-I4B chip in data taking condition as a function of the TID. The temperature of the chip was 38 °C and the dose rate 120 krad h^{-1}. After reaching the maximum of each peak the chip was annealed for several hours resulting in the observed partial recovery.

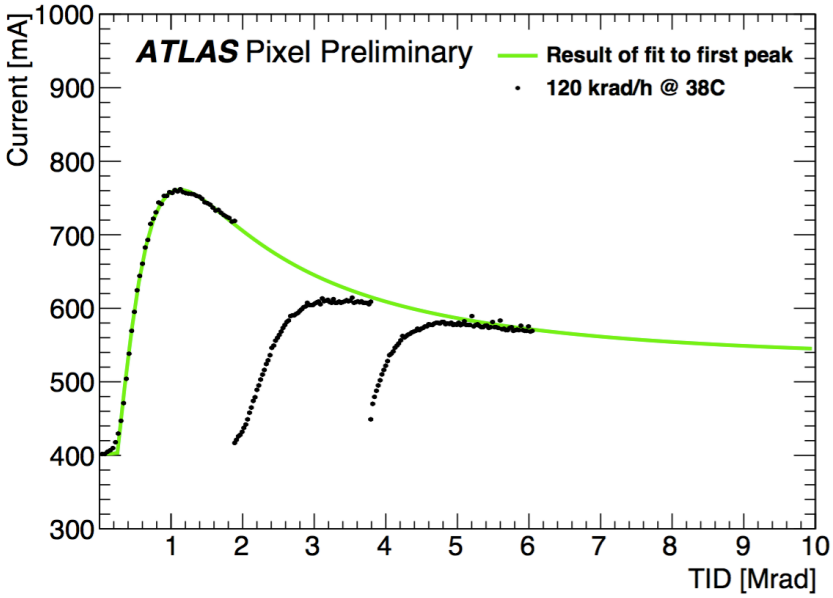


Fig. 74: Current consumption of a single FE-I4B chip in data taking condition as a function of the TID. The temperature of the chip was 38 °C and the dose rate 120 krad h^{-1}. After reaching the maximum of each peak the chip was annealed several hours resulting in the observed partial recovery [2]. The fit performed on the first set of data (first peak) has been carried out by using the current parametrization described in Ref. [5].

In order to study the dependence of the LV current increase on temperature and dose rate several irradiation tests were performed by setting one of those variables and changing the other. Figure 75 shows the results of three different measurements, performed with three different and previously not irradiated chips. The dose rate was 120 krad h^{-1} and the temperatures were 38 °C, 15 °C, and −15 °C. Before irradiation, the LV current of the three chips was 400 mA (38 °C), 360 mA (15 °C), and 380 mA (−15 °C). For comparison, Fig. 76 shows the result of two different measurements where the temperature was kept fix at 15 °C, while the dose rate set to 120 krad h^{-1} or 420 krad h^{-1}. Also in this case the tests were performed with different and previously not irradiated chips. The measurements described above revealed two facts:

- at a given dose rate the LV current increase is stronger at lower temperatures;
- at a given temperature, the LV current increase is stronger at higher dose rates.

To simulate the dose rate conditions of the 2015 and 2016 data taking, a first irradiation was performed at −15 °C and 120 krad h^{-1}. This was followed by several hours of annealing and a second irradiation this time performed at 5 °C and 420 krad h^{-1}. As shown in Fig. 77, the second LV current peak is lower than the first one, i.e., by increasing the operational temperature of the chip it was possible to keep the increase of the LV current below the boundary current given by the first irradiation. To verify that a temperature of 5 °C was safe for the IBL detector operation, a measurement at 10 krad h^{-1} was performed. The maximum LV current increase was of the order of 250 mA, which gives a LV current

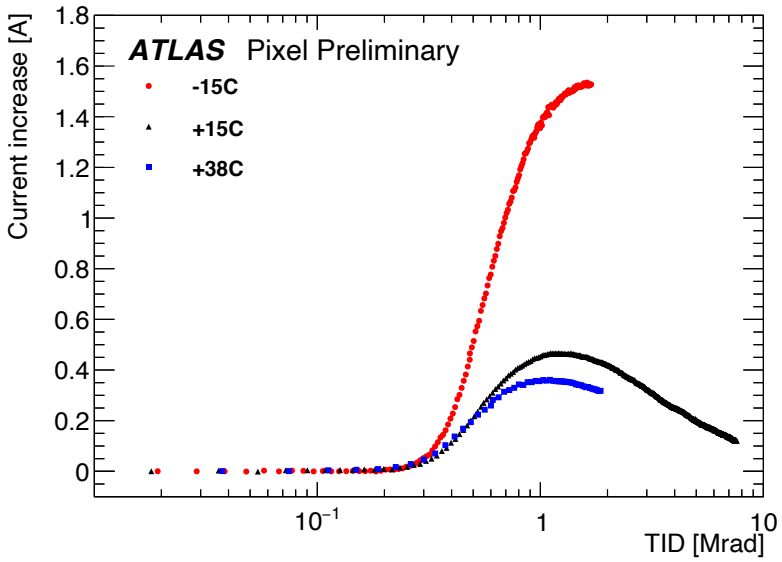


Fig. 75: Increase of the LV current of three single FE-I4B chips in data taking condition as a function of the TID (x-axis in log scale). Test measurements were carried out at 38 °C (blue), at 15 °C (black), and at −15 °C (red) with a dose rate of 120 krad h^{-1}. A dose rate up to 10 krad h^{-1} is expected in the experiment. The LV current of the single FE-I4B chips before irradiation were 400 mA (38 °C), 360 mA (15 °C), and 380 mA (−15 °C) [2].

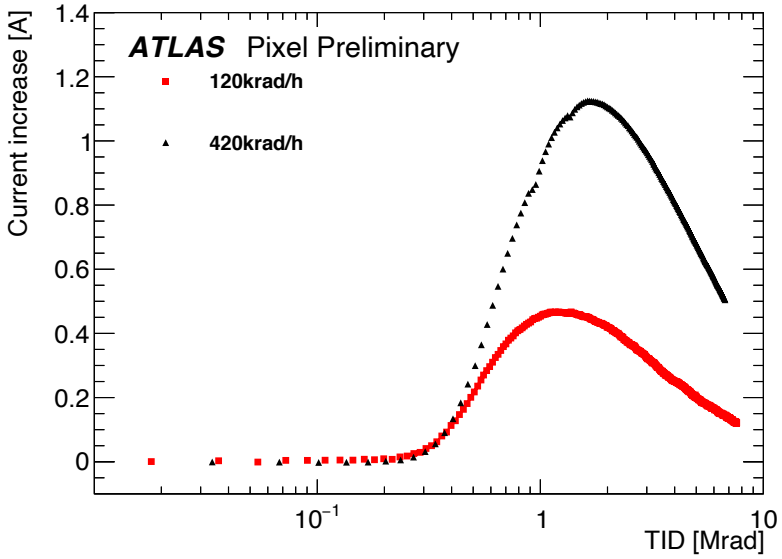


Fig. 76: Increase of the LV current of two FE-I4B chips in data taking as a function of the TID (x-axis in log scale). Test measurements were carried out at 15 °C with a dose rate of 120 krad h^{-1} (red), and 420 krad h^{-1} (black). A dose rate up to 10 krad h^{-1} is expected in the experiment. The LV current of the single FE-I4B chips before irradiation were 380 mA (420 krad h^{-1}) and 360 mA (120 krad h^{-1}) [2].

increase of 1 A for a four-chip unit; this would not exceed the safety limit of the LV current originally set to 2.8 A. In principle, lower operational temperatures are favourable for the sensor performance and properties after irradiation and therefore preferred. Consequently, irradiation and electrical tests were

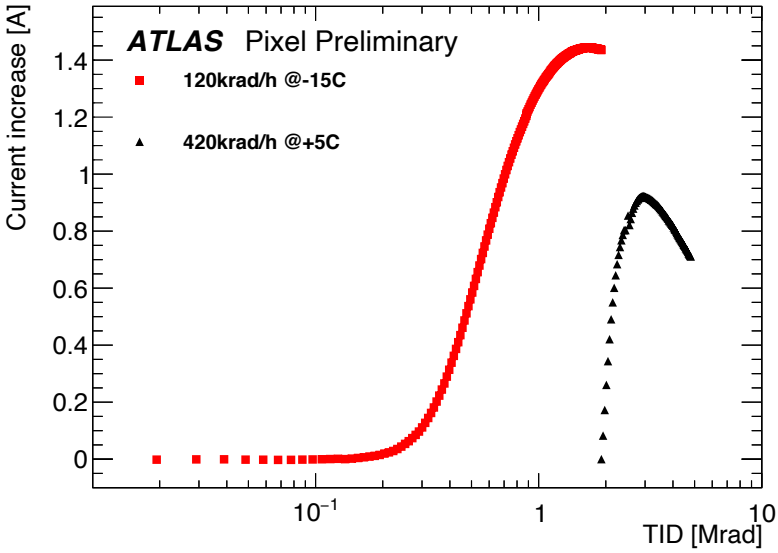


Fig. 77: Increase of the LV current of a single FE-I4B chip in data taking condition as a function of the TID (x-axis in log scale) during two consecutive irradiation campaigns in a lab measurement. Between the two irradiations several hours of annealing period at room temperature was performed, and resulted in the observed recovery. The TID of both irradiations is summed up. The LV current of a single FE-I4B chip before irradiation was 380 mA (first step) and 550 mA (second step) [2].

also performed at a temperature of 0 °C to investigate the feasibility for a colder operation. In addition it was investigated the evolution of the maximum of the LV current peak under several irradiation steps followed, interleaved with periods of annealing. In this case the first two consecutive peaks of the LV current increase exceeded the maximum current allowed for a safe detector operation. Therefore, it was decided to set 5 °C as minimum temperature for a safe and successful data taking.

Another effect was confirmed during the irradiation campaign of one FE-I4B chip with 16 MeV protons at room temperature (see Fig. 78). The chip was left without powering for 30 minutes in the beam, integrating a 2 Mrad dose (on top of the 9.2 Mrad of dose previously collected). As a result, the chip was completely annealed; this behaviour confirmed the observations with the IBL detector at LHC, with the return to baseline of the LV current consumption. The LHC data were taken with a module $T \sim -7$ °C on the 6 October 2015 (see Fig. 71). To be noticed that a similar effect was also observed during X-ray irradiation of CMS DC-DC converters (see Section 6.2).

6.1.1.3 Detector operation guidelines

Based on the observations during the first year of data taking in 2015 with the IBL detector, it was decided to raise the safety limit for the IBL LV currents from 2.8 A to 3 A for module groups of four chips, which means a maximum current consumption of 750 mA per chip. Since the average current consumption for a single FE-I4B chip is about 400 mA before irradiation, the increase of the current due to the TID effects cannot be higher than 350 mA per chip. Given the above results it was decided to increase the IBL operation temperature from −10 °C to 15 °C. In addition, the digital supply voltage (V_D) was lowered from 1.2 V to 1 V to decrease the LV current.
Thanks to dedicated measurements at 5 °C and at a dose rate comparable to the LHC in 2016 (10 krad h^{-1}), it is proven that the current increase is of the order of 250 mA. With this a module group of four chips does not exceed the safety limit of 3 A. Therefore operating the IBL at 5 °C is safe with respect to the expected luminosity in 2016. The temperature of the IBL cooling system was

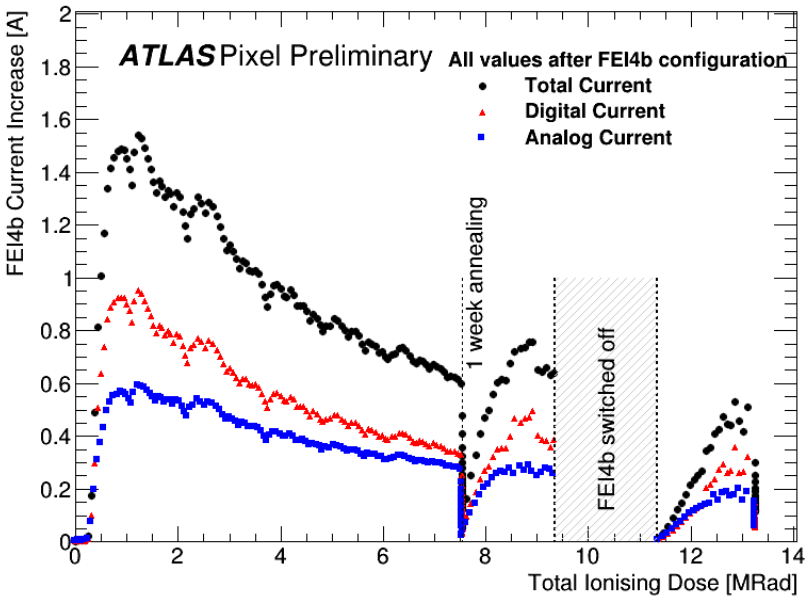


Fig. 78: LV current in a single FE-I4B chip during proton irradiation as a function of the TID delivered. The LV current is shown for the analogue and digital part of the FE-I4B chip, the sum of the two is also reported (total current). The LV current was monitored both during the irradiation and for about an hour afterward, showing an annealing effect. The FE-I4B chip was at room temperature and the dose rate was 3 Mrad·h^{-1} for the first irradiation and 4 Mrad·h^{-1} for the following campaign. The measurement was made in two steps, separated by one week in which the chip was not powered and left at room temperature. During the second irradiation, the chip was switched off for half an hour while the irradiation continued. In this measurement, the chip was irradiated with a 18 MeV proton beam [6].

lowered to a set point of 5 °C. The digital supply voltage (V_D) was raised from 1 V to 1.2 V, after an accumulated dose of $\sim$4.3 Mrad which, as the measurements show, is well beyond the high peak region for the current consumption. An overview of the mean LV current of the IBL FE-I4B chips as a function of integrated luminosity and TID during stable beam is shown in Fig. 79.

The LV currents are averaged for all modules across 100 luminosity blocks ($\sim$ 100 minutes), and the changes in digital supply voltage (V_D) and the temperature (T_{Set}) are highlighted. In addition, since the shift of the tuning parameters can be seen even at low dose rates and warmer temperatures, a re-tuning on a regular basis was performed.

6.1.1.4 Observations collected at the end of Run 2

During the late years of Run 2 (2016–2018), the LHC instantaneous and integrated luminosity grow considerably respect to the previous years. The effect of the detector occupancy on the IBL LV currents became visible.

Figure 80 shows the average IBL LV current at the start of each stable beam period, whenever the FE-I4B pre-amplifiers were turned ON, for the entire Run 2 period. A clear correlation of the current consumption with the LHC peak luminosity was observed. This correlation became $\sim$ 100% for the difference between IBL LV currents at the start of each LHC fill (I_{start}) and right before the fill, with amplifiers OFF (I_{ampoff}), for 2017–2018 data (see Fig. 81). In this figure the TID effects are very small and the current difference is dominated by the chip digital activity proportional to the LHC peak luminosity.

Figure 82 shows the IBL LV current consumption during the inter-fill periods, when no beams were present in the machine and the FE-I4B pre-amplifiers were off. In this case, the only contribution comes from the integrated TID effect; such contribution became less and less effective, showing a sort

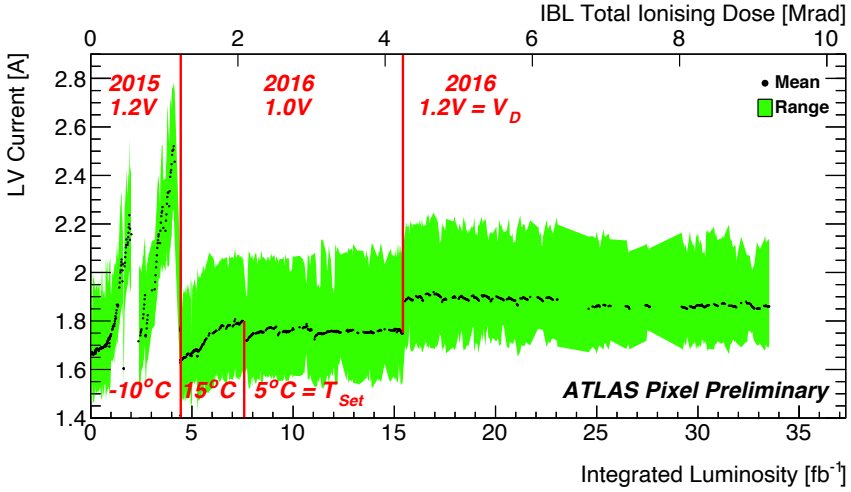


Fig. 79: Mean IBL LV current during stable beam against integrated luminosity and TID. Changes in digital voltage (V_D) are highlighted. The set temperatures (T_{Set}) of the modules correspond to actual module temperatures of about $-5\,°C$, $20\,°C$, and $10\,°C$. There were significant increases in LV current during 2015; this was addressed in 2016 by increasing the module temperatures and decreasing the digital voltage. The digital voltages were later increased back to decrease readout error frequency.

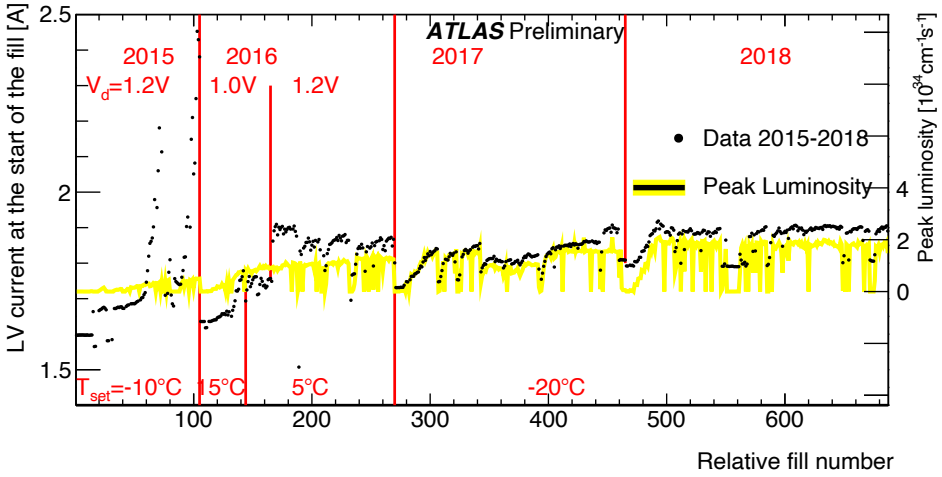


Fig. 80: Mean IBL LV current at the start of each stable beam fill (pre-amplifiers turned on)

of saturation on the LV currents in 2018 respect to the previous years.

Figure 83 shows the average IBL LV current consumption for FE-I4B chips with planar sensors that shares the same z coordinates. In total there are 56 FE-I4Bs per each z location. Higher current is present in the central part of the detector whilst a smaller impact is visible in the forward region. This increase of the current in the central z region is the sum of the TID effects and occupancy effects. The shape of the distribution is present during the entire Run 2 period.

6.1.1.5 Summary

During the first year of data taking in 2015, a peculiar increase of the LV current of the FE-I4B chip and the detuning of its parameters (threshold and time-over-threshold) was observed in relation to the received total ionizing dose. It was tracked back to the generation of a leakage current in NMOS transistors induced by radiation. Dedicated irradiation and electrical tests of FE-I4B chips showed that the leakage

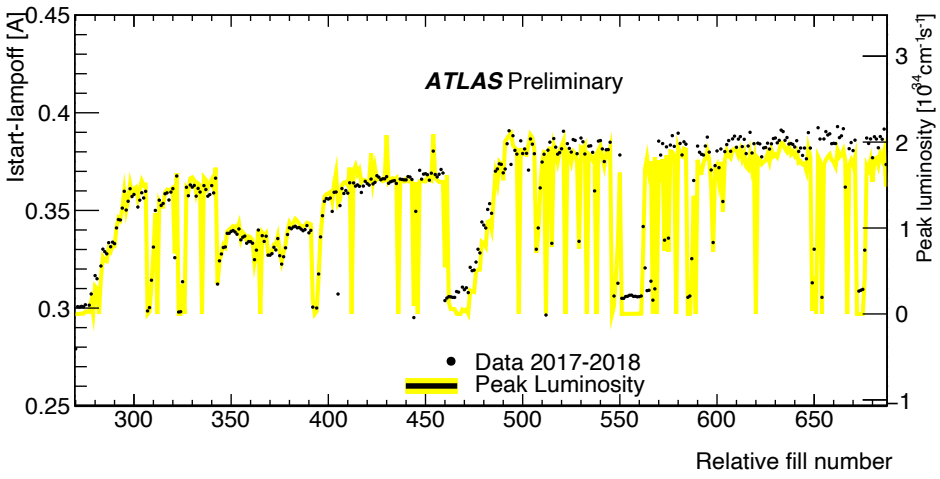


Fig. 81: Mean IBL LV current at the start of each stable beam fill (I_{start}) (pre-amplifiers turned on) subtracted of the mean current right before the fill injection (I_{ampoff}) (pre-amplifiers turned off).

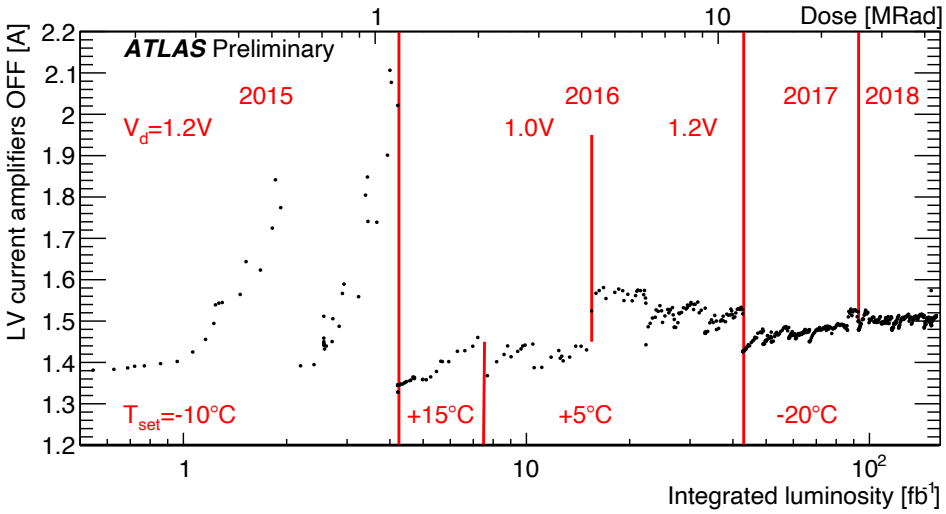


Fig. 82: Mean IBL LV current during the Run 2 inter-fill periods (pre-amplifiers turned off)

current reaches its peak value when the total ionizing dose is in the range of 1–3 Mrad, and above this the current decreases to a value close to the pre-irradiation one. This effect was shown to be temperature and dose rate dependent. Due to safety concerns, the IBL was temporarily powered off in October 2015 (during two LHC fills). A complete annealing of the LV currents was observed; this effect was confirmed in a dedicated test during the proton irradiation campaign. Thanks to the intensive irradiation studies it was possible to propose special detector settings (temperature and digital supply voltage) that could guarantee a successful data-taking in the following months.

With the increase of the integrated luminosity/dose at the end of Run 2 operation, a clear saturation of the LV current was observed. Furthermore, a minimal contribution of the LV current from the detector occupancy was also visible during the high luminosity fills (peak lumi $> 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$) in the years 2017–2018. A clear z dependence on the IBL LV currents was observed during Run 2, similar to the data obtained from sensor leakage current measurements and simulation presented in Chapters 5 and 7.

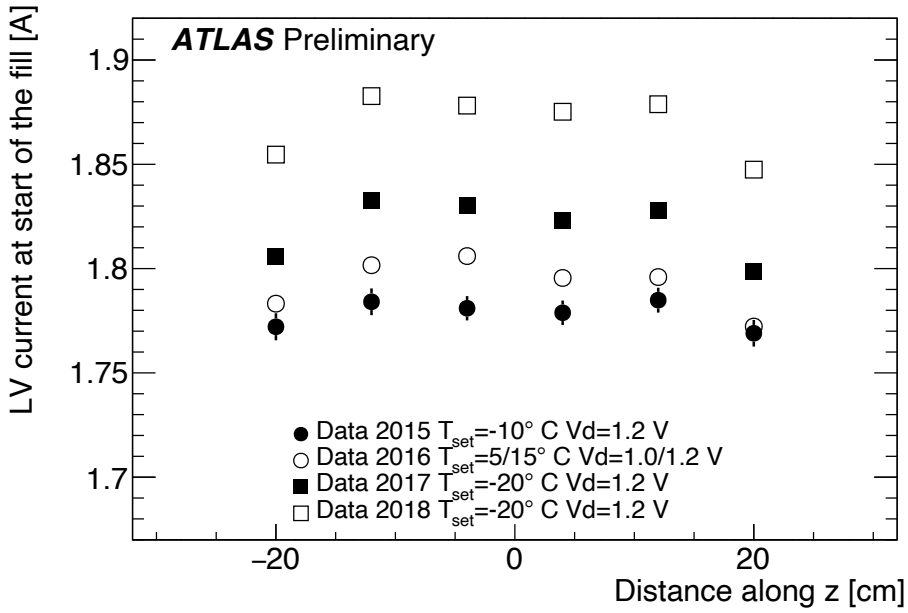


Fig. 83: Mean IBL LV current at the start of the stable beam fills during Run 2 (pre-amplifiers turned on) for different z regions.

6.1.2 SEU/SET studies on IBL and SCT detectors

An overall theoretical description of SEU/SET effects in electronics is given in Section 2.2. In this section we will present the experimental observations on the ATLAS IBL and SCT detector electronics, giving the results of detail studies performed during the LHC Run 1 and Run 2 periods [7], including the adopted mitigation strategies and the plans for the future operation in Run 3.

6.1.2.1 SEU and SET measurement in IBL front-end chips

The readout integrated circuits in the ATLAS IBL detector are custom designed with SEU-hardened memory cells [8] (dual interlocked cells or DICE latches [9] and triple redundancy). These reduce the SEU rate, but do not completely eliminate it. The effects of SEUs were indeed visible in the behaviour of the FE-I4B during 2017, when the LHC peak luminosity increased further respect to 2016 and was constantly above $1.5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. Under these conditions, more frequent front end re-configurations were needed to preserve good data quality and data taking efficiency.

Impacted FEs can stop sending hits, become very noisy, or experience large drops/increases (up to ± 100 mA) of the LV current consumption monitored from the detector control system (DCS) (see Fig. 84).

Since 2016, part of the SEU/SET effects was treated by occasional reconfiguration of the problematic modules. However, to minimize the impact of SEUs on ATLAS data taking, it was later decided to regularly reconfigure the global registers of the FE-I4B chips in the entire IBL.

Thanks to a joint effort of online software and firmware, it was possible to introduce this procedure without any additional dead time in ATLAS. Starting in August 2017, the global registers of the IBL FE-I4B chips were reconfigured every ~ 5 s, improving the overall data acquisition (DAQ) efficiency and eliminating the low voltage current drops that were previously observed.

Unfortunately it was not possible to regularly reconfigure also the single pixel DICE latches in the FE-I4B since the needed software modifications were impacting the overall stability of the DAQ system. However, a test run was performed in July 2018 and can be used as proof of concept for future

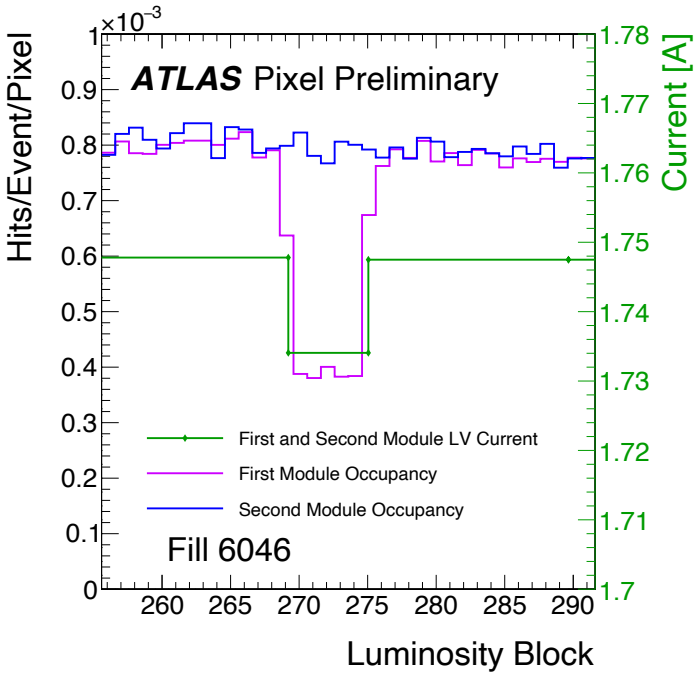


Fig. 84: Effects of SEU on FE-I4B global registers during a typical LHC fill; in this case, the peak luminosity reached $1.5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, and $490\,\mathrm{pb}^{-1}$ were delivered over the entire fill. During the data taking, at luminosity block (LB) $\sim$ 268, a drop in the LV current consumption can be observed. At the same time, a drop in occupancy is observed in one of the two DAQ modules that share the same LV power supply. At LB $\sim$ 277, the critical DAQ module was manually reconfigured, bringing the LV current consumption and hit occupancy back to their values before the SEU.

implementations.

The global configuration memory (GCM) of the FE-I4B, located at the end of the column area outside of the pixel matrix region, is implemented as a memory block of 32 words of 16 bits (512 bits in total). The design used for this global memory is based on the triplication of the DICE latch to further suppress SEU. Such triplication is not possible inside the pixel due to space constraints. An example of a fundamental parameter, vital for a proper chip functionality, is given by the global threshold, generated by a coarse and a fine DAC.

Each single pixel has instead a 13 bit configuration register, comprising a 1-bit enable flag, a 5-bit threshold tuning DAC (TDAC), a 4-bit ToT tuning DAC (FDAC), a 1-bit HitBus (input to logical OR of all pixel discriminators outputs in the matrix), and 2 bits for the selection of the charge injection capacitor. The ToT represents the time of a single pixel discriminator being over threshold and has a 4-bit resolution, in counts of an externally supplied clock, nominally 40 MHz, that corresponds to the LHC bunch crossing (BC) time of 25 ns.

The occurrence of SEUs during data taking modifies both single pixel and global front-end configurations: for the single pixel upset, quiet or noisy pixels can appear introducing buffer overflows and dead time in the FE-I4B; for what concerns the global register upset, lowering the global thresholds or changing other fundamental registers can impact severely the correct chip functionality.

Figure 85 shows the fraction of noisy pixels (meaning pixels that fire in correspondence with empty and well isolated bunches in the LHC ring) as a function of the single pixel TDAC, for a typical LHC fill in 2017. TDAC values for each pixel are taken from the initial pixel configuration. The pixels with more than 200 hits in this fill are defined as noisy. Low values of TDAC correspond to high thresholds.

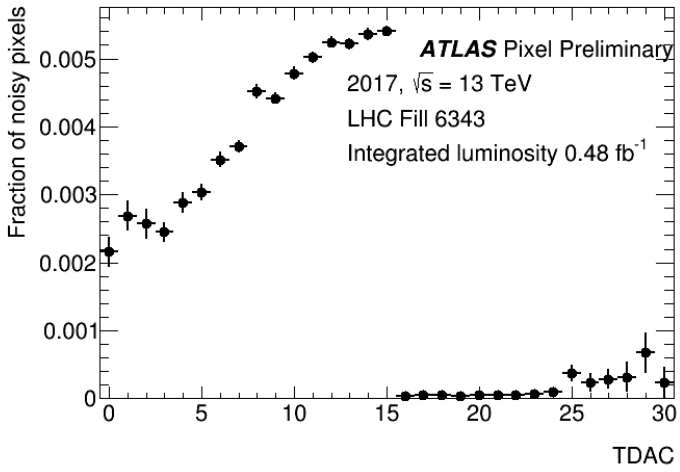
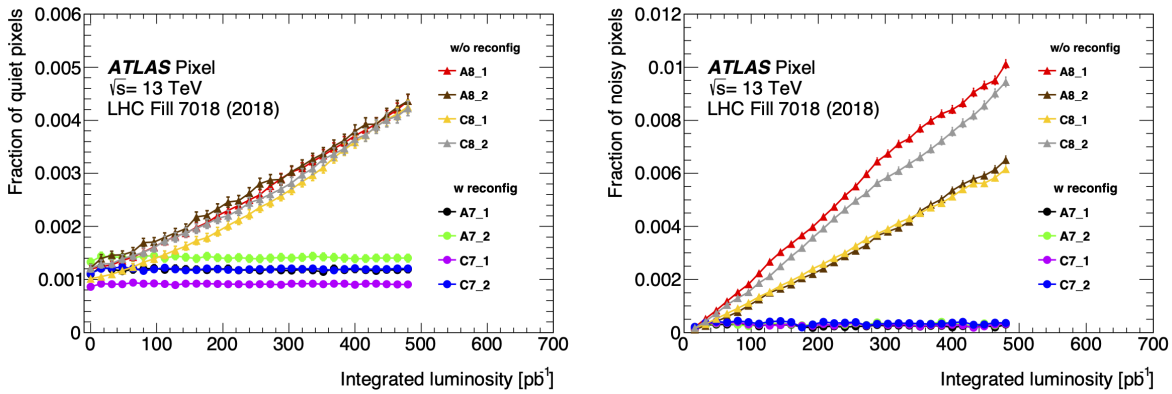


Fig. 85: Fraction of noisy pixels as a function of pixel TDAC during empty bunches of LHC fill 6343. TDAC values for each pixel are taken from the initial pixel configuration. The pixels with more than 200 hits in this fill are treated as noisy.

The higher fraction of noisy pixels with initial TDAC < 15 indicates that some pixels become noisy due to the SEU flip $0 \rightarrow 1$ of the most significant bit (MSB) of TDAC, which corresponds to lower the pixel threshold by $\sim 1850\,\mathrm{e}$ (with $2500\,\mathrm{e}$ being the typical discrimination threshold). No correlation of the noise with FDAC values was observed.

On the other hand, a pixel is defined to be quiet if it fired zero times in 16 pb^{-1} of data taking. A pixel can become quiet during data taking due to a flip on the Enable bit ($1 \rightarrow 0$). The increasing fraction of quiet and noisy pixels versus integrated luminosity ($\mathcal{L}$) for a typical LHC fill in 2018 in the eight forward 3D rings (each being an average over 14 FE-I4B with the same η coordinate) is shown in Fig. 86. Four η rings (A7_1/2 and C7_1/2) were regularly reconfigured, including the single pixel registers whilst the other four η rings (A8_1/2 and C8_1/2) were not reconfigured.



(a) (b)

Fig. 86: Fraction of quiet (a) or noisy (b) pixels versus integrated luminosity in fill 7018 from 2018, shown in the eight 3D IBL η rings.

Module-to-module differences in the initial number of quiet pixels indicate different fractions of silent pixels, which fire zero times during the entire fill. The fraction of pixels that become quiet due to SEU is seen to increase linearly with integrated luminosity. The dependence of the number of quiet pixels as the function of luminosity was fitted with a linear function $p_0 + p_1 \cdot \mathcal{L}$, where the mean p_1 is

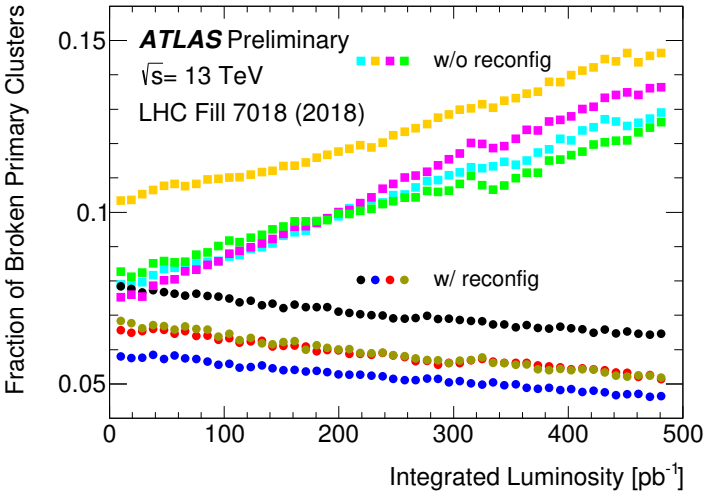


Fig. 87: Fraction of broken primary clusters versus integrated luminosity in fill 7018 from 2018, shown in the eight rings of 3D modules. Half of the modules were left without reconfiguration, whilst the other half were regularly reconfigured, including the single pixel registers.

$5.4 \pm 1.3 \times 10^{-3}$ fb.

The fraction of pixels that become quiet due to SEU ($p_1 \cdot \mathcal{L}$) is equal to the ratio $N_{\text{errors}} \,/\, N_{\text{latches}}$ in Eq. 29. The pixel latch SEU cross-section in FE-I4B is calculated with the 'quiet-pixel-fraction':

$$\sigma = \frac{p_1 \cdot \mathcal{L}}{\Phi} \,. \tag{29}$$

The predicted flux of hadrons with energy above 20 MeV with PYTHIA/FLUKA simulations in the extreme outside 3D sensor IBL module is $\Phi = 0.91 \times 10^{13}$ hadrons (T $>$ 20 MeV) cm^{-2} per 1fb^{-1} (see Table 6 in Chapter 4). The SEU cross-section is calculated to be $(0.60 \pm 0.14) \times 10^{-15}$cm^2, which is of the same order of magnitude as the test beam result [8].

The number of clusters produced by primary charged particles from a 13 TeV pp collision vertex (referred to as 'primary clusters') is proportional to luminosity. Quiet pixels can cause clusters to be broken. In the 3D modules, the average length of a primary cluster is nine pixels, so broken clusters are a very sensitive probe of quiet pixels caused by a flip of the SEU Enable bit from $1 \rightarrow 0$. If two clusters are separated by a one-pixel gap along z and Δrow is no larger than three pixels, then these clusters are assumed to be broken from one long cluster. Background where two clusters are close together due to random coincidence is flat in Δrow. Figure 87 shows the fraction of broken primary clusters versus integrated luminosity in fill 7018 from 2018, in the 8 rings of 3D modules. The rings were no single pixel reconfiguration was applied show the increase in the number of broken clusters with luminosity. On the other hand, rings where pixel reconfiguration was regularly done show a decrease of the fraction of broken clusters, that corresponds to a decrease of the fraction of quite pixels visible in Fig. 86 (a).

Figure 88 shows the average fraction of quiet pixels in each chip ring after $\sim$480 pb^{-1} of data taking in LHC fill 7018. It is compared with the PYTHIA/FLUKA simulation, which is normalized to the average fraction in data.

The FE-I4B provides the functionality to read back the content of the DICE latches by copying the latch content in the Shift Register (SR) for each double column and transmitting it back to the readout drivers (RODs). The SEU measurement scheme is to write to a register in the device being tested, let a certain fluence of particles traverse the device, and then read back the register. The fraction of pixels in which the bit state flips ($\frac{N_i(0)-N_i}{N_i}$ $(i = 0, 1)$) after taking data of integrated luminosity $\mathcal{L}$ depends on the

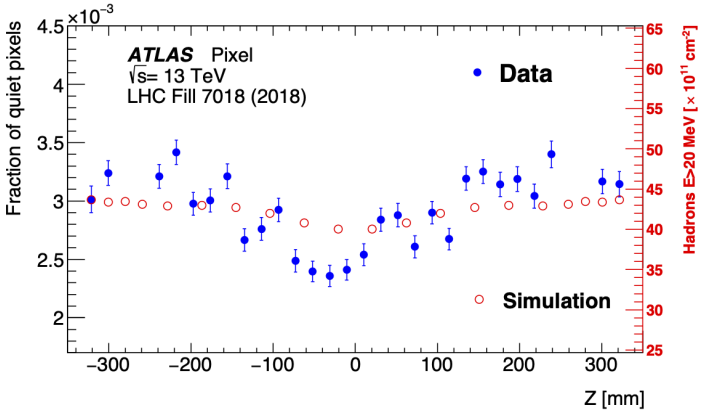


Fig. 88: Average fraction of quiet pixels in each IBL chip ring after $\sim 480\,\mathrm{pb}^{-1}$ of data taking in LHC fill 7018 of 2018, compared with PYTHIA/FLUKA simulations. Four points are missing due to the reconfiguration tests happening during that fill in four specific front-end rings.

probability of $0 \to 1$ ($P_{0\to1}$) and $1 \to 0$ ($P_{1\to0}$) transitions:

$$\frac{N_1(0) - N_1}{N_1} = P_{1\to0} \cdot \mathcal{L} \tag{30}$$

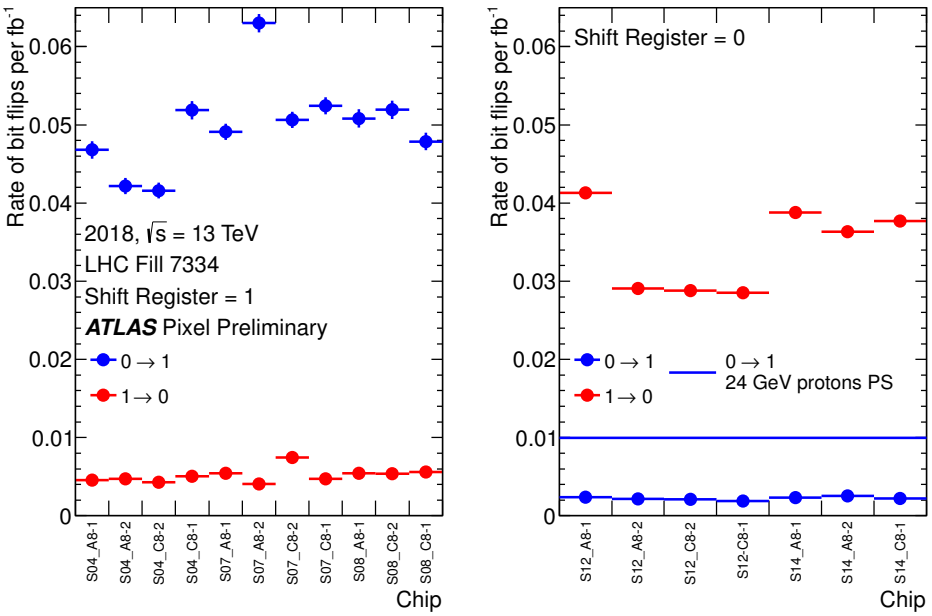
$$\frac{N_0(0) - N_0}{N_0} = P_{0\to1} \cdot \mathcal{L}\,. \tag{31}$$

Read back cannot be performed while a FE receives trigger signals, so there are only two read-backs for planar modules: before the start of the collisions and after beam dump. The first point is zero by construction. $P_{0\to1}$ and $P_{1\to0}$ are extracted from these measurements. This procedure allows for an independent measurement of the SEU probabilities for each of the 13 pixel latches.

The $0 \to 1$ and $1 \to 0$ transition probabilities have been measured for the pixel latch memories. The simulation of the SEUs in DICE memories [10–12] demonstrates that the dominant effect comes from glitches on the LOAD signal. The LOAD signal stores into the DICE latch the current content of the SR. In this case, the polarity of the transition depends on the actual values stored in the SR. The last bit (out of 13 bits) loaded into the SR is the output enable bit. As the enable bit is usually 1, this favours $0 \to 1$ transitions.

These asymmetries were studied in detail during LHC fill 7334 with the read-back method. The probability of a pixel memory bit flip strongly depends on the value stored in the input SR. Pixel memory read-back results and chip simulations confirm that the FE-I4B SEEs are dominated by single event transient effects (SET), which create fake LOAD signals. $0 \to 1$ flips in pixel memory are dominant when the SR is loaded with 1, and $1 \to 0$ flips are dominant when SR is loaded with 0. The average rate of the SEU/SET bit flips in pixel memory of FE-I4B per fb^{-1} was studied in LHC fill 7334 as a function of the chip number. In Fig. 89 (a), the SR was set to 1, and $0 \to 1$ flips dominate due to the SET on the LOAD line, while low rate $1 \to 0$ flips are due to real memory SEU. In Fig. 89 (b), the SR was set to 0, and $1 \to 0$ flips dominate. The values of the SR are refreshed several times during the LHC fill. The extrapolation of the measurement of the SEU rate with 24 GeV protons at CERN PS is shown with a blue line in Fig. 89 (b). During the CERN PS measurement, the value of the SR was not refreshed, which may explain the higher rate of bit flips due to SET contributions. Figures 89 (a) and (b) present different chips at slightly different locations, so part of the difference may come from chip-to-chip process variations, tuning, and particle flux differences.

In the same fill, the average rate of the SEU/SET bit flips in pixel memory was studied as a function of the bit number (0-12). In Fig. 90 (a), the SR was set to 1, and $0 \to 1$ flips dominate due to the SET on the LOAD line, while low rate $1 \to 0$ flips are due to real memory SEU. In Fig. 90 (b), the SR is set to 0,



(a) (b)

Fig. 89: In (a), the SR was set to 1, and $0 \rightarrow 1$ flips dominate. In (b), the SR was set to 0, and $1 \rightarrow 0$ flips dominate. The extrapolation of the measurement of SEU rate with 24 GeV protons on CERN PS is shown with blue line in (b).

and $1 \rightarrow 0$ flips dominate. Flips in bit-8 (HitBus) are twice as frequent, probably due to specific layout of that memory bit.

During LHC fill 7333 the values of the global configuration memory were read back several times and compared with the initial setting. In Fig. 91, the cumulative fraction of SEU/SET bit flips in the global configuration memory of FE-I4B is shown as a function of integrated luminosity.

The high rate of $0 \rightarrow 1$ flips is probably due to SET on the LOAD line with register value 1. The pattern 0xFFFF was loaded last into the SR. The values of the SR are refreshed several times during the fill. No $1 \rightarrow 0$ real SEU transitions were observed during the fill due to the triply redundant memory design. For the calculation of SEE cross-sections, we use the average prediction of the flux of hadrons with energy above 20 MeV[4] in the two outer 3D IBL modules: $91.0 \times 10^{11}\text{cm}^{-2}\text{fb}^{-1}$. This flux was calculated from 13 TeV proton–proton minimum bias events generated using PYTHIA8 [14], applying the A3[5] tune to ATLAS data, and using NNPDF23LO Parton Density Functions (PDF) [15]. The flux of hadrons in the ATLAS detector was simulated using FLUKA version 2011.2x particle transport code [16]. The systematic error on the hadron flux was estimated to be $\sim 30\%$.

In Table 12, we summarize the measured rates and SEE cross-sections. The rates presented are averages over all available chips and 12 pixel memory bits, excluding the HitBus bit (which shows abnormal rates related to the special layout interconnecting all pixels in the matrix). The systematic errors on the SEE rates were calculated from the RMS spread of the rates in different IBL chips and in different pixel memory bits for SEU and SET dominated samples. SET cross-sections are greater than SEU cross-sections by a factor of 10. Some differences in $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions are observed, but fall within the systematic errors. These variations are related to differences in the geometrical positions of the chips, differences in process variations, and differences in the mixture of SEU and SET effects.

The measured cross-sections are compatible with the cross-sections measured with 24 GeV pro-

[4]The choice of 20 MeV hadron energy cut was justified in Ref. [13] by effective reduction of SEU effects below this energy.
[5]A3 is one of the tunes of PYTHIA8 Monte-Carlo generator to the ATLAS LHC data.

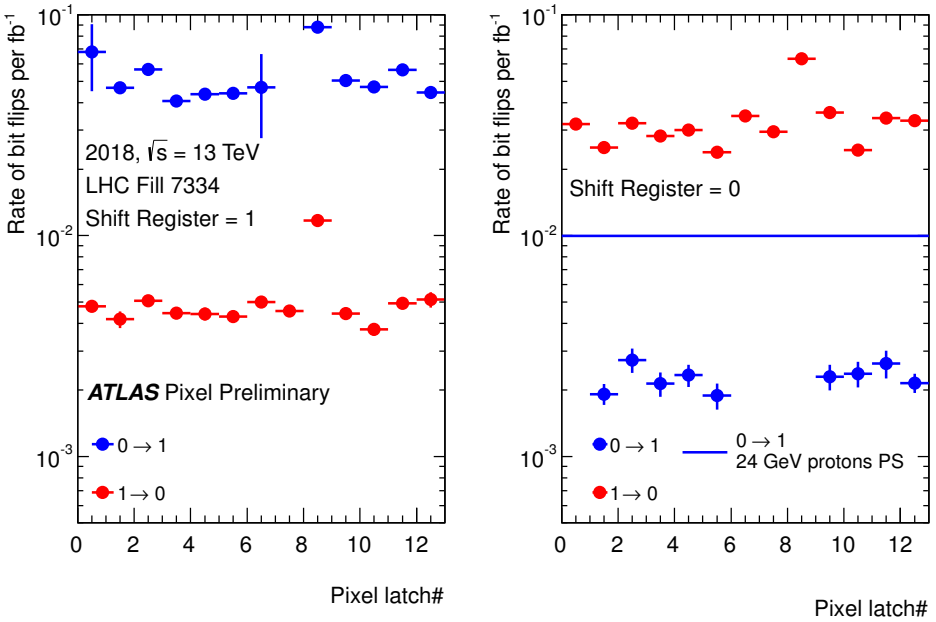


Fig. 90: Average rate of SEU/SET bit flips in pixel memory of FE-I4B per fb^{-1} in LHC fill 7334, as a function of bit number (0-12). In (a), the SR was set to 1, and $0 \rightarrow 1$ flips dominate. In (b), the SR was set to 0, and $1 \rightarrow 0$ flips dominate. The extrapolation of the measurement of the SEU rate with 24 GeV protons at CERN PS is shown with a blue line.

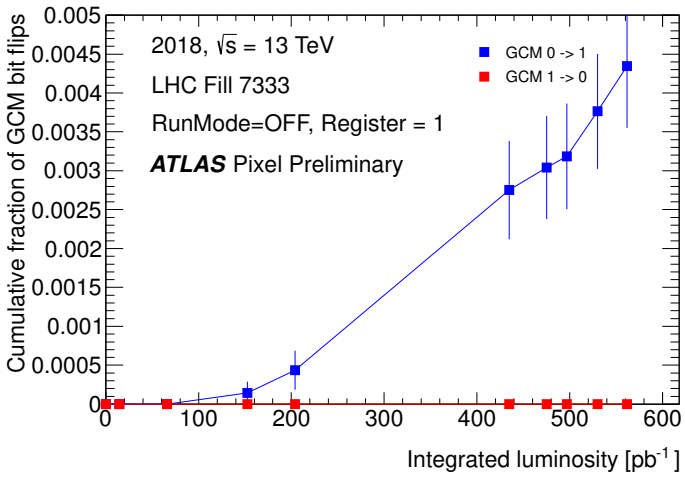


Fig. 91: Cumulative fraction of SEU/SET bit flips in the global configuration memory (GCM) of FE-I4B as a function of integrated luminosity in LHC fill 7333.

Table 12: Summary of measured rates and SEE cross-sections

Beam, SEE type	**Transition**	**SR** value	**Rate per fb^{-1} (%) (stat./syst.)**	**Cross-section 10^{-15} cm^2**
LHC: mainly SEU	$0 \to 1$	0	$0.22 \pm 0.01 \pm 0.09$	0.24 ± 0.13
LHC: mainly SEU	$1 \to 0$	1	$0.46 \pm 0.01 \pm 0.19$	0.51 ± 0.26
LHC: mainly SET on LOAD line	$1 \to 0$	0	$3.07 \pm 0.02 \pm 0.80$	3.39 ± 1.34
LHC: mainly SET on LOAD line	$0 \to 1$	1	$4.68 \pm 0.03 \pm 1.21$	5.16 ± 2.04
24 GeV protons Mostly SEU with some SET admixture	$0 \to 1$	0	n.a.	1.10

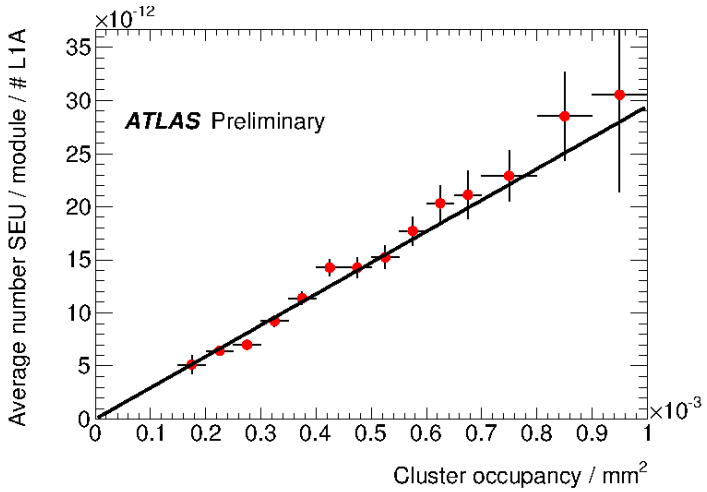


Fig. 92: SEU rate per module versus module cluster occupancy. The line shows the result of a linear fit through the origin.

tons at CERN PS. So for future HL-LHC experiments, measurement of SEE cross-sections using the 24 GeV proton PS beam is recommended, and special attention should be paid to the optimization of chip design not only against SEU, but also against SET effects.

6.1.2.2 SEU in SCT front-end chips

From test beam data single event upsets (SEU) are expected in the on-detector p-i-n diodes that receive the TTC data and in the ABCD ASICs. Extrapolations of the test beam results were used to compare with the measured *in situ* results [17].

p-i-n diodes

While no direct measurements of SEU rates could be performed *in situ*, the occurrence of SEUs led to a characteristic signature of synchronization errors [17]. The characteristic signature for a genuine SEU is the occurrence of a burst of events which fails this synchronization test. The correlation between the measured SEU rate and the cluster occupancy in a module in a given run is shown in Fig. 92. The cluster occupancy is a good proxy for particle flux, as the rate of noise hits is negligible.

The measured number of SEUs in a data set corresponding to an integrated luminosity of 8.69 fb^{-1} was 2504. The value of the SEU cross-sections determined from the test beams was used to predict the

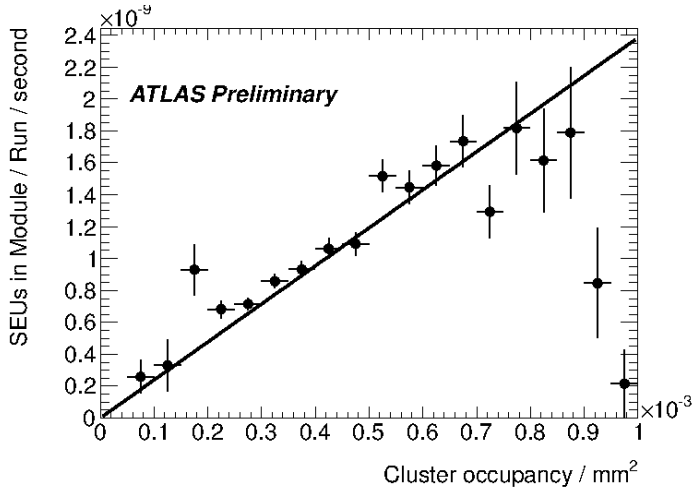


Fig. 93: Rate of SEUs in the ABCD DAC registers versus the module occupancy in a run

number of SEUs. The value determined was 1900 which is in reasonable agreement given the uncertainties in the extrapolation [17].

ABCD registers

SEUs in the ABCD registers cannot be directly identified during ATLAS operation. However, an indirect determination of SEUs in the ABCD register that sets the DAC value for the threshold is possible. The MSB is normally set to '1' and if an SEU causes it to be flipped to a '0' the threshold would become below the baseline. This would then result in a very high occupancy until the register was reset. This allowed the detection of SEU bursts. To demonstrate that these candidates are genuine SEUs, the rate was measured as a function of fluence. The results are illustrated in Fig. 93 and also show the expected linear relationship. The measured number of SEU events in a data set corresponding to 20.3 fb^{-1} was 3046 ± 100. Simple extrapolation of the measured SEU cross-sections at test beams gave a prediction of 1000 [17]. The discrepancy is probably a reflection of the uncertainties in the extrapolation of the SEU cross-sections with energy. Mitigation strategies including regular resets have reduced the data loss due to SEU to a negligible level.

6.1.3 Optical links studies in SCT

The radiation damage in the optical links was measured *in situ* [18] and compared with extrapolations of test beam data [19], [20]. The radiation induced damage expected at the end of Run 3 can be accommodated in the links power budgets.

6.1.3.1 VCSELs

The optical power of the on-detector VCSELs was measured in special runs by measuring the photocurrents in the off-detector p-i-n diodes which received the light. The optical power decreased linearly with luminosity. The decrease in optical power was measured in different regions of the SCT that were exposed to different fluences. The results of these measurements [18] are summarized in a plot of the change in VCSEL output versus the fluence (see Fig. 94). Assuming that the threshold current and slope efficiency change linearly with fluence the results can be compared to test beam data with and without annealing. As these links have had more annealing time than used in the test beam studies, the plot indicates that the radiation damage is slightly larger than expected.

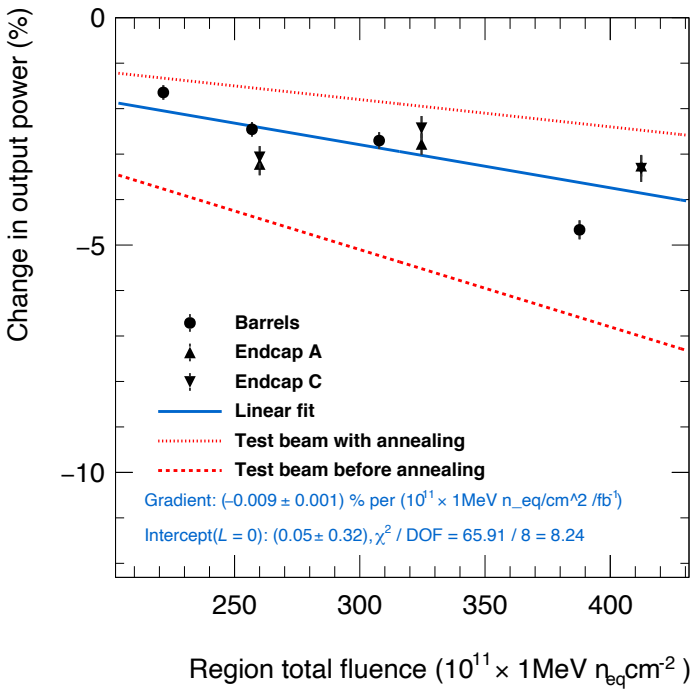


Fig. 94: Plot of the change in VCSEL output versus fluence for the different regions of the SCT

6.1.3.2 The p-i-n diodes

The radiation damage in the p-i-n diodes was studied *in situ* by measuring the photo-currents for the on-detector devices. The decrease in responsivity is not linear and tends asymptotically to a fixed value. The results of these fits are shown for one layer of the barrel in Fig. 95. The other regions gave similar results [18] and the weighted mean value for the asymptotic decrease of responsivity was $R_{\infty}^{\text{eff}} = 0.731 \pm 0.027 \pm 0.046$, which is in good agreement with the value of 0.71 obtained in test beam measurements [19].

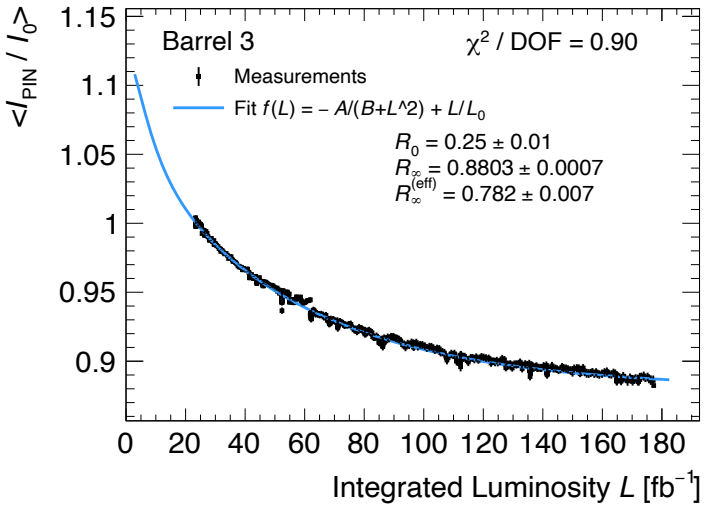


Fig. 95: On-detector p-i-n diodes. Each point represents the mean value for one day averaged over all modules in this layer. The value is the normalized mean value of the photo-current I_{PIN}.

6.1.4 Irradiation effects in TRT electronics

The signals coming from the TRT straws are detected by custom designed electronics [24]. The analogue part of the electronics 'amplifier, shaper, discriminator and baseline restorer' (ASDBLR) performs the amplification, shaping, discrimination and base-line restoration against the long trailing signal caused by the drifting ions. ASDBLR is capable of detecting signals at two different thresholds: a tracking threshold about 200 eV (low-level level threshold), and the transition radiation threshold about 5 keV (high-level level threshold). The output is a ternary signal, with the first level indicating the time the input signal exceeded the low threshold and the second level indicating the time the input signal exceeded the high threshold. The digital readout chip for the TRT is the 'drift time measurement/read out chip' (DTMROC). A DTMROC receives the signals from two ASDBLR's, that is from 16 straws. It samples each input eight times per 25 ns bunch crossing in 3.125 ns intervals. It also determines whether the high threshold was exceeded in each bunch crossing. The high and low thresholds for a ASDBLR are set by two registers in a DTMROC. DTMROCs are also capable of injecting test charge to ASDBLRs which is shaped similar to the integral of the expected ionization signal in a xenon filled straw in TRT. When a L1A signal is received, the data is sent from DTMROCs to the back-end consisting of the TRT Read-out Driver and subsequently the ATLAS central ROS system [25].

The TRT front-end electronics is susceptible to radiation damage caused by the intense particle flux coming from beam collisions. There are two important effects: irreversible radiation damage on the gain and the offset of the ASDBLR transistors, and the temporary radiation damage (SEU) in the DTMROCs.

6.1.4.1 Effective threshold shift in ASDBLR

Transistors are sensitive to displacement damage from neutrons, protons, pions, and other interacting particles such as kaons. In ASDBLRs, this causes an increase in current at the base of the transistors of the pre-amplifiers, which lowers the gain [24]. The loss of gain can manifest itself both as a decrease in the gain of the amplifier and as a shift in the offset. Both of these effects can contribute to an effective shift in the low or high threshold. Extensive irradiation tests, to many tens of Mrad, were carried out on the electronics prior to the construction of ATLAS and no significant effects were to be expected in either Run 1 or Run 2. However, during Run 1, it was observed that the detection efficiency for $Z \rightarrow ee$ decreased slowly during the run [26]. This was traced to a small shift in the effective high threshold. While similar shifts in the effective low threshold also occurred, it did not cause observable effects since the low threshold was adjusted regularly to maintain a constant noise occupancy. On the other hands, the high-level thresholds were not tuned time to time as it was expected that any small shifts that might occur would not affect the efficiency for electron identification.

This phenomenon, which was not observed in the former irradiations tests since they were performed only with higher dose, was investigated using a cobalt-60 source that produces gamma-rays at 1.17 MeV and 1.33 MeV at Brookhaven National Lab (BNL). Sets of TRT endcap front-end boards (triplet with 12 DTMROCs, 24 ASDBLRs, 192 ASDBLR channels) were irradiated with various doses: 30 krad which is roughly equivalent to the total Run 1 dose, 60 krad, and 500 krad. The metric of interest is the effective low-level threshold defined as the at the low-level threshold which the ASDBLR outputs would produce a 50% occupancy; measurements were made both with zero injected charge and with an injected charge from the DTMROCs with a pulse height corresponds to an ionization energy of typical low-level threshold hits (400 eV). Figure 96 shows the shift in the effective low-level threshold measured with and without charge injection. The observed shift, corresponding to an ionization energy of about 30 eV, after 30 krad is similar to that observed in the detector during Run 1. Tests to higher total dose rates showed no further shift up to 500 krad.

Measurements of the shift in the high-level threshold after irradiation at BNL were not recorded. However, a similar examination is performed in the ATLAS TRT by similarly measuring the 50% occupancy high-level threshold regularly over the time of Run 1 and Run 2. Figure 97 summarizes the

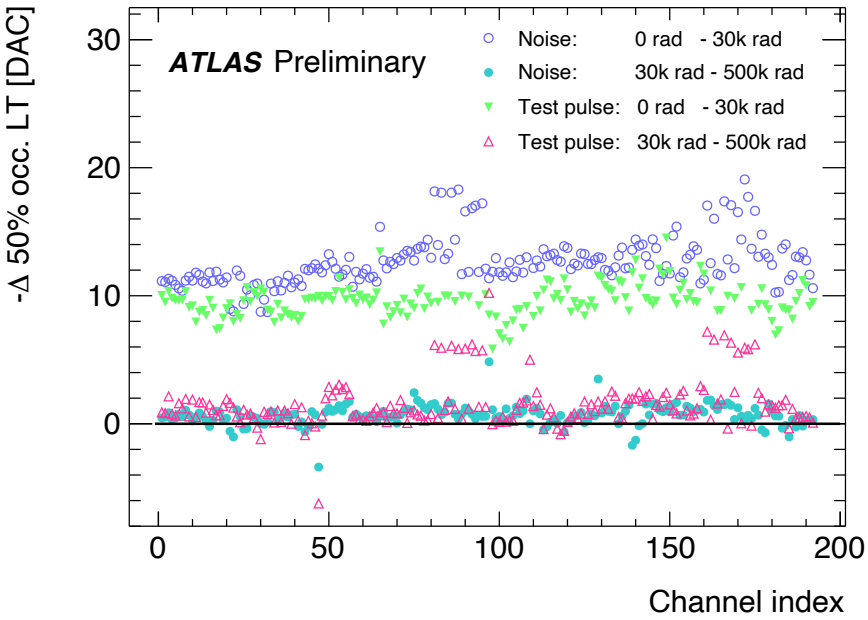


Fig. 96: The magnitude of negative shift in the effective low-level thresholds (LT) of ASDBLR chips after being irradiated by a Co^{60} source at BNL. The effective low-level threshold is determined as the DAC value that yields 50% occupancy for noise or a test pulse which corresponds to an ionization energy of 400 eV. The individual shifts of 24 ASDBLRs (192 channels) on a test board are shown. A shift of 12–13 DAC counts, corresponding to an ionization energy of about 30 eV is observed for both threshold definitions after an irradiation of 30 krad, which corresponds to the average dose accumulated in the inner layer of the TRT over the course of Run 1. No significant shift is seen for additional irradiations up to 500 krad, except for the three chips which saturated at about 60 krad.

chronological change of effective high-level threshold measured using the test pulse with the height equivalent to an ionization energy of 1.9 keV. The shift is clearly observed during Run 1 and was sufficient to cause the observed decrease in electron efficiency. The effect saturates after about 30 krad and there is no further shift during Run 2, which is consistent with what is found in the low-level threshold in the BNL experiment. Nonetheless, the high-level thresholds used for operation have been updated since the beginning of the Run 2 to compensate for any possible shift, calculated based on the extrapolated 50% occupancy threshold shift at the test pulse height equivalent to the transition radiation signal which is about 5 keV ionization energy equivalence.

6.1.4.2 Single event upset in DTMROCs

When a charged particle or electromagnetic radiation traverses digital micro-circuitry, secondary ionization charges can cause internal logic elements to change their state (SEU 'bit flips'). In the DTMROCs the bits that are susceptible to SEUs are:

(1) straw hit data bits in the buffer;
(2) event identifier bits associated with the straw data;
(3) the bit flips in the registers storing the configuration information.

While the former two have relatively limited impact on the data taking either because only small subset of data is read out on the L1A or because they are frequently reset according to the LHC orbit, the SEUs on the configuration registers can cause serious impact. The general configuration and the threshold information are the most critical part of the configuration registers. Therefore they are triplicated and

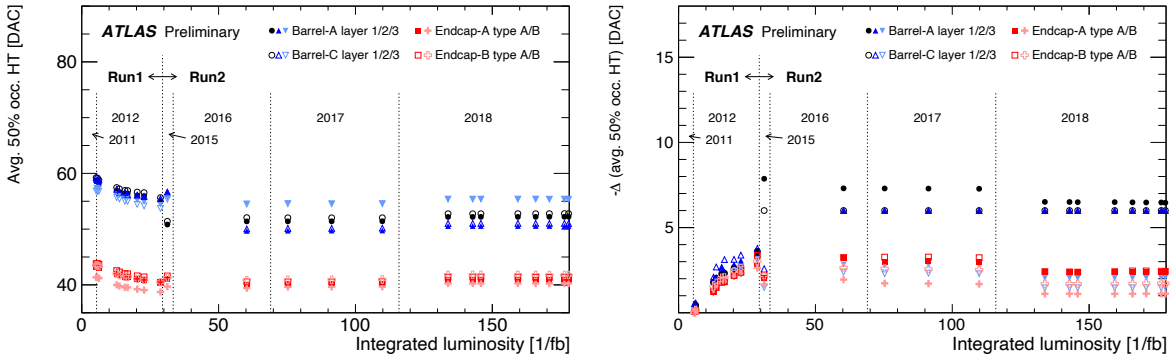


Fig. 97: (a) The effective high-level threshold (HT) of ASDBLR chips and (b) its decrease since the beginning of 2012, as function of integrated luminosity recorded in the ATLAS over the last year of the Run 1 (2012) and Run 2 (2015–2018). The HT is determined as the DAC value that yields 50% occupancy for a test pulse which corresponds to an ionization energy of 1.9 keV. Values are shown separately for the A side and C side of the detector for the three barrel layers and groups of endcap layers with type A and type B front-end boards, which largely correspond to the low-/high-z part of the endcaps. All shown values are averaged over all channels in the respective detector part. The TRT active gas mixture of barrel layers 1 and 2 have been changed between Run 1 and 2015; and between 2015 and 2016. This required a change of the ASDBLR shaping, which resulted in a large change in the HT. The other changes to the HT during Run 2 are still being investigated, however, they are unrelated to radiation as the changes are independent of integrated luminosity.

automatically corrected using the parity logic in the DTMROCs. A polling scheme is also implemented in the TRT DAQ system to monitor and correct the DTMROC configuration registers. This is done by the TRT-TTCs requesting read back during the 199 bunch-crossing long beam gap booked at the end of the orbit, and compare the register information to the originally written configuration from the TRT-TTC. Any mismatch is logged in the database. The registers regarding to the general configuration and the thresholds are additionally re-written once the bit changes are detected. The polling is done sequentially and each DTMROC channel is fetched at about 10 Hz.

A SEU rate measurement has been performed utilizing this polling system during the $\sqrt{s} = 7$ TeV operation in 2011, or the $\sqrt{s} = 13$ TeV operation in 2015-16. After removing the events recorded due to the other known reasons such as bad communication between the TRT-TTCs and the DTMROCs, 46 and 1016 SEU events are observed in total during the $\sqrt{s} = 7$ TeV operation in 2011 and the $\sqrt{s} = 13$ TeV operation in 2015-16 respectively. Figure 98 shows the calculated SEU rate for the entire TRT as function of the average instantaneous luminosity in the various selected run period. A good linearity with respect to the instantaneous luminosity at the same centre-of-mass energy is found. The SEU cross-section per DTMROC chip is derived as $(1.2-5.7) \times 10^{-14}$ cm^2 given the particle fluence in the TRT (charged and neutral hadrons with $E > 20$ MeV: $4.0 \times 10^{11} - 1.8 \times 10^{12}$ cm^{-2} per 1 fb^{-1} of integrated luminosity depending on the position [27]), and the total number of chips (22 016). This is largely consistent with the measured SEU cross-section $(0.8 - 1.2) \times 10^{-14}$ cm^2 for the DTMROC prototypes obtained using the 24 GeV proton test beam at the CERN PS irradiation facility [28].

6.2 CMS

The CMS tracking detector consists of the silicon pixel and silicon strip detectors. Together they provide charged particle tracking in the pseudo-rapidity range of $|\eta| < 2.5$. The original CMS pixel detector [30] was running during the years 2009–2012 and 2015–2016 and was replaced with the CMS Phase-1 pixel detector [31] during the extended year-end technical stop 2016/17.

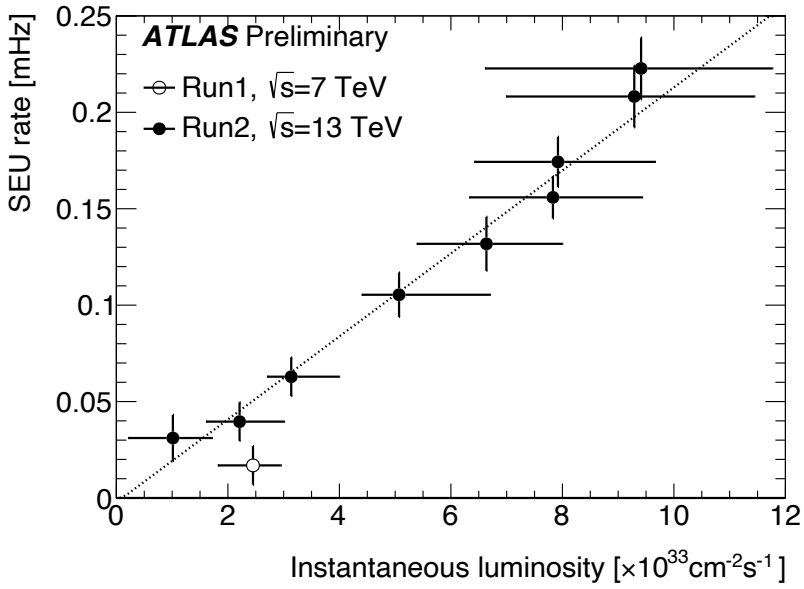


Fig. 98: Single event upset (SEU) rate in the DTMROCs measured as a function of the instantaneous luminosity observed in the ATLAS detector, using 2011 Run 1 data, collected at $\sqrt{s} = 7$ TeV (hollow dots) and 2015–2016 Run 2 data, collected at $\sqrt{s} = 13$ TeV (closed dots). The SEU rate is calculated for selected run periods for which the instantaneous luminosity is determined as the average over the respective period. The x-axis error bars represent the luminosity range from the different runs in the period. Only one point is shown for the $\sqrt{s} = 7$ TeV result due to the limited data statistics. The observed SEU rate depends linearly on the instantaneous luminosity at the same centre-of-mass energy.

6.2.1 Radiation effects in the CMS pixel detector

The CMS pixel detector and its readout electronics have been described in Section 3.2.2.1. In the following some of the radiation effects observed in both the Phase-0 and Phase-1 pixel detectors will be described.

Evolution of low voltage currents

Figure 99 shows the evolution of the analogue low voltage currents in the CMS Phase-0 barrel pixel detector over its full lifetime. The current is averaged for all ROCs belonging to the layer in question. To be comparable, the current measurements are always taken 10 minutes into an LHC fill after it has reached stable proton collisions. Several distinct features can be seen in the plot. The current rises most steeply in the innermost layers in early Run 1 necessitating a recalibration of layers 1 and 2 already after few fb^{-1}. Another two recalibrations were performed during Run 1 on all layers afterwards. It can be seen that the increase per luminosity decreases over the course of the run from initially around 0.4 mA/fb^{-1}/ROC for layers 1 and 2 gradually decreasing to 0.1 mA/fb^{-1}/ROC. For layer 3 the initial increase is lower at around 0.2 mA/fb^{-1}. The analogue circuitry is powered via a bandgap reference voltage which increases with dose. This effect has been measured for the Phase-1 PSI46dig in Ref. [34] to be around 11% for TID expected for the lifetime of the Phase-1 detector with a 10% increase below 300 kGy. The increase reaches a plateau of around 14% for very high TIDs.

Radiation and SEU effects

The SEU cross-section in 250 nm technology which is used for the readout ASICs has been measured and protection measures have been put in place [33]. The large majority of SEUs in the ROCs will not be visible as they only affect small parts of the ASIC like single-pixel trim bits and do not affect the detector

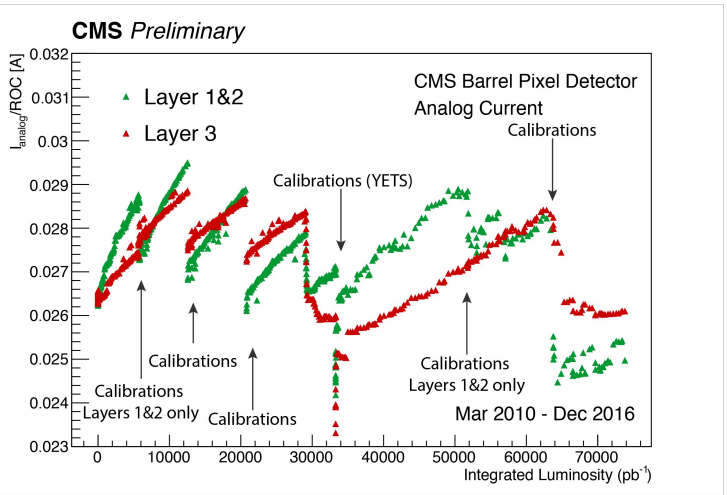


Fig. 99: Evolution of the analogue supply currents per ROC for the CMS Phase-0 pixel detector as a function of the integrated luminosity. Recalibrations, full or partial, are indicated as well as short technical stops (TS) and year-end technical stops (YETS).

response in a significant way. The data taking will be affected by SEUs when vital parts of the ASIC get affected which can happen with some probability. Also the TBM chips can be affected by SEUs in which case the readout to a group of ROCs is stopped. Both SEUs for single ROCs and TBMs get detected in the front-end driver (FED) that keeps a list of channels which do not send data. Once a programmable threshold of channels has been reached, a recovery procedure is initiated which will be described in more detail below. The threshold is adapted depending on the position in the detector and hence the potential impact on the data quality. The rate at which ROCs become fully inefficient in the Phase-0 detector was estimated from data to be around 1/2–4 pb^{-1} for the PSI46 and about 1/73 pb^{-1} for the TBM.

In the Phase-1 detector the TBM ASICs have been found to be more susceptible to SEUs because of a single non-protected transistor in the readout control. This condition cannot be recovered with a reprogramming of the chip but instead a power-on reset has to be issued. In 2017 the power cycling was performed using the DCDC converters of the Phase-1 detector. This procedure led to the discovery of the DCDC converter issue caused by a problem in the FEAST ASIC. The description of this problem is beyond the scope of this report, more details can be found in [35]. The rate at which TBM cores got stuck because of this problem was about 0.7%/100 pb^{-1} for BPIX layer 1, the worst affected region of the detector. During LS2, the innermost barrel pixel layer will be replaced. Improved versions of the readout ASICs will be deployed and the increased SEU susceptibility of the TBM will be removed for the newly installed modules. Figure 100 shows the evolution of inactive ROCs in the barrel layer 1 over a long (11 h) LHC fill with peak instantaneous luminosity around 1.5×10^{34} cm^{-1}s^{-1}.

The recovery from SEUs or SEU like effects is done by completely reprogramming the front-end ASICs. This can either be done specifically targeting affected detector regions or by performing a full reprogramming of the full detector. For the year 2018 the firmware of the front-end controllers, responsible for reprogramming of the detector modules, underwent a major revision. In the original firmware the amount of parallelism was limited by FIFO sizes and the structuring of the on-board memory. The new firmware features a segmented DDR memory and multiple segments per module with a maximum of 28 modules per channel. With the new firmware the time needed to perform pixel-level reprogramming of the detector modules decreased dramatically to only few seconds. This allowed to deploy a more complete recovery scheme for the 2018 run where a full pixel-level reprogramming of the modules was possible also in short interruptions of the data taking (making use of the CMS *soft error recovery* mechanism). In Fig. 101 the recovery time before and after the firmware update are compared. Here it is important to note that before the firmware update only a partial recovery was performed while with the

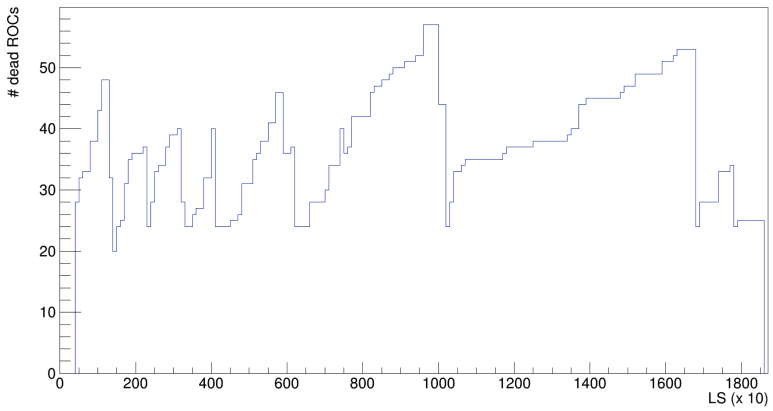


Fig. 100: The number of inactive ROCs as a function of time in BPIX layer 1 during a typical LHC fill in 2017. The number of inactive ROCs increases until a programmable threshold is reached, at which point the SEU recovery mechanism is activated and the ROCs are recovered. The SEU recovery mechanism can be activated several times during an LHC fill. The SEU rate depends on the instantaneous luminosity, which decreases over the time of the fill. In the fill used for this plot, the peak luminosity was around 1.5 $\times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The typical rate for inactive ROCs is one in five minutes at an instantaneous luminosity of 1.0 $\times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ for BPIX layer 1 modules. See Ref. [32].

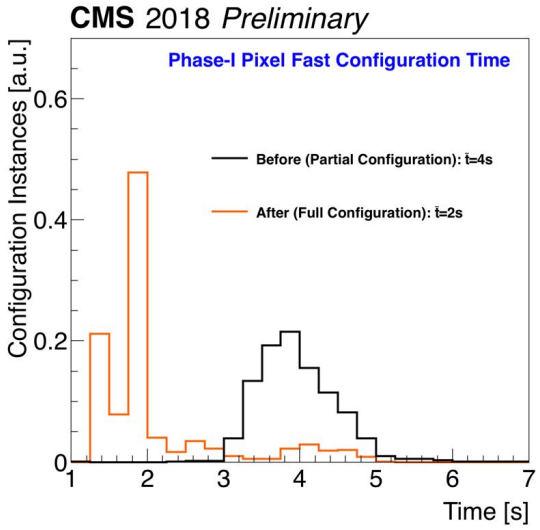


Fig. 101: Comparison of fast module configuration time before and after the PixelFEC firmware upgrade in 2018.

new firmware the full pixel-level reprogramming is carried out. The time needed for the full procedure with the new firmware is less than for the partial recovery with the old. For Run 3 a new scheme is being developed that will make use of fast reset commands to perform continuous reprogramming of pixel registers during a run.

6.2.2 Radiation effects in the CMS strip detector

The CMS strip tracker and the main components of its front-end electronics have been described in Section 3.2.2.2. In the following some of the radiation effects observed in the Front-End electronics of the system will be described.

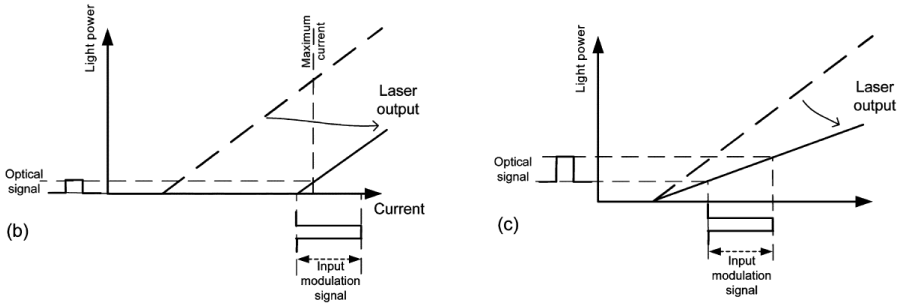


Fig. 102: Schematic laser light-current characteristics to illustrate the two main failure modes in the optical link system. Left: failure due to the laser threshold increasing beyond the maximum DC supply of the laser driver ASIC. Right: failure due to 50% loss of initial output efficiency. From Ref. [36].

Radiation effects in the optical link system

The optical links of the strip detector are expected to undergo changes in their operational performance with increasing irradiation. Extensive tests prior to installation [36] suggest ample margin should be available at the end of life of the detector. Nonetheless, the performance of the optical links is continuously monitored also during operation. To this end, a calibration procedure normally used as optical link set up run, referred to as *gain scan* in the following, is used. The gain scan is a 2-dimensional scan of the gain and bias parameters of the LLD. The gain scan makes use of a feature of the APV25 chip which emits a digital 'high' signal (referred to as *tick mark*) every 70 clock cycles in the absence of a L1A. The height of this signal at the output is 800 mV differential ($\pm$ 400 mV) and it is stable to about 5% between APV chips. The height of the tick mark at the input of the FED is measured for all combinations of bias and gain settings.

The two main radiation effects on the optical link system are an increase in laser bias voltage and a decrease in gain [37] which are also illustrated in Fig. 102. The increase of threshold current is the more prominent effect and we will focus on it in the following. In Fig. 103 the threshold increase relative to a reference point in early 2016 is shown for two of the readout partitions of the strip tracker. The links are grouped by detector layer and the marker indicates the average threshold current increase for this layer. Each year is marked in a different colour, the operating temperature of the strip tracker was changed from -15°C to -20°C in early 2018. For each year also the start of high luminosity data taking is indicated. It can be seen that the threshold increases during periods of high luminosity production as can be expected. Annealing of the current is observed especially during year-end technical stops when the detector often is brought to room temperature for brief periods. The change to -20°C is visible as an additional step down beyond the annealing, in some cases leading to threshold current below the ones from the reference point.

The expected change in threshold current with temperature can be parametrized as

$$I_{\mathrm{th}} = I_{\mathrm{th}}(0) \cdot \exp\left(\Delta T / T_0\right) , \tag{32}$$

where $I_{\mathrm{th}}(0)$ is the characteristic current and T_0 is the characteristic temperature. In order to try and obtain a measurement unaffected by different operating temperatures, the threshold current for different periods is scaled to a common reference. Various temperature measurements are available throughout the tracker but no direct measurement on the AOH is available. The temperature measurement on the front-end hybrid is taken as proxy and the rescaling to a common temperature for all time periods is performed. The result of this can be seen in Fig. 104. It can be seen that the trend seen in the non-rescaled figure is maintained but additional noise is observed, making the trend less clear. Two main effects are hypothesized to explain this effect currently, firstly the non-ideal proxy temperature on the front-end hybrid and the fact that the temperature measurements for technical reasons are not acquired directly during the gain scans but are chosen from suitable periods close in time. Especially the second

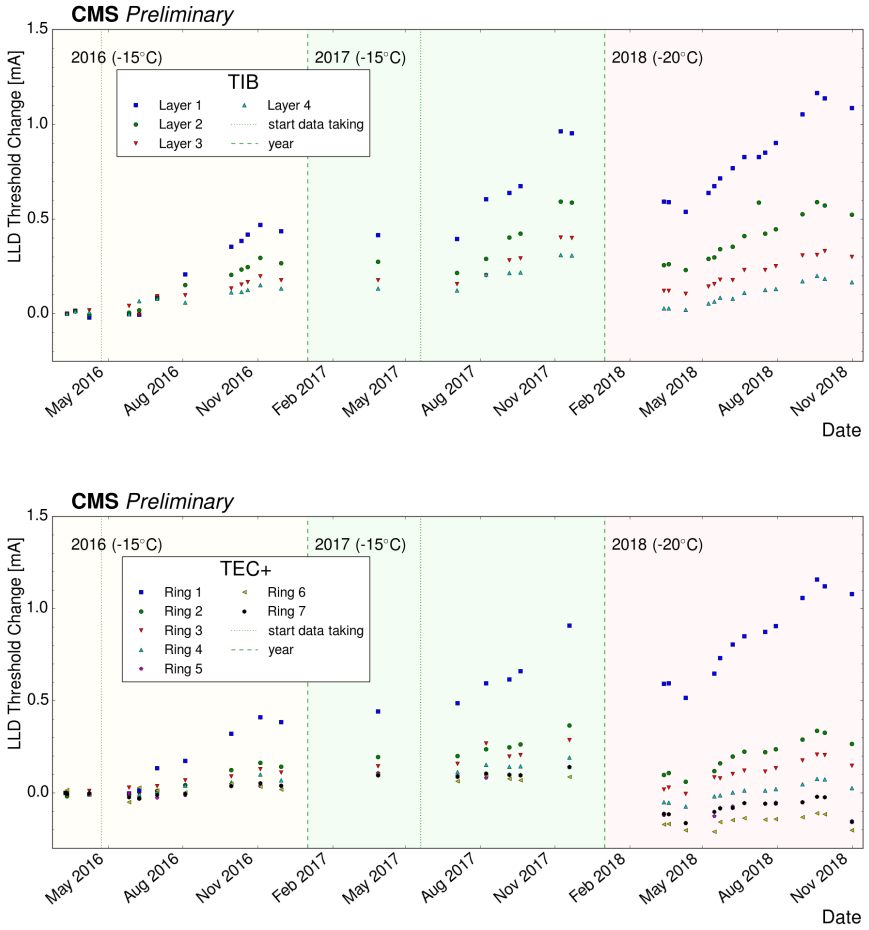


Fig. 103: Laser driver threshold increase as function of time for laser drivers in TIB (top) and TEC+ (bottom). Years are indicated in different colours, for each the start of high luminosity data taking is indicated in addition.

effect can lead to the additional spread as temperature data are taken from runs with potentially very different conditions.

The evolution of the threshold current is also compared to simulations. The data used are restricted to the running years 2016–2017 when the operating temperature of the strip tracker remained constant at $-15°C$. The simulations are performed taking into account the luminosity delivered to CMS, split into 3.5 hours equivalent to irradiation duration in qualification tests [37]. The predicted damage (and hence threshold increase) is taken as the threshold increase at the qualification fluence of 500 fb^{-1} scaled linearly to the luminosity delivered during the 3.5 hour block under consideration. The total damage is taken as the sum of the individual threshold increases also taking into account annealing based again on measurements in Ref. [37]. The comparison of the simulation to the gain scan data taking during 2016–2017 for the inner barrel is shown in Fig. 105. Very good agreement between data and simulation can be seen giving confidence in the adopted methodology and the predicted long-term behaviour of the optical links also during operating conditions. Further comparisons with data from other years are in preparation with the temperature scaling behaviour described above as one of the critical ingredients.

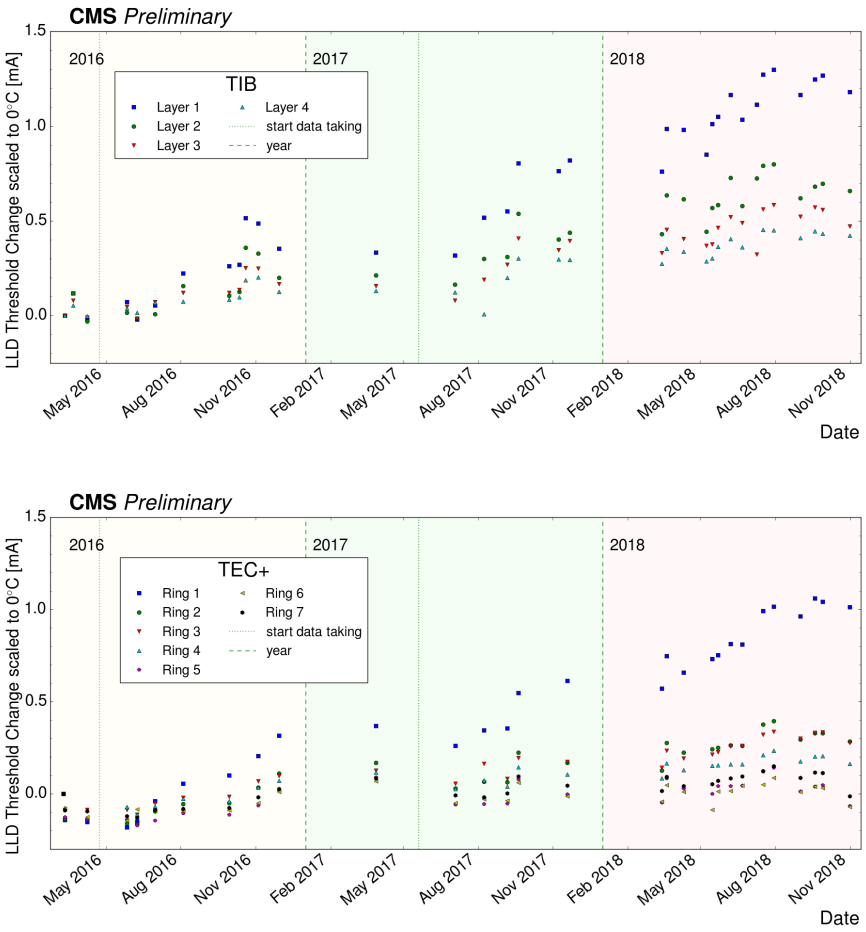


Fig. 104: Threshold current evolution as a function of time for the TIB partition (top) and TEC+ (bottom). The threshold current is scaled to 0°C. The increase is different by regions of equal radius, i.e., layers in the TIB and rings in the TEC.

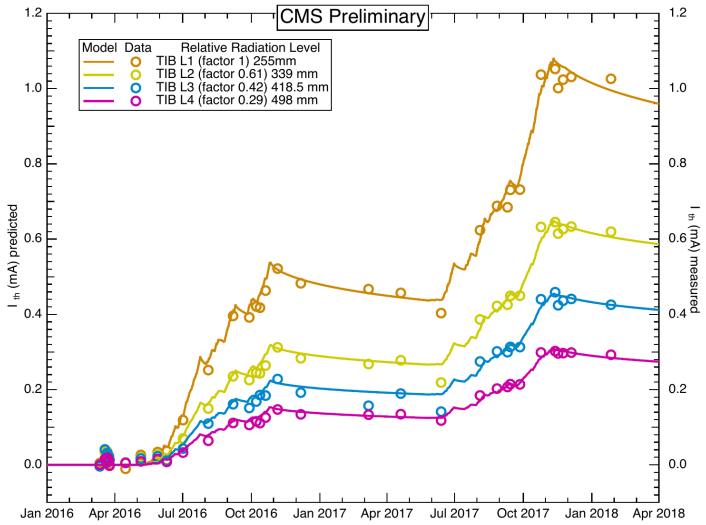


Fig. 105: Threshold current evolution as a function of time for the TIB subdetector compared to simulation.

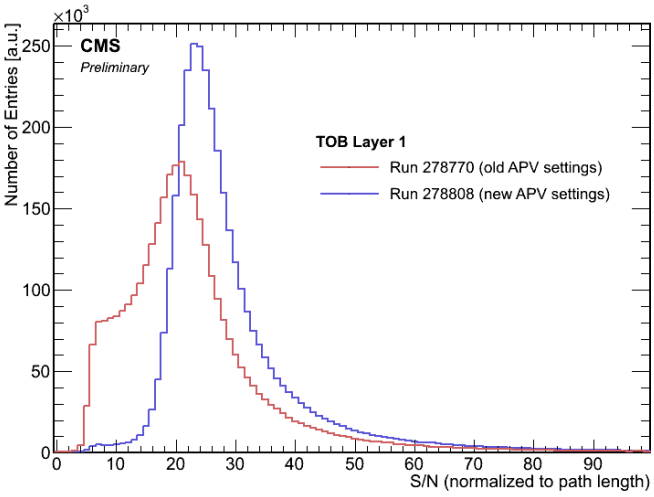


Fig. 106: Signal-to-noise distribution for hits on reconstructed particle tracks for two runs in 2016. The red curve comes from a run affected by the APV pre-amplifier saturation, the blue curve from a run with very similar conditions after the effect had been corrected.

APV25 pre-amplifier saturation

In late 2015 and early 2016 the strip tracker observed a loss of efficiency and a reduction of the signal-to-noise for clusters on particle tracks. The observed inefficiency finally reached levels of 10% of loss of hits on track for the most affected layer (outer barrel layer 1). While the initial hypothesis brought forward for the explanation of the effect was the passage of highly ionizing particles, it was subsequently found that the issue was caused by saturation effects in the APV25 pre-amplifier. The effect on the signal-to-noise distribution is illustrated in Fig. 106.

The red curve shows the signal-to-noise for clusters on tracker in the innermost layer of the outer barrel region. This is the region with 500 μm thick sensors closest to the interaction region. Two main effects on the curve can be seen: an increased population of clusters at low signal-to-noise and a shifted most probable value (MPV) for the bulk of the distribution.

The root cause for this behaviour was finally traced to a larger than expected increase in decay time of the pre-amplifier when operating at low temperature (during LHC Run 1 the strip tracker was operated at $+4\,^{\circ}$C coolant temperature). The effect was removed by a change of the pre-amplifier feedback voltage (VFD) which very much reduced the decay time of the pre-amplifier. With this change, the hit efficiency was fully recovered even at beyond design instantaneous luminosities. The signal-to-noise distribution was also brought back to the expected Landau-like shape. This is again visible in Fig. 106, where the blue curve shows the signal-to-noise after the change of VFD. It can be seen that the MPV is shifted significantly compared to the pre-VFP change situation and also the population at low signal-to-noise has disappeared almost completely. The effect on the hit finding efficiency can be seen in Fig. 107. It can be seen that the saturation effect causes a drastic decrease in hit efficiency before the change of the VFP parameter while only a very slight decrease with increasing instantaneous luminosity is seen after the change.

One hypothesis is that the residual inefficiency is caused by actual highly ionizing particles (HIP). It has been shown [39] that charge depositions from HIPs can momentarily make the APV baseline drop very strongly and make the chip insensitive to further particle hits. This effect is recovered over the timescales of few tens of bunch crossings. An analysis is performed to identify events affected by highly ionizing particles. This is done in a run where non-zero suppressed data are recorded with the strip

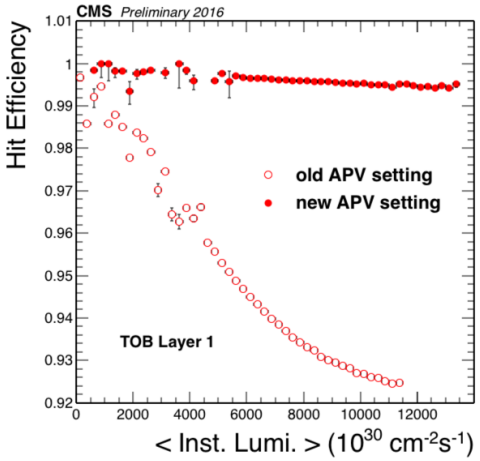


Fig. 107: Hit efficiency for clusters on tracks. The open points are data taken before the change of the APV pre-amplifier feedback voltage, and a clear decrease with increasing instantaneous luminosities can be seen. The full circles show data taken after the change. The inefficiency is much reduced and only a very slight decrease is seen as function of the luminosity [38].

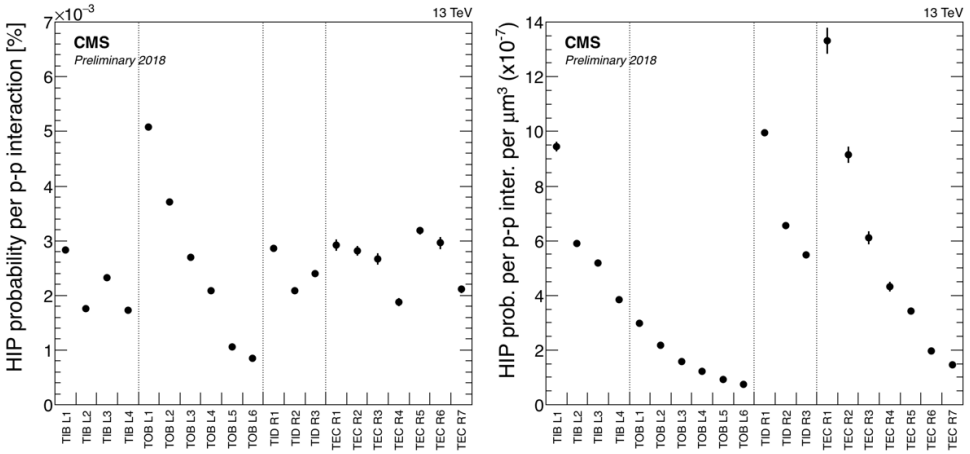


Fig. 108: Left: average probability of HIP event occurrence per pp interaction for different layers/rings of the silicon strip tracker. Right: average probability of HIP event occurrence per pp interaction normalized to unit detector volume for all layers/rings of the silicon strip tracker [38].

tracker during pp collision data taking[6]. Events affected by HIPs exhibit a strongly suppressed baseline of the APV25 with little variation between the strips. The probability of the occurrence of this type of events can be seen in Fig. 108 (left) for the different layers and rings of the strip tracker. It can be seen that the probability is again highest in the inner most layer of the outer barrel. To compensate for the effect of the sensor thickness and also the fact that the sensors with the same surface area can be read out by either 4 or 6 APV chips, the probability is normalized to a volume of 1 μm^3 read out by a given chip. This can be seen in Fig. 108 (right). It can be seen that with this normalization the probability follows a $1/r^2$ behaviour for all regions of the detector.

The residual inefficiency as function of detector layer and event pile-up is shown in Fig. 109. It can be seen that the efficiency decreases linearly as function of increasing pile-up with the effect decreasing with increasing radius. This behaviour is consistent with a higher probability of HIP-like events occurring

[6]Due to the very large event size of about 14 MB the readout rate is strongly limited and thus this mode can only be used during special runs.

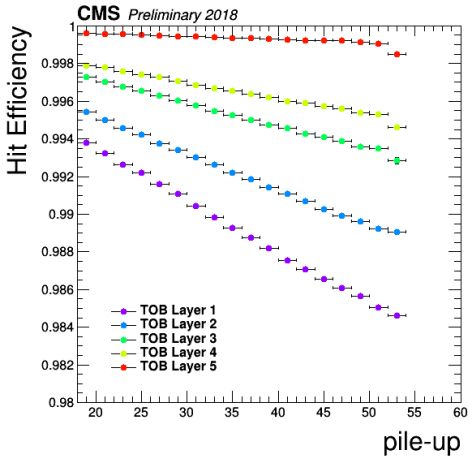


Fig. 109: Hit efficiency of silicon strip detectors from 5 TOB layers as a function of the pileup. Data from the long LHC fill 6714 (14 hours) taken in 2018 have been used. The number of colliding bunch crossings is 2544 and the peak pileup is 53.1 [38].

as function of radius and pile-up.

Noise increase in runs with no sensor bias

On a few occasions during LHC Run 2, the strip tracker observed high noise in the inner parts of endcap regions of the detector when the detector had been exposed to high luminosity beams but was fully switched off. The reasons for this configuration were for example infrastructure interruptions due to e.g., the cooling plants not being available. In order to investigate the origin of the failure a test was conducted during one of the last fills of the LHC Run 2. During this fill the powering status of modules of the inner rings of two endcap disks were changed. For one of the two endcaps, only the sensor bias voltage was turned off. For the other endcap the low voltage to the front-end electronics was turned off in addition to turning off the bias voltage. The results of this test can be seen in Fig. 110. It can be seen that high noise is present in both endcaps, i.e., irrespective of the powering status of the front-end electronics. The effect thus seems to come purely from the missing sensor bias. The effect decays with a timescale of several hours, its root cause is currently still unknown.

6.3 Discussion and outlook

The impact of radiation on tracker electronics at LHC has strong implications in the design and construction of the high-luminosity LHC detectors. The radiation effects on electronics can be separated in three main categories: TID, SEE and NIEL. A brief theoretical introduction was already given in Section 2.2. In this section we have shown the experimental observations of such effects on both electronics and opto-electronics. The operation of ATLAS and CMS trackers during the LHC Run 1 and Run 2 periods was strongly influenced by the unexpected behaviour of the detector electronics. The inner pixel layers of the two experiments were affected the most by the radiation damage.

In September/October 2015, ATLAS had to cope with a strong increase of the LV currents of the ROC (FE-I4B) in the newly installed IBL detector; this was caused by the generation of radiation induced current in NMOS transistors. CMS Pixel went through a complete replacement of the DC-DC converters (executed during the 2017–2018 winter shutdown), whose failures were also induced by the increase of leakage current in NMOS transistors.

The ATLAS IBL FE-I4B (130 nm CMOS technology) showed a strong drift of the LV currents and a de-tuning of the detector parameters, reaching a maximum of the effect between 1 and 3 Mrad.

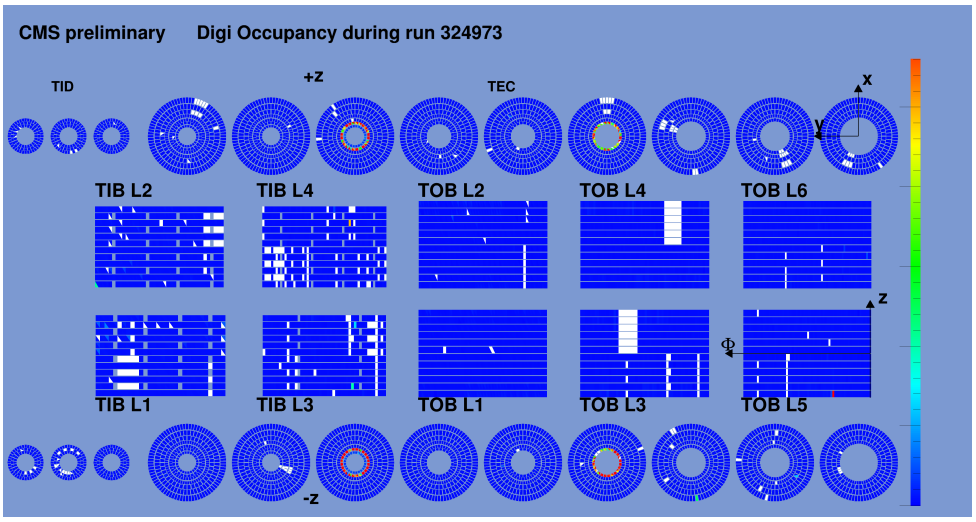


Fig. 110: Single strip occupancy from a run directly after dump of the LHC stable beams. Both sets of power groups in the positive and negative end caps which have been left without sensor bias only (TEC+) and without both sensor bias and front-end low voltage (TEC-) exhibit high occupancies.

The drift was characterized and reproduced during an X-ray irradiation campaign at CERN, where the dependency on parameters like dose rate, temperature and digital supply voltage was studied. Important guidelines were given to operate the detector safely, running temporarily at warmer temperature and lower digital supply voltage until the 'TID bump' was reached in 2016.

A similar but much less pronounced behaviour was observed in the analogue currents of the CMS pixel ROCs (PSI46v2, 250 nm CMOS technology), during Run 1 and at the beginning of Run 2 (before the replacement with the Phase-1 pixel detector chips (PSI46dig and PROC 600). For the CMS pixel ROCs in the Phase-0 detector, a regular calibration was performed in order to contain the drift of the currents. For both cases, a plateau of the TID effects seems to be reached for high dose values > 300 kGy (reached by the IBL detector during 2018); the increase was quantified to be $\sim 14\%$ for the CMS Phase-1 pixel detector.

Furthermore, a beam annealing effect was observed in the ATLAS IBL FE-I4B chips in early October 2015, when the IBL was kept off and irradiated for a short time period (during two LHC fills). Such effect was reproduced during an irradiation campaign with 16 MeV protons and was observed during X-ray irradiation of CMS DC-DC converters. More systematic studies are needed for better understanding of this effect.

CMS observed SEU effects in the pixel detector. The most pronounced effect on data taking came from SEUs in the TBM chips of the Phase-1 detector. Because of an unprotected transistor their rate was greatly enhanced and in addition SEUs could result in the need for a power-on reset. These SEUs subsequently led to the discovery of the DC-DC converter problem during 2017. SEUs in the ROCs are also observed and the rates were quantified and found to be consistent with expectations. Particular emphasis was placed on the recovery mechanism. Actions were taken to mitigate the impact on the data quality and to limit the dead time in the DAQ system whenever a certain fraction of detector was affected. An upgrade of the control firmware for the 2018 run greatly reduced the recovery time needed.

The entire ATLAS tracker was affected by SEU, with different level of severity depending on the proximity and peculiarity of some of the electronics components. In the ATLAS IBL, SEUs were observed at rates close to the expectation based on previous tests in 24 GeV proton beam. SEUs in the global and local pixel configuration memories of FE-I4B chip were observed during LHC fills which had several consequences, including: module de-synchronization, current jumps, quiet modules, quiet pixels, noisy pixels, and broken clusters. Even in this case, a recovery mechanism was put in place in

2017, performing a regular reconfiguration of the FE-I4B global registers in the entire detector without introducing additional DAQ dead time. Furthermore, by read-back measurements and simulations of the electronics, it was demonstrated that SETs on the LOAD line of the DICE latch dominate the memory flips.

The ATLAS SCT observed and analysed the effects of SEU in their on-detector p-i-n diodes and in ROCs (ABCD). The macroscopic effect of such issues were respectively de-synchronization (bit flip in the trigger transmission) and noise (bit flip in the threshold value). Both measurements show a good agreement with the extrapolations from test beam results.

The ATLAS TRT also observed an effect on their ROCs (DTMROCs), in particular in the configuration registers. For this reason a continuous polling and rewriting of such registers was implemented in the DAQ system using the abort gap timing in the LHC orbit.

For what concerns the damage from NIEL, ATLAS TRT analogue electronics (ASDBLR, BiCMOS DMILL radiation hard process) experienced a shift of the effective threshold cause by a loss of gain. This effect could be reproduced during an irradiation campaign at BNL and shows a saturation effect at about 30 kGy.

ATLAS SCT observed an effect on the opto-electronics, measuring the decrease of power of the on-detector VCSELs and a decrease of photo-current of the on-detector p-i-n diodes. Both effects are in good agreement with the test beam results even if the VCSEL optical power degradation seems a bit higher than expected considering the longer annealing periods during the LHC operation respect to the test beam campaigns.

CMS strips has also observed an impact of radiation on its optical links. The evolution of the optical link properties is monitored regularly during operations using optical link set up runs which scan gain and bias of the LLDs. As expected, a clear shift of the threshold current during Run 2 was seen. Important correction factors in this measurement come from the temperature and the fluence seen by the device. The data are compared to simulation for periods with constant operating temperature and very good agreement between data and simulation was found.

CMS observed occupancy dependent inefficiencies in the Strip Tracker during 2015 and 2016. This was eventually traced to saturation effects in the pre-amplifier of the APV25 chip caused by slower than anticipated discharge times at low temperatures. A change of a configuration register cured the problem. Residual dynamic inefficiencies which are observed as function of increasing instantaneous luminosity are likely caused by heavily ionizing particles (HIP). The rate of HIP-like events was measured in special runs with non-zero suppressed readout.

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